

### Features

- AEC-Q100 Grade 2 temperature range (-40°C to 105°C). Grade 3 and 4 also available
- Any frequency between 1 MHz and 220 MHz, accurate to 6 decimal places. For frequency between 220 and 725 MHz, see [SiT9387](#)
- LVPECL, LVDS and HCSL output signaling types
- 0.23 ps RMS (typ) phase jitter (random, 12 kHz to 20 MHz)
- Frequency stability as low as  $\pm 10$  ppm – [contact SiTime](#)
- Industry-standard packages: 3.2 x 2.5, 7.0 x 5.0 mm.  
[Contact SiTime](#) for 5.0 x 3.2 mm package

### Applications

- Automotive, and other high reliability electronics
- Infotainment systems, collision detection devices and in-vehicle 10/40/100 Gbps Ethernet



### Electrical Characteristics

**Table 1. Electrical Characteristics — Common to LVPECL, LVDS and HCSL**

All Min and Max limits in the Electrical Characteristics tables are specified over temperature and rated operating voltage with standard output termination show in the termination diagrams. Typical values are at 25°C and nominal supply voltage.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
<b>Frequency Range</b>						
Output Frequency Range	f	1	–	220	MHz	Accurate to 6 decimal places
<b>Frequency Stability</b>						
Frequency Stability		-10	–	+10	ppm	Inclusive of initial tolerance, operating temperature, rated power supply voltage and load variations. <a href="#">Contact SiTime</a> for $\pm 10$ ppm
		-20	–	+20	ppm	
		-25	–	+25	ppm	
		-50	–	+50	ppm	
First Year Aging	F_1y	–	$\pm 1$	–	ppm	At 25°C
<b>Temperature Range</b>						
Operating Temperature Range	T_use	-20	–	+70	°C	AEC-Q100 Grade 4
		-40	–	+85	°C	AEC-Q100 Grade 3
		-40	–	+105	°C	AEC-Q100 Grade 2
<b>Supply Voltage</b>						
Supply Voltage	Vdd	2.97	3.3	3.63	V	
		2.70	3.0	3.30	V	
		2.52	2.8	3.08	V	
		2.25	2.5	2.75	V	
<b>Input Characteristics</b>						
Input Voltage High	VIH	70%	–	–	Vdd	Pin 1, OE
Input Voltage Low	VIL	–	–	30%	Vdd	Pin 1, OE
Input Pull-up Impedance	Z_in	–	100	-	k $\Omega$	Pin 1, OE logic high or logic low
<b>Output Characteristics</b>						
Duty Cycle	DC	45	–	55	%	
<b>Startup and OE Timing</b>						
Start-up Time	T_start	–	–	3.0	ms	Measured from the time Vdd reaches its rated minimum value
OE Enable/Disable Time	T_oe	–	–	3.8	$\mu$ s	f = 156.25 MHz. Measured from the time OE pin reaches rated VIH and VIL to the time clock pins reach 90% of swing and high-Z. See <a href="#">Figure 6</a> and <a href="#">Figure 7</a>

Table 2. Electrical Characteristics – LVPECL

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
<b>Current Consumption</b>						
Current Consumption	I <sub>dd</sub>	–	–	89	mA	Excluding Load Termination Current, V <sub>dd</sub> = 3.3 V or 2.5 V
OE Disable Supply Current	I <sub>OE</sub>	–	–	58	mA	OE = Low
Output Disable Leakage Current	I <sub>leak</sub>	–	0.15	–	μA	OE = Low
Maximum Output Current	I <sub>driver</sub>	–	–	33	mA	Maximum average current drawn from OUT+ or OUT-
<b>Output Characteristics</b>						
Output High Voltage	VOH	V <sub>dd</sub> -1.15	–	V <sub>dd</sub> -0.7	V	See Figure 2
Output Low Voltage	VOL	V <sub>dd</sub> -2.0	–	V <sub>dd</sub> -1.5	V	See Figure 2
Output Differential Voltage Swing	V <sub>Swing</sub>	1.2	1.6	2.0	V	See Figure 3
Rise/Fall Time	Tr, Tf	–	225	310	ps	20% to 80%, see Figure 3
<b>Jitter – 7.0 x 5.0 package</b>						
RMS Period Jitter <sup>(1)</sup>	T <sub>jitt</sub>	–	1.0	1.6	ps	f = 100, 156.25 or 212.5 MHz, V <sub>dd</sub> = 3.3 V or 2.5 V
RMS Phase Jitter (random)	T <sub>phj</sub>	–	0.225	0.270	ps	f = 156.25 MHz, Integration bandwidth = 12 kHz to 20 MHz, all V <sub>dd</sub> levels, includes spurs. Temperature ranges -20 to 70°C and -40 to 85°C
		–	0.225	0.300	ps	f = 156.25 MHz, Integration bandwidth = 12 kHz to 20 MHz, all V <sub>dd</sub> levels, includes spurs. Temperature range -40 to 105°C
		–	0.1	–	ps	f = 156.25 or 322.265625 MHz, IEEE802.3-2005 10GbE jitter mask integration bandwidth = 1.875 MHz to 20 MHz, includes spurs, all V <sub>dd</sub> levels
<b>Jitter – 3.2 x 2.5 package</b>						
RMS Period Jitter <sup>(1)</sup>	T <sub>jitt</sub>	–	1.0	1.6	ps	f = 100, 156.25 or 212.5 MHz, V <sub>dd</sub> = 3.3 V or 2.5 V
RMS Phase Jitter (random)	T <sub>phj</sub>	–	0.225	0.275	ps	f = 156.25 MHz, Integration bandwidth = 12 kHz to 20 MHz, all V <sub>dd</sub> levels, includes spurs. Temperature range -20 to 70°C and -40 to 85°C
		–	0.225	0.340	ps	f = 156.25 MHz, Integration bandwidth = 12 kHz to 20 MHz, all V <sub>dd</sub> levels, includes spurs. Temperature range -40 to 105°C
		–	0.1	–	ps	f = 156.25 or 322.265625 MHz, IEEE802.3-2005 10GbE jitter mask integration bandwidth = 1.875 MHz to 20 MHz, includes spurs, all V <sub>dd</sub> levels

**Notes:**

1. Measured according to JESD65B.

Table 3. Electrical Characteristics – LVDS

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
<b>Current Consumption</b>						
Current Consumption	I <sub>dd</sub>	–	–	79	mA	Excluding Load Termination Current, V <sub>dd</sub> = 3.3 V or 2.5 V
OE Disable Supply Current	I <sub>OE</sub>	–	–	58	mA	OE = Low
Output Disable Leakage Current	I <sub>leak</sub>	–	0.15	–	μA	OE = Low
<b>Output Characteristics</b>						
Differential Output Voltage	VOD	250	–	450	mV	See Figure 4
VOD Magnitude Change	ΔVOD	–	–	50	mV	See Figure 4
Offset Voltage	VOS	1.125	–	1.375	V	See Figure 4
VOS Magnitude Change	ΔVOS	–	–	50	mV	See Figure 4
Rise/Fall Time	T <sub>r</sub> , T <sub>f</sub>	–	400	515	ps	Measured with 2 pF capacitive loading to GND, 20% to 80%, see Figure 5
<b>Jitter – 7.0 x 5.0 package</b>						
RMS Period Jitter <sup>[2]</sup>	T <sub>jitt</sub>	–	1.0	1.6	ps	f = 100, 156.25 or 212.5 MHz, V <sub>dd</sub> = 3.3 V or 2.5 V
RMS Phase Jitter (random)	T <sub>phj</sub>	–	0.215	0.265	ps	f = 156.25 MHz, Integration bandwidth = 12 kHz to 20 MHz, all V <sub>dd</sub> levels, includes spurs. Temperature ranges -20 to 70°C and -40 to 85°C.
		–	0.215	0.300	ps	f = 156.25 MHz, Integration bandwidth = 12 kHz to 20 MHz, all V <sub>dd</sub> levels, includes spurs. Temperature range -40 to 105°C
		–	0.1	–	ps	f = 156.25 or 322.265625 MHz, IEEE802.3-2005 10GbE jitter mask integration bandwidth = 1.875 MHz to 20 MHz, includes spurs, all V <sub>dd</sub> levels.
<b>Jitter – 3.2 x 2.5 package</b>						
RMS Period Jitter <sup>[2]</sup>	T <sub>jitt</sub>	–	1.0	1.6	ps	f = 100, 156.25 or 212.5 MHz, V <sub>dd</sub> = 3.3 V or 2.5 V
RMS Phase Jitter (random)	T <sub>phj</sub>	–	0.235	0.275	ps	f = 156.25 MHz, Integration bandwidth = 12 kHz to 20 MHz, all V <sub>dd</sub> levels, includes spurs. Temperature ranges -20 to 70°C and -40 to 85°C
		–	0.235	0.320	ps	f = 156.25 MHz, Integration bandwidth = 12 kHz to 20 MHz, all V <sub>dd</sub> levels, includes spurs. Temperature range -40 to 105°C
		–	0.1	–	ps	f = 156.25 or 322.265625 MHz, IEEE802.3-2005 10GbE jitter mask integration bandwidth = 1.875 MHz to 20 MHz, includes spurs, all V <sub>dd</sub> levels

## Notes:

2. Measured according to JESD65B.

Table 4. Electrical Characteristics – HCSL

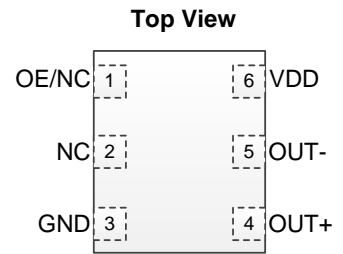
Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
<b>Current Consumption</b>						
Current Consumption	I <sub>dd</sub>	–	–	92	mA	Excluding Load Termination Current, V <sub>dd</sub> = 3.3 V or 2.5 V
OE Disable Supply Current	I <sub>OE</sub>	–	–	58	mA	OE = Low
Output Disable Leakage Current	I <sub>leak</sub>	–	0.15	–	μA	OE = Low
Maximum Output Current	I <sub>driver</sub>	–	–	35	mA	Maximum average current drawn from OUT+ or OUT-
<b>Output Characteristics</b>						
Output High Voltage	VOH	0.60	–	0.90	V	See <a href="#">Figure 2</a>
Output Low Voltage	VOL	-0.05	–	0.08	V	See <a href="#">Figure 2</a>
Output Differential Voltage Swing	V <sub>Swing</sub>	1.2	1.4	1.80	V	See <a href="#">Figure 3</a>
Rise/Fall Time	Tr, Tf	–	360	495	ps	Measured with 2 pF capacitive loading to GND, 20% to 80%, see <a href="#">Figure 3</a>
<b>Jitter – 7.0 x 5.0 package</b>						
RMS Period Jitter <sup>[3]</sup>	T <sub>jitt</sub>	–	1.0	1.6	ps	f = 100, 156.25 or 212.5 MHz, V <sub>dd</sub> = 3.3 V or 2.5 V
RMS Phase Jitter (random)	T <sub>phj</sub>	–	0.220	0.270	ps	f = 156.25 MHz, Integration bandwidth = 12 kHz to 20 MHz, all V <sub>dd</sub> levels, includes spurs. Temperature range -20 to 70°C and -40 to 85°C.
		–	0.220	0.300	ps	f = 156.25 MHz, Integration bandwidth = 12 kHz to 20 MHz, all V <sub>dd</sub> levels, includes spurs. Temperature range -40 to 105°C
		–	0.1	–	ps	f = 156.25 or 322.265625 MHz, IEEE802.3-2005 10GbE jitter mask integration bandwidth = 1.875 MHz to 20 MHz, includes spurs, all V <sub>dd</sub> levels.
<b>Jitter – 3.2 x 2.5 package</b>						
RMS Period Jitter <sup>[3]</sup>	T <sub>jitt</sub>	–	1.0	1.6	ps	f = 100, 156.25 or 212.5 MHz, V <sub>dd</sub> = 3.3 V or 2.5 V
RMS Phase Jitter (random)	T <sub>phj</sub>	–	0.230	0.275	ps	f = 156.25 MHz, Integration bandwidth = 12 kHz to 20 MHz, all V <sub>dd</sub> levels, includes spurs. Temperature ranges -20 to 70°C and -40 to 85°C.
		–	0.230	0.340	ps	f = 156.25 MHz, Integration bandwidth = 12 kHz to 20 MHz, all V <sub>dd</sub> levels, includes spurs. Temperature range -40 to 105°C
		–	0.1	–	ps	f = 156.25 or 322.265625 MHz, IEEE802.3-2005 10GbE jitter mask integration bandwidth = 1.875 MHz to 20 MHz, includes spurs, all V <sub>dd</sub> levels.

**Notes:**

- Measured according to JESD65B.

**Table 5. Pin Description**

Pin	Map	Functionality	
1	OE/NC	Output Enable (OE)	H <sup>[5]</sup> : specified frequency output L: output is high impedance
		Non Connect (NC)	H or L or Open: No effect on output frequency or other device functions
2	NC	NA	No Connect; Leave it floating or connect to GND for better heat dissipation
3	GND	Power	Vdd Power Supply Ground
4	OUT+	Output	Oscillator output
5	OUT-	Output	Complementary oscillator output
6	Vdd	Power	Power supply voltage <sup>[6]</sup>



**Figure 1. Pin Assignments**

**Notes:**

- In OE mode, a pull-up resistor of 10 kΩ or less is recommended if pin 1 is not externally driven.
- A capacitor of value 0.1 μF or higher between Vdd and GND is required. An additional 10 μF capacitor between Vdd and GND is required for the best phase jitter performance.

**Table 6. Absolute Maximum Ratings**

Attempted operation outside the absolute maximum ratings may cause permanent damage to the part. Actual performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

Parameter	Min.	Max.	Unit
Vdd	-0.5	4.0	V
VIH		Vdd + 0.3V	V
VIL	-0.3		V
Storage Temperature	-65	150	°C
Maximum Junction Temperature		130	°C
Soldering Temperature (follow standard Pb-free soldering guidelines)		260	°C

**Table 7. Thermal Considerations<sup>[7]</sup>**

Package	$\theta_{JA}$ , 4 Layer Board (°C/W)	$\theta_{JC}$ , Bottom (°C/W)
3225, 6-pin	80	30
7050, 6-pin	52	19

**Notes:**

- Refer to JESD51 for  $\theta_{JA}$  and  $\theta_{JC}$  definitions, and reference layout used to determine the  $\theta_{JA}$  and  $\theta_{JC}$  values in the above table.

**Table 8. Maximum Operating Junction Temperature<sup>[8]</sup>**

Max Operating Temperature (ambient)	Maximum Operating Junction Temperature
70°C	95°C
85°C	110°C
105°C	130°C

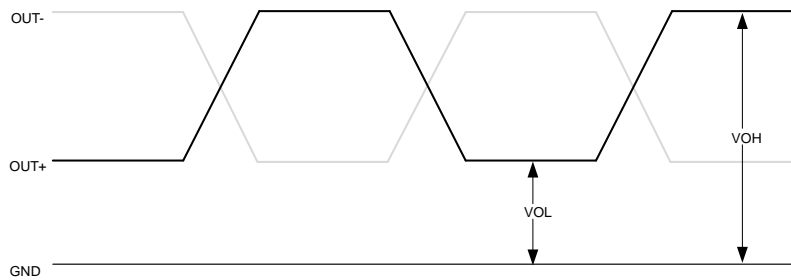
**Notes:**

- Datasheet specifications are not guaranteed if junction temperature exceeds the maximum operating junction temperature.

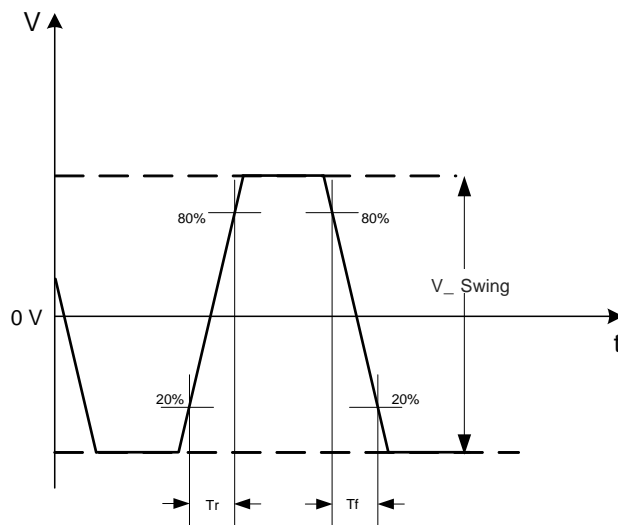
**Table 9. Environmental Compliance**

Parameter	Test Conditions	Value	Unit
Mechanical Shock Resistance	MIL-STD-883F, Method 2002	10,000	g
Mechanical Vibration Resistance	MIL-STD-883F, Method 2007	70	g
Soldering Temperature (follow standard Pb free soldering guidelines)	MIL-STD-883F, Method 2003	260	°C
Moisture Sensitivity Level	MSL1 @ 260°C		
Electrostatic Discharge (HBM)	HBM, JESD22-A114	2,000	V
Charge-Device Model ESD Protection	JESD220C101	750	V
Latch-up Tolerance	JESD78 Compliant		

### Waveform Diagrams (continued)

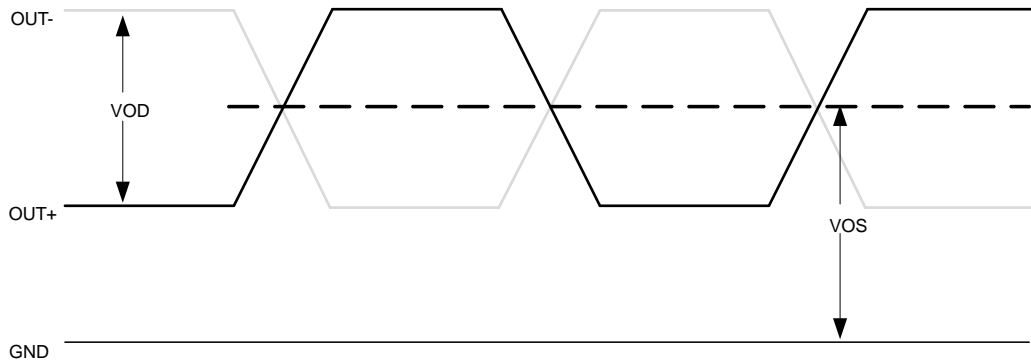


**Figure 2. LVPECL/HCSL Voltage Levels per Differential Pin (OUT+/OUT-)**

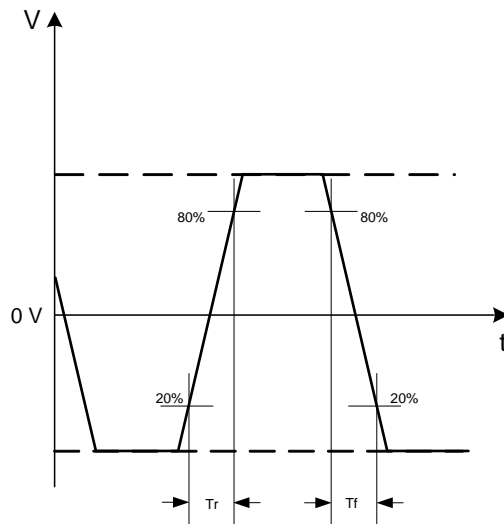


**Figure 3. LVPECL/HCSL Voltage Levels across Differential Pair**

**Waveform Diagrams (continued)**

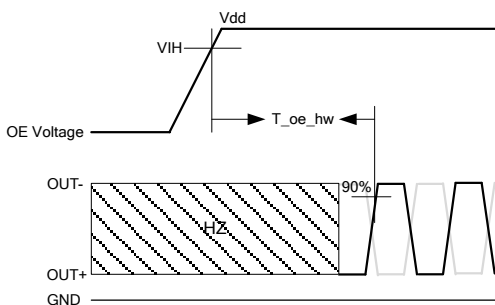


**Figure 4. LVDS Voltage Levels per Differential Pin (OUT+/OUT-)**

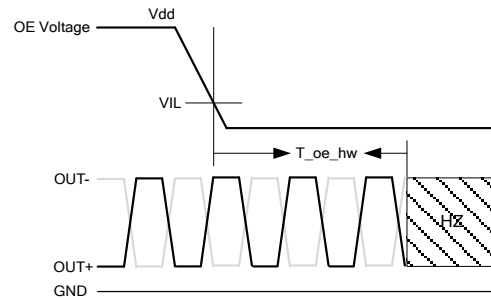


**Figure 5. LVDS Differential Waveform**

**Timing Diagrams**



**Figure 6. Hardware OE Enable Timing**



**Figure 7. Hardware OE Disable Timing**

## Termination Diagrams

### LVPECL

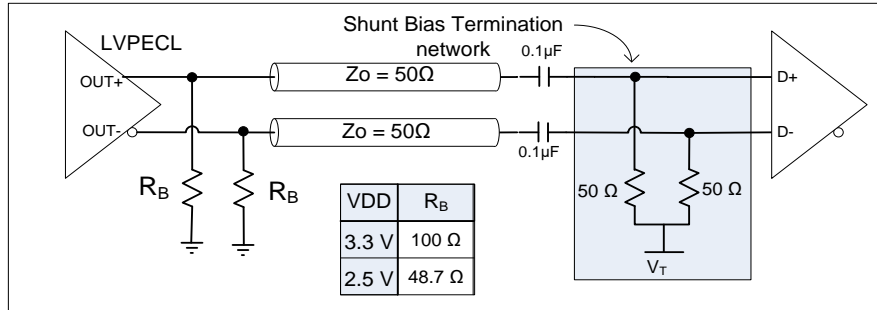


Figure 8. LVPECL with AC-coupled termination

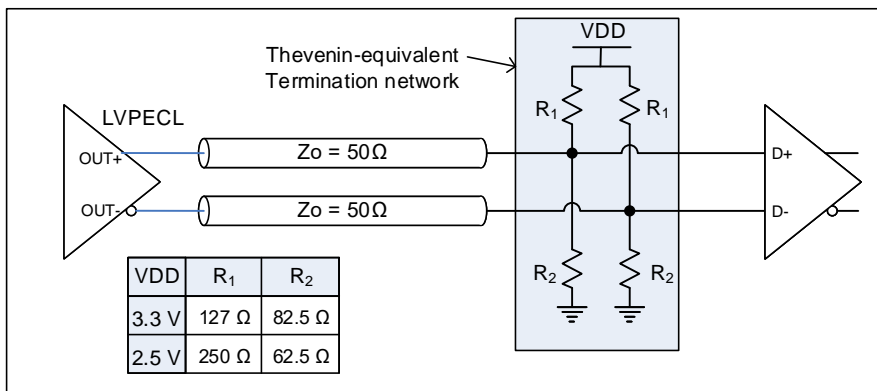


Figure 9. LVPECL DC-coupled load termination with Thevenin equivalent network

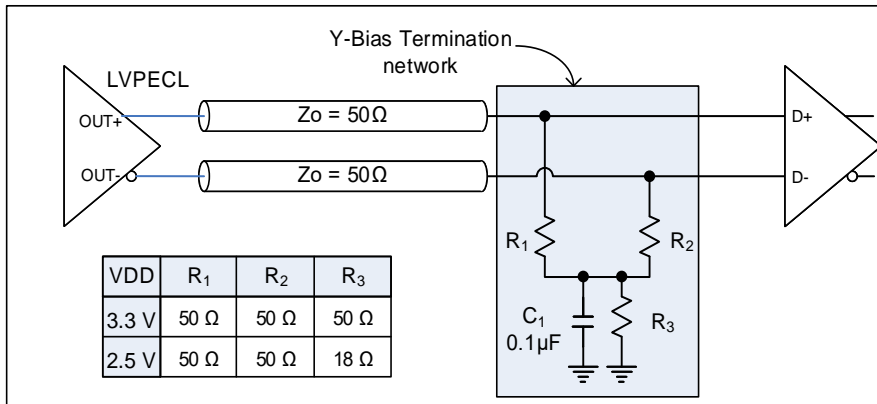


Figure 10. LVPECL with Y-Bias termination

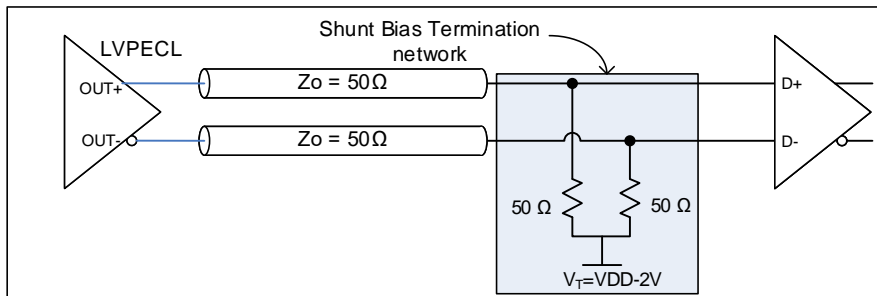


Figure 11. LVPECL with DC-coupled parallel shunt load termination



Termination Diagrams (continued)

LVDS

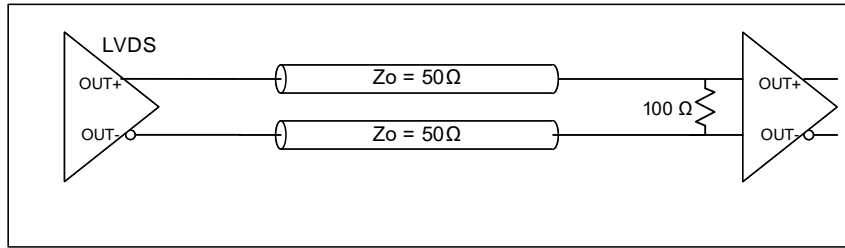


Figure 12. LVDS single DC termination at the load

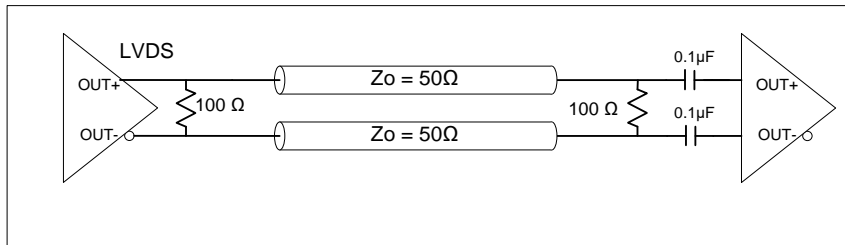


Figure 13. LVDS double AC termination with capacitor close to the load

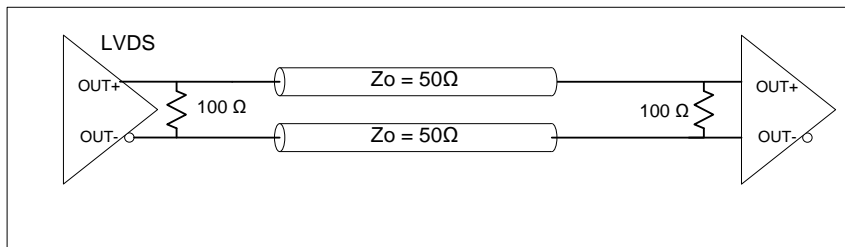


Figure 14. LVDS double DC termination

HCSL

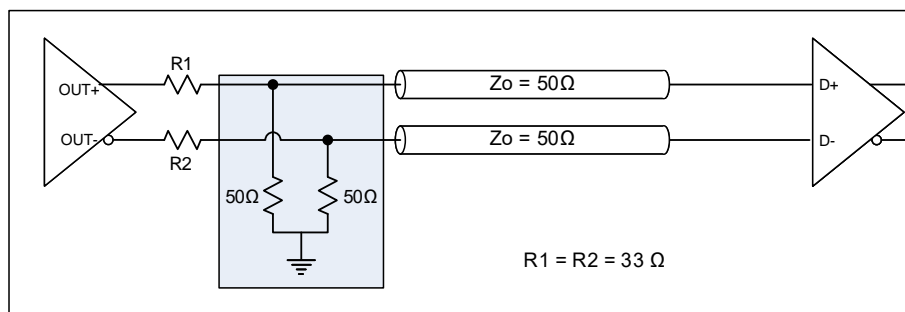


Figure 15. HCSL interface termination

## Dimensions and Patterns

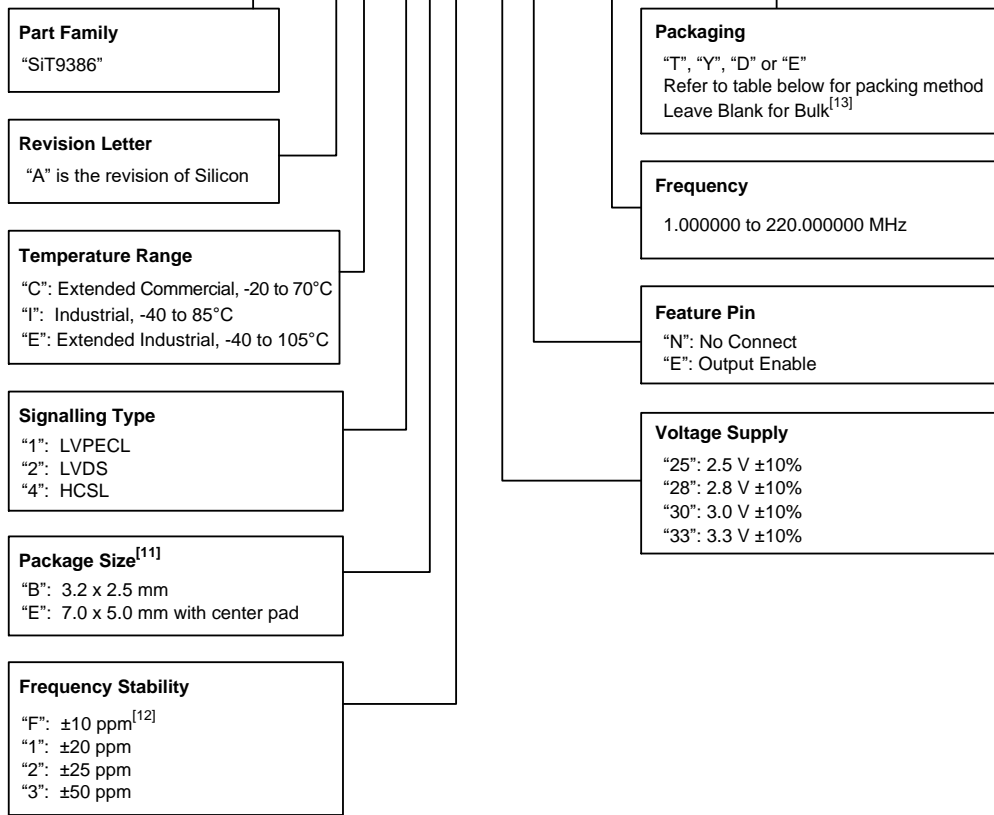
Package Size – Dimensions (Unit: mm) <sup>[9]</sup>	Recommended Land Pattern (Unit: mm) <sup>[10]</sup>																																																																																						
<p><b>3.2 x 2.5 x 0.85 mm</b></p> <table border="1"> <thead> <tr> <th></th> <th>SYMBOL</th> <th>MIN</th> <th>NOM</th> <th>MAX</th> </tr> </thead> <tbody> <tr> <td>TOTAL THICKNESS</td> <td>A</td> <td>0.800</td> <td>0.850</td> <td>0.900</td> </tr> <tr> <td>STAND OFF</td> <td>A1</td> <td>0.000</td> <td>0.035</td> <td>0.050</td> </tr> <tr> <td rowspan="2">BODY SIZE</td> <td>X</td> <td colspan="3">D 3.200 BSC</td> </tr> <tr> <td>Y</td> <td colspan="3">E 2.500 BSC</td> </tr> <tr> <td>LEAD WIDTH</td> <td>b</td> <td>0.550</td> <td>0.600</td> <td>0.650</td> </tr> <tr> <td rowspan="2">LEAD LENGTH</td> <td>L</td> <td>0.650</td> <td>0.700</td> <td>0.750</td> </tr> <tr> <td>L1</td> <td colspan="3">0.800 REF</td> </tr> <tr> <td>LEAD PITCH</td> <td>e</td> <td colspan="3">1.100 BSC</td> </tr> <tr> <td>PACKAGE TOLERANCE</td> <td>aaa</td> <td colspan="3">0.100</td> </tr> <tr> <td>MOLD FLATNESS</td> <td>bbb</td> <td colspan="3">0.100</td> </tr> <tr> <td>COPLANARITY</td> <td>ccc</td> <td colspan="3">0.080</td> </tr> <tr> <td>DIMPLE WIDTH</td> <td>T</td> <td colspan="3">0.150 REF</td> </tr> <tr> <td>DIMPLE LENGTH</td> <td>P</td> <td colspan="3">0.150 REF</td> </tr> <tr> <td>DIMPLE DEPTH</td> <td>A2</td> <td colspan="3">0.100 REF</td> </tr> </tbody> </table> <p>Notes: 1. All dimensions are in millimeters</p> <table border="1"> <thead> <tr> <th colspan="2">Package Outline</th> </tr> </thead> <tbody> <tr> <td>6L PQFD</td> <td>POD-038-PQFD-006-C03225</td> </tr> <tr> <td colspan="2">3.200x2.500x0.850 mm</td> </tr> <tr> <td>2020/09/23 Rev C00</td> <td></td> </tr> </tbody> </table>		SYMBOL	MIN	NOM	MAX	TOTAL THICKNESS	A	0.800	0.850	0.900	STAND OFF	A1	0.000	0.035	0.050	BODY SIZE	X	D 3.200 BSC			Y	E 2.500 BSC			LEAD WIDTH	b	0.550	0.600	0.650	LEAD LENGTH	L	0.650	0.700	0.750	L1	0.800 REF			LEAD PITCH	e	1.100 BSC			PACKAGE TOLERANCE	aaa	0.100			MOLD FLATNESS	bbb	0.100			COPLANARITY	ccc	0.080			DIMPLE WIDTH	T	0.150 REF			DIMPLE LENGTH	P	0.150 REF			DIMPLE DEPTH	A2	0.100 REF			Package Outline		6L PQFD	POD-038-PQFD-006-C03225	3.200x2.500x0.850 mm		2020/09/23 Rev C00		<p><b>3.2 x 2.5 x 0.85 mm</b></p> <p style="text-align: center;"> <a href="#">POD-038-PQFD-006-C03225-C00.pdf</a> </p>					
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**Notes:**

9. Top Marking: Y denotes manufacturing origin and XXXX denotes manufacturing lot number. The value of "Y" will depend on the assembly location of the device.
10. A capacitor of value 0.1  $\mu$ F or higher between Vdd and GND is required. An additional 10  $\mu$ F capacitor between Vdd and GND is required for the best phase jitter performance
11. The center pad has no electrical function. Soldering down the center pad to the GND is recommended for best thermal dissipation, but is optional.

## Ordering Information

### SiT9386AC-1B2-33E123.456789T



**Notes:**

- 12. [Contact SiTime](#) for 5.0 x 3.2 mm package.
- 13. [Contact SiTime](#) for ±10 ppm option.
- 14. Bulk is available for sampling only.

**Table 10. Ordering Codes for Supported Tape & Reel Packing Method**

Device Size (mm x mm)	8 mm T&R (3ku)	8 mm T&R (1ku)	12 mm T&R (3ku)	12 mm T&R (1ku)	16 mm T&R (3ku)	16 mm T&R (1ku)
7.0 x 5.0	—	—	—	—	T	Y
3.2 x 2.5	D	E	—	—	—	—

Table 11. Additional Information

Document	Description	Download Link
<b>ECCN #: EAR99</b>	Five character designation used on the commerce Control List (CCL) to identify dual use items for export control purposes.	—
<b>Part number Generator</b>	Tool used to create the part number based on desired features.	<a href="https://www.sitime.com/part-number-generator">https://www.sitime.com/part-number-generator</a>
<b>Manufacturing Notes</b>	Tape & Reel dimension, reflow profile and other manufacturing related info	<a href="https://www.sitime.com/sites/default/files/gated/Manufacturing-Notes-for-SiTime-Products.pdf">https://www.sitime.com/sites/default/files/gated/Manufacturing-Notes-for-SiTime-Products.pdf</a>
<b>Qualification Reports</b>	RoHS report, reliability reports, composition reports	<a href="http://www.sitime.com/support/quality-and-reliability">http://www.sitime.com/support/quality-and-reliability</a>
<b>Performance Reports</b>	Additional performance data such as phase noise, current consumption and jitter for selected frequencies	<a href="http://www.sitime.com/support/performance-measurement-report">http://www.sitime.com/support/performance-measurement-report</a>
<b>Termination Techniques</b>	Termination design recommendations	<a href="http://www.sitime.com/support/application-notes">http://www.sitime.com/support/application-notes</a>
<b>Layout Techniques</b>	Layout recommendations	<a href="http://www.sitime.com/support/application-notes">http://www.sitime.com/support/application-notes</a>

Table 12. Revision History

Revision	Release Date	Change Summary
0.1	8-Mar-2021	Initial draft
0.87	6-Nov-2017	Updated package drawings Corrected tape/reel ordering information Updated Electrical Characteristics based on characterization Included max numbers for IPJ Added additional information table Corrected formatting issues Increased temperature range from 95°C to 105°C Removed $\pm 10$ ppm options for automotive and industrial temperature ranges Changed $\pm 20$ ppm to "contact SiTime" Updated termination diagrams Lower mechanical shock from 20,000 to 10,000 g
0.90	24-Nov-2017	Ordering information updates and page layout changes
1.0	15-Mar-2019	Updated Electrical Characteristics tables Updated waveform diagrams Added OE enable/disable timing diagrams Updated package dimensions Added an AEC-Q100 Grade 4 temperature option Updated the ordering information
1.01	9-Mar-2021	Updated L1 and Dimple Width package dimensions for 3.2 x 2.5 mm package Updated hyperlinks and changed rev table date format

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[SIT8918AA-11-33S-16.000000G](#) [SIT9122AI2C233E300.000000X](#) [9120AC-2D2-33E212.500000](#) [9102AI-243N25E100.00000](#) [8208AC-82-](#)  
[18E-25.00000](#) [8008AI-72-XXE-24.545454E](#) [8004AC-13-33E-133.33000X](#) [AS-4.9152-16-SMD-TR](#) [ASFL1-48.000MHZ-LC-T](#)  
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[9102AI-233N25E200.00000](#) [9102AI-232H25S125.00000](#) [9102AI-133N25E200.00000](#) [9102AC-283N25E200.00000](#) [9001AC-33-33E1-30.000](#)  
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[100.000M TR](#) [SIT1602BC-83-33E-10.000000Y](#) [8003AI-12-33S-40.00000Y](#) [1602BI-13-33S-19.200000E](#)