

4Gb DDR4 SDRAM

Lead-Free&Halogen-Free

(RoHS Compliant)

H5AN4G4NBJR-xxC

H5AN4G8NBJR-xxC

H5AN4G6NBJR-xxC

H5AN4G8NBJR-xxI

H5AN4G6NBJR-xxI

* SK hynix reserves the right to change products or specifications without notice.

Revision History

Revision No.	History	Draft Date	Remark
0.1	Initial Release	Apr. 2016	
0.2	Add Industrial Temperature Range	Oct. 2016	
1.0	x16 IDD, IPP Update	Dec. 2016	Page 32, 33
1.1	x16 IPP Typo	Dec. 2016	Page 33
1.2	x8 IDD, IPP Update	Jan. 2017	Page 32, 33
1.3	DBI Info. Update	Mar. 2017	Page 3
1.4	x4 IDD, IPP Update x16 3200Mbps IDD, IPP Update	Jun. 2017	Page 32,33
1.5	3200Mbps IDD, IPP Update	Jun. 2017	Page 32,33
1.6	AC timing update 2666Mbps update	Dec. 2017	Page 17
1.7	3200Mbps Parameter update	Mar. 2018	

Description

The H5AN4G4NBJR-xxC, H5AN4G8NBJR-xxC, H5AN4G6NBJR-xxC, H5AN4G8NBJR-xxI, H5AN4G6NBJR-xxI are a 4Gb CMOS Double Data Rate IV (DDR4) Synchronous DRAM, ideally suited for the main memory applications which requires large memory density and high bandwidth. SK hynix 4Gb DDR4 SDRAMs offer fully synchronous operations referenced to both rising and falling edges of the clock. While all addresses and control inputs are latched on the rising edges of the CK (falling edges of the CK), Data, Data strobes and Write data masks inputs are sampled on both rising and falling edges of it. The data paths are internally pipelined and 8-bit prefetched to achieve very high bandwidth.

Device Features and Ordering Information

FEATURES

- VDD=VDDQ=1.2V +/- 0.06V
- Fully differential clock inputs (CK, $\overline{\text{CK}}$) operation
- Differential Data Strobe (DQS, $\overline{\text{DQS}}$)
- On chip DLL align DQ, DQS and $\overline{\text{DQS}}$ transition with CK transition
- DM masks write data-in at the both rising and falling edges of the data strobe
- All addresses and control inputs except data, data strobes and data masks latched on the rising edges of the clock
- Programmable CAS latency 9, 11, 12, 13, 14, 15, 16, 17, 18, 19 and 20
- Programmable additive latency 0, CL-1, and CL-2 supported (x4/x8 only)
- Programmable CAS Write latency (CWL) = 9, 10, 11, 12, 14, 16, 18
- Programmable burst length 4/8 with both nibble sequential and interleave mode
- BL switch on the fly
- 16banks
- AverageRefreshCycle (Tcase of 0 °C~95 °C)
 - 7.8 μs at 0 °C ~ 85 °C
 - 3.9 μs at 85 °C ~ 95 °C
- Operating Temperature Range
 - Commercial Temperature (0 °C~ 95 °C)
 - Industrial Temperature (-40°C~ 95 °C)
- JEDEC standard 78ball FBGA(x4/x8), 96ball FBGA(x16)
- Driver strength selected by MRS
- Dynamic On Die Termination supported
- Two Termination States such as RTT_PARK and RTT_NOM switchable by ODT pin
- Asynchronous RESET pin supported
- ZQ calibration supported
- TDQS (Termination Data Strobe) supported (x8 only)
- Write Levelization supported
- 8 bit pre-fetch
- This product in compliance with the RoHS directive.
- Internal Vref DQ level generation is available
- Write CRC is supported at all speed grades
- Maximum Power Saving Mode is supported
- TCAR(Temperature Controlled Auto Refresh) mode is supported
- LP ASR(Low Power Auto Self Refresh) mode is supported
- Fine Granularity Refresh is supported
- Per DRAM Addressability is supported
- Geardown Mode(1/2 rate, 1/4 rate) is supported
- Programmable Preamble for read and write is supported
- Self Refresh Abort is supported
- CA parity (Command/Address Parity) mode is supported
- Bank Grouping is applied, and CAS to CAS latency (tCCD_L, tCCD_S) for the banks in the same or different bank group accesses are available
- DBI(Data Bus Inversion) is supported(x8/x16)

ORDERING INFORMATION

Part No.	Configuration	Package
H5AN4G4NBJR-*xxC	1G x 4	78ball FBGA
H5AN4G8NBJR-*xxC	512M x 8	
H5AN4G8NBJR-*xxI		
H5AN4G6NBJR-*xxC	256M x 16	96ball FBGA
H5AN4G6NBJR-*xxI		

* xx means Speed Bin Grade

OPERATING FREQUENCY

MT/s	Grade	tCK (ns)	CAS Latency (tCK)	tRCD (ns)	tRP (ns)	tRAS (ns)	tRC (ns)	CL-tRCD-tRP
DDR4-1600	-PB	1.25	11	13.75 (13.50)*	13.75 (13.50)*	35	48.75 (48.50)*	11-11-11
DDR4-1866	-RD	1.071	13	13.92 (13.50)*	13.92 (13.50)*	34	47.92 (47.50)*	13-13-13
DDR4-2133	-TF	0.937	15	14.06 (13.50)*	14.06 (13.50)*	33	47.06 (46.50)*	15-15-15
DDR4-2400	-UH	0.833	17	14.16 (13.75)*	14.16 (13.75)*	32	46.16 (45.75)*	17-17-17
DDR4-2666	-VK	0.75	19	14.25 (13.75)*	14.25 (13.75)*	32	46.25 (45.75)*	19-19-19
DDR4-3200	-XN	0.625	22	13.75	13.75	33	46.75	22-22-22

*SK hynix DRAM devices support optional downbinning to CL17, CL15, CL13 and CL11. SPD setting is programmed to match.

Package Ballout/Mechanical Dimension

x4 Package Ball out (Top view): 78ball FBGA Package

	1	2	3	4	5	6	7	8	9	
A	VDD	VSSQ	NC				DM_n, DBI_n	VSSQ	VSS	A
B	VPP	VDDQ	DQS_c				DQ1	VDDQ	ZQ	B
C	VDDQ	DQ0	DQS_t				VDD	VSS	VDDQ	C
D	VSSQ	NC	DQ2				DQ3	NC	VSSQ	D
E	VSS	VDDQ	NC				NC	VDDQ	VSS	E
F	VDD	NC	ODT				CK_t	CK_c	VDD	F
G	VSS	NC	CKE				CS_n	NC	TEN	G
H	VDD	WE_n A14	ACT_n				CAS_n A15	RAS_n A16	VSS	H
J	VREFCA	BG0	A10 AP				A12 BC_n	BG1	VDD	J
K	VSS	BA0	A4				A3	BA1	VSS	K
L	RESET_n	A6	A0				A1	A5	ALERT_n	L
M	VDD	A8	A2				A9	A7	VPP	M
N	VSS	A11	PAR				NC	A13	VDD	N
	1	2	3	4	5	6	7	8	9	

x8 Package Ball out (Top view): 78ball FBGA Package

	1	2	3	4	5	6	7	8	9	
A	VDD	VSSQ	TDQS_c				DM_n/DBI_n TDQS_t	VSSQ	VSS	A
B	VPP	VDDQ	DQS_c				DQ1	VDDQ	ZQ	B
C	VDDQ	DQ0	DQS_t				VDD	VSS	VDDQ	C
D	VSSQ	DQ4	DQ2				DQ3	DQ5	VSSQ	D
E	VSS	VDDQ	DQ6				DQ7	VDDQ	VSS	E
F	VDD	NC	ODT				CK_t	CK_c	VDD	F
G	VSS	NC	CKE				CS_n	NC	TEN	G
H	VDD	WE_n A14	ACT_n				CAS_n A15	RAS_n A16	VSS	H
J	VREFCA	BG0	A10 AP				A12 BC_n	BG1	VDD	J
K	VSS	BA0	A4				A3	BA1	VSS	K
L	RESET_n	A6	A0				A1	A5	ALERT_n	L
M	VDD	A8	A2				A9	A7	VPP	M
N	VSS	A11	PAR				NC	A13	VDD	N
	1	2	3	4	5	6	7	8	9	

x16 Package Ball out (Top view): 96ball FBGA Package

	1	2	3	4	5	6	7	8	9	
A	VDDQ	VSSQ	DQU0				DQSU_c	VSSQ	VDDQ	A
B	VPP	VSS	VDD				DQSU_t	DQU1	VDD	B
C	VDDQ	DQU4	DQU2				DQU3	DQU5	VSSQ	C
D	VDD	VSSQ	DQU6				DQU7	VSSQ	VDDQ	D
E	VSS	DMU_n/ DBIU_n	VSSQ				DML_n/ DBIL_n	VSSQ	VSS	E
F	VSSQ	VDDQ	DQSL_c				DQL1	VDDQ	ZQ	F
G	VDDQ	DQL0	DQSL_t				VDD	VSS	VDDQ	G
H	VSSQ	DQL4	DQL2				DQL3	DQL5	VSSQ	H
J	VDD	VDDQ	DQL6				DQL7	VDDQ	VDD	J
K	VSS	CKE	ODT				CK_t	CK_c	VSS	K
L	VDD	WE_n A14	ACT_n				CS_n	RAS_n A16	VDD	L
M	VREFCA	BG0	A10/AP				A12 BC_n	CAS_n A15	VSS	M
N	VSS	BA0	A4				A3	BA1	TEN	N
P	RESET_n	A6	A0				A1	A5	ALERT_n	P
R	VDD	A8	A2				A9	A7	VPP	R
T	VSS	A11	PAR				NC	A13	VDD	T
	1	2	3	4	5	6	7	8	9	

Pin Functional Description

Symbol	Type	Function
CK_t, CK_c	Input	Clock: CK_t and CK_c are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c.
CKE, (CKE1)	Input	Clock Enable: CKE HIGH activates, and CKE Low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is asynchronous for Self-Refresh exit. After VREFCA and VREFDQ have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK, CK_c, ODT and CKE, are disabled during power-down. Input buffers, excluding CKE, are disabled during Self-Refresh.
CS_n, (CS1_n)	Input	Chip Select: All commands are masked when CS_n is registered HIGH. CS_n provides for external Rank selection on systems with multiple Ranks. CS_n is considered part of the command code.
C0,C1,C2	Input	Chip ID: Chip ID is only used for 3DS for 2,4,8high stack via TSV to select each slice of stacked component. Chip ID is considered part of the command code.
ODT, (ODT1)	Input	On Die Termination: ODT (registered HIGH) enables termination resistance internal to the DDR4 SDRAM. When enabled, ODT is only applied to each DQ, DQS_t, DQS_c and DM_n/DBI_n/TDQS_t,NU/TDQS_c (When TDQS is enabled via Mode Register A11=1 in MR1) signal for x8 configurations. For x16 configuration ODT is applied to each DQ, DQSU_c, DQSU_t, DQSL_t, DQSL_c, DMU_n, and DML_n signal. The ODT pin will be ignored if MR1 is programmed to disable RTT_NOM.
ACT_n	Input	Activation Command Input: ACT_n defines the Activation command being entered along with CS_n. The input into RAS_n/A16, CAS_n/A15 and WE_n/A14 will be considered as Row Address A16, A15 and A14.
RAS_n/A16, CAS_n/A15, WE_n/A14	Input	Command Inputs RAS_n/A16, CAS_n/A15 and WE_n/A14 (along with CS_n) define the command being entered. Those pins have multi function. For example, for activation with ACT_n Low, those are Addressing like A16,A15 and A14 but for non-activation command with ACT_n High, those are Command pins for Read, Write and other command defined in command truth table.
DM_n/DBI_n/ TDQS_t, (DMU_n/DBI- U_n), (DML_n/ DBIL_n)	Input/ Output	Input Data Mask and Data Bus Inversion: DM_n is an input mask signal for write data. Input data is masked when DM_n is sampled LOW coincident with that input data during a Write access. DM_n is sampled on both edges of DQS. DM is muxed with DBI function by Mode Register A10,A11,A12 setting in MR5. For x8 device, the function of DM or TDQS is enabled by Mode Register A11 setting in MR1. DBI_n is an input/output identifying whether to store/output the true or inverted data. If DBI_n is LOW, the data will be stored/output after inversion inside the DDR4 SDRAM and not inverted if DBI_n is HIGH. TDQS is only supported in x8.
BG0 - BG1	Input	Bank Group Inputs: BG0 - BG1 define to which bank group an Active, Read, Write or Pre-charge command is being applied. BG0 also determines which mode register is to be accessed during a MRS cycle. x4/8 have BG0 and BG1 but x16 has only BG0.
BA0 - BA1	Input	Bank Address Inputs: BA0 - BA1 define to which bank an Active, Read, Write or Pre-charge command is being applied. Bank address also determines if the mode register or extended mode register is to be accessed during a MRS cycle.

Symbol	Type	Function
A0 - A17	Input	Address Inputs: Provided the row address for ACTIVATE Commands and the column address for Read/Write commands to select one location out of the memory array in the respective bank. (A10/AP, A12/BC_n, RAS_n/A16, CAS_n/A15 and WE_n/A14 have additional functions, see other rows. The address inputs also provide the op-code during Mode Register Set commands. A17 is only defined for the x4 configuration.
A10 / AP	Input	Auto-precharge: A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. (HIGH: Autoprecharge; LOW: no Autoprecharge). A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses.
A12 / BC_n	Input	Burst Chop: A12 / BC_n is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. (HIGH, no burst chop; LOW: burst chopped). See command truth table for details.
RESET_n	Input	Active Low Asynchronous Reset: Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation. RESET_n is a CMOS rail to rail signal with DC high and low at 80% and 20% of V _{DD} .
DQ	Input/ Output	Data Input/ Output: Bi-directional data bus. If CRC is enabled via Mode register then CRC code is added at the end of Data Burst. Any DQ from DQ0~DQ3 may indicate the internal Vref level during test via Mode Register Setting MR4 A4=High. During this mode, RTT value should be set to Hi-Z. Refer to vendor specific datasheets to determine which DQ is used.
DQS_t, DQS_c, DQSU_t, DQSU_c, DQSL_t, DQSL_c	Input/ Output	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. For x16, DQSL corresponds to the data on DQ0-DQ7; DQSU corresponds to the data on DQ8-DQ15. The data strobe DQS_t, DQSL_t, and DQSU_t are paired with differential signals DQS_c, DQSL_c, and DQSU_c, respectively, to provide differential pair signaling to the system during reads and writes. DDR4 SDRAM supports differential data strobe only and does not support single-ended.
TDQS_t, TDQS_c	Output	Termination Data Strobe: TDQS_t/TDQS_c is applicable for x8 DRAMs only. When enabled via Mode Register A11 = 1 in MR1, the DRAM will enable the same termination resistance function on TDQS_t/TDQS_c that is applied to DQS_t/DQS_c. When disabled via mode register A11 = 0 in MR1, DM/DBI/TDQS will provide the data mask function or Data Bus Inversion depending on MR5; A11, 12, 10 and TDQS_c is not used. x4/x16 DRAMs must disable the TDQS function via mode register A11 = 0 in MR1.
PAR	Input	Command and Address Parity Input : DDR4 Supports Even Parity check in DRAMs with MR setting. Once it's enabled via Register in MR5, then DRAM calculates Parity with ACT_n, RAS_n/A16, CAS_n/A15, WE_n/A14, BG0-BG1, BA0-BA1, A17-A, and C0-C2(3DS devices). Input parity should maintain at the rising edge of the clock and at the same time with command & address with CS_n LOW.
ALERT_n	Output	Alert: It has multi functions such as CRC error flag, Command and Address Parity error flag as Output signal. If there is error in CRC, then Alert_n goes LOW for the period time interval and goes back HIGH. If there is error in Command Address Parity Check, then Alert_n goes LOW for relatively long period until on going DRAM internal recovery transaction to complete. During Connectivity Test mode, this pin works as input. Using this signal or not is dependent on system. In case of not connected as Signal, ALERT_n Pin must be bounded to VDD on board.

Symbol	Type	Function
TEN	Input	Connectivity Test Mode Enable: Required on x16 devices and optional input on x4/x8 with densities equal to or greater than 8Gb. HIGH in this pin will enable Connectivity Test Mode operation along with other pins. It is a CMOS rail to rail signal with AC high and low at 80% and 20% of VDD. Using this signal or not is dependent on System. This pin may be DRAM internally pulled low through a weak pull-down resistor to VSS.
NC		No Connect: No internal electrical connection is present.
V _{DDQ}	Supply	DQ Power Supply: 1.2 V +/- 0.06 V
V _{SSQ}	Supply	DQ Ground
V _{DD}	Supply	Power Supply: 1.2 V +/- 0.06 V
V _{SS}	Supply	Ground
V _{pp}	Supply	DRAM Activation Power Supply: 2.5V (2.375V min , 2.75 max)
V _{REFCA}	Supply	Reference voltage for CA
ZQ	Supply	Reference Pin for ZQ calibration

Note:

Input only pins (BG0-BG-1, BA0-BA1, A0-A17, ACT_n, RAS_n,/A16, CAS_n/A15, WE_n/A14, CS_n, CKE, ODT, and RESET_n) do not supply termination.

ROW AND COLUMN ADDRESS TABLE

4Gb

Configuration		1Gb x 4	512Mb x 8	256Mb x 16
Bank Address	# of Bank Groups	4	4	2
	BG Address	BG0~BG1	BG0~BG1	BG0
	Bank Address in a BG	BA0~BA1	BA0~BA1	BA0~BA1
Row Address		A0~A15	A0~A14	A0~A14
Column Address		A0~ A9	A0~ A9	A0~ A9
Page size		512B	1 KB	2 KB

Absolute Maximum Ratings

Absolute Maximum DC Ratings

Absolute Maximum DC Ratings

Symbol	Parameter	Rating	Units	NOTE
VDD	Voltage on VDD pin relative to Vss	-0.3 ~ 1.5	V	1,3
VDDQ	Voltage on VDDQ pin relative to Vss	-0.3 ~ 1.5	V	1,3
VPP	Voltage on VPP pin relative to Vss	-0.3 ~ 3.0	V	4
V _{IN} , V _{OUT}	Voltage on any pin except VREFCA relative to Vss	-0.3 ~ 1.5	V	1,3,5
T _{STG}	Storage Temperature	-55 to +100	°C	1,2

NOTE :

- Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability
- Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
- VDD and VDDQ must be within 300 mV of each other at all times; and VREFCA must be not greater than 0.6 x VDDQ, When VDD and VDDQ are less than 500 mV; VREFCA may be equal to or less than 300 mV
- VPP must be equal or greater than VDD/VDDQ at all times
- Overshoot area above 1.5V is specified in DDR4 Device Operation.

DRAM Component Operating Temperature Range Temperature Range

Symbol	Parameter	Rating	Units	Notes
T _{OPER}	Normal Operating Temperature Range	0 to 85	°C	1,2
	Extended Temperature Range	85 to 95	°C	1,4
	Industrial Temperature Range	-40 to 95	°C	1,3,4

Notes:

1. Operating Temperature T_{OPER} is the case surface temperature on the center / top side of the DRAM. For measurement conditions, please refer to the JEDEC document JESD51-2.
2. The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0 - 85°C under all operating conditions.
3. The industrial temperature range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between -40 - 85°C under all operating conditions.
4. Some applications require operation of the DRAM in the Extended Temperature Range between 85°C and 95°C case temperature. Full specifications are guaranteed in this range, but the following additional conditions apply:
 - a. Refresh commands must be doubled in frequency, therefore reducing the Refresh interval tREFI to 3.9 μs. It is also possible to specify a component with 1X refresh (tREFI to 7.8μs) in the Extended Temperature Range.
 - b. If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6 = 0b and MR2 A7 = 1b) or enable the optional Auto Self-Refresh mode (MR2 A6 = 1b and MR2 A7 = 0b).

AC & DC Operating Conditions

Recommended DC Operating Conditions

Recommended DC Operating Conditions

Symbol	Parameter	Rating			Unit	NOTE
		Min.	Typ.	Max.		
VDD	Supply Voltage	1.14	1.2	1.26	V	1,2,3
VDDQ	Supply Voltage for Output	1.14	1.2	1.26	V	1,2,3
VPP	Supply Voltage for DRAM Activating	2.375	2.5	2.75	V	3

NOTE:

1. Under all conditions VDDQ must be less than or equal to VDD.
2. VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.
3. DC bandwidth is limited to 20MHz.

IDD and IDDQ Specification Parameters and Test Conditions

IDD, IPP and IDDQ Measurement Conditions

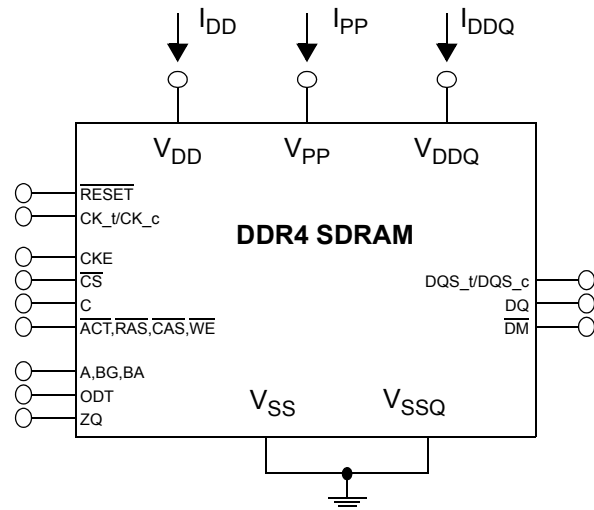
In this chapter, IDD, IPP and IDDQ measurement conditions such as test load and patterns are defined. Figure shows the setup and test load for IDD, IPP and IDDQ measurements.

- IDD currents (such as IDD0, IDD0A, IDD1, IDD1A, IDD2N, IDD2NA, IDD2NL, IDD2NT, IDD2P, IDD2Q, IDD3N, IDD3NA, IDD3P, IDD4R, IDD4RA, IDD4W, IDD4WA, IDD5B, IDD5F2, IDD5F4, IDD6N, IDD6E, IDD6R, IDD6A, IDD7 and IDD8) are measured as time-averaged currents with all VDD balls of the DDR4 SDRAM under test tied together. Any IPP or IDDQ current is not included in IDD currents.
- IPP currents have the same definition as IDD except that the current on the VPP supply is measured.
- IDDQ currents (such as IDDQ2NT and IDDQ4R) are measured as time-averaged currents with all VDDQ balls of the DDR4 SDRAM under test tied together. Any IDD current is not included in IDDQ currents.

Attention: IDDQ values cannot be directly used to calculate IO power of the DDR4 SDRAM. They can be used to support correlation of simulated IO power to actual IO power as outlined in Figure 2. In DRAM module application, IDDQ cannot be measured separately since VDD and VDDQ are using one merged-power layer in Module PCB.

For IDD, IPP and IDDQ measurements, the following definitions apply:

- "0" and "LOW" is defined as $V_{IN} \leq V_{ILAC}(\max)$.
- "1" and "HIGH" is defined as $V_{IN} \geq V_{IHAC}(\min)$.
- "MID-LEVEL" is defined as inputs are $V_{REF} = V_{DD} / 2$.
- Timings used for IDD, IPP and IDDQ Measurement-Loop Patterns are provided in Table 1.
- Basic IDD, IPP and IDDQ Measurement Conditions are described in Table 2.
- Detailed IDD, IPP and IDDQ Measurement-Loop Patterns are described in Table 3 through Table 11.
- IDD Measurements are done after properly initializing the DDR4 SDRAM. This includes but is not limited to setting
 - RON = RZQ/7 (34 Ohm in MR1);
 - RTT_NOM = RZQ/6 (40 Ohm in MR1);
 - RTT_WR = RZQ/2 (120 Ohm in MR2);
 - RTT_PARK = Disable;
 - Qoff = 0_B (Output Buffer enabled) in MR1;
 - TDQS_t disabled in MR1;
 - CRC disabled in MR2;
 - CA parity feature disabled in MR5;
 - Gear down mode disabled in MR3
 - Read/Write DBI disabled in MR5;
 - DM disabled in MR5
- Attention: The IDD, IPP and IDDQ Measurement-Loop Patterns need to be executed at least one time before actual IDD or IDDQ measurement is started.
- Define $D = \{CS_n, ACT_n, RAS_n, CAS_n, WE_n\} := \{HIGH, LOW, LOW, LOW, LOW\}$; apply BG/BA changes when directed.
- Define $D\# = \{CS_n, ACT_n, RAS_n, CAS_n, WE_n\} := \{HIGH, HIGH, HIGH, HIGH, HIGH\}$; apply invert of BG/BA changes when directed above.



NOTE:

1. DIMM level Output test load condition may be different from above

Figure 1 - Measurement Setup and Test Load for IDD, IPP and IDDQ Measurements

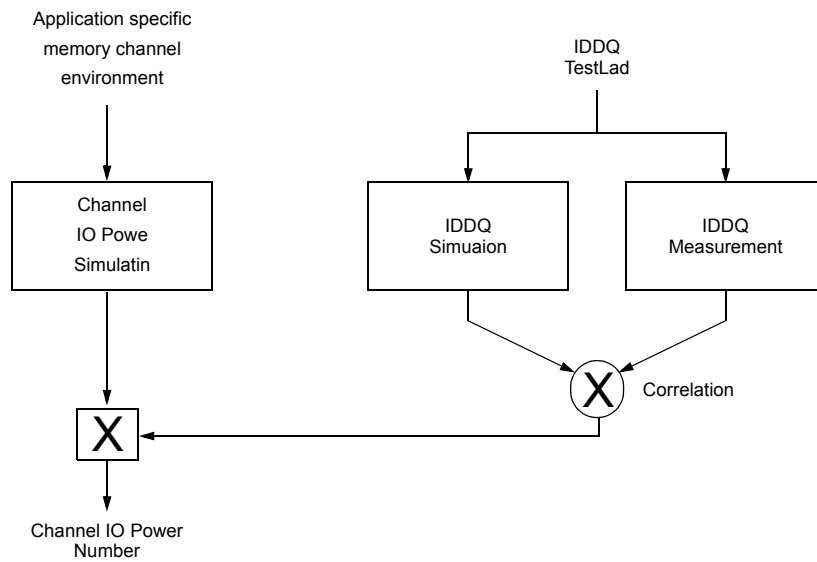


Figure 2 - Correlation from simulated Channel IO Power to actual Channel IO Power supported by IDDQ Measurement

Table 1 -Timings used for IDD, IPP and IDDQ Measurement-Loop Patterns

Symbol		DDR4-1600	DDR4-1866	DDR4-2133	DDR4-2400	DDR4-2666	Unit
		11-11-11	13-13-13	15-15-15	17-17-17	19-19-19	
tCK		1.25	1.071	0.937	0.833	0.75	ns
CL		11	13	15	17	19	nCK
CWL		11	12	14	16	18	nCK
nRCD		11	13	15	17	19	nCK
nRC		39	45	51	56	62	nCK
nRAS		28	32	36	39	43	nCK
nRP		11	13	15	17	19	nCK
nFAW	x4	16	16	16	16	16	nCK
	x8	20	22	23	26	28	nCK
	x16	28	28	32	36	40	nCK
nRRD S	x4	4	4	4	4	4	nCK
	x8	4	4	4	4	4	nCK
	x16	5	5	6	7	8	nCK
nRRD L	x4	5	5	6	6	7	nCK
	x8	5	5	6	6	7	nCK
	x16	6	6	7	8	9	nCK
tCCD_S		4	4	4	4	4	nCK
tCCD_L		5	5	6	6	7	nCK
tWTR_S		2	3	3	3	4	nCK
tWTR_L		6	7	8	9	10	nCK
nRFC 2Gb		128	150	171	193	214	nCK
nRFC 4Gb		208	243	278	313	347	nCK
nRFC 8Gb		280	327	374	421	467	nCK
nRFC 16Gb		440	514	587	661	734	nCK

Table 2 -Basic IDD, IPP and IDDQ Measurement Conditions

Symbol	Description
IDD0	Operating One Bank Active-Precharge Current (AL=0) CKE: High; External clock: On; tCK, nRC, nRAS, CL: see Table 1; BL: 8 ¹ ; AL: 0; CS_n: High between ACT and PRE; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling according to Table 3; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: Cycling with one bank active at a time: 0,0,1,1,2,2,... (see Table 3); Output Buffer and RTT: Enabled in Mode Registers ² ; ODT Signal: stable at 0; Pattern Details: see Table 3
IDD0A	Operating One Bank Active-Precharge Current (AL=CL-1) AL = CL-1, Other conditions: see IDD0
IPP0	Operating One Bank Active-Precharge IPP Current Same condition with IDD0
IDD1	Operating One Bank Active-Read-Precharge Current (AL=0) CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, CL: see Table 1; BL: 8 ¹ ; AL: 0; CS_n: High between ACT, RD and PRE; Command, Address, Bank Group Address, Bank Address Inputs, Data IO: partially toggling according to Table 4; DM_n: stable at 1; Bank Activity: Cycling with one bank active at a time: 0,0,1,1,2,2,... (see Table 4); Output Buffer and RTT: Enabled in Mode Registers ² ; ODT Signal: stable at 0; Pattern Details: see Table 4
IDD1A	Operating One Bank Active-Read-Precharge Current (AL=CL-1) AL = CL-1, Other conditions: see IDD1
IPP1	Operating One Bank Active-Read-Precharge IPP Current Same condition with IDD1
IDD2N	Precharge Standby Current (AL=0) CKE: High; External clock: On; tCK, CL: see Table 1; BL: 8 ¹ ; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling according to Table 5; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers ² ; ODT Signal: stable at 0; Pattern Details: see Table 5
IDD2NA	Precharge Standby Current (AL=CL-1) AL = CL-1, Other conditions: see IDD2N
IPP2N	Precharge Standby IPP Current Same condition with IDD2N
IDD2NT	Precharge Standby ODT Current CKE: High; External clock: On; tCK, CL: see Table 1; BL: 8 ¹ ; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling according to Table 6; Data IO: VSSQ; DM_n: stable at 1; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers ² ; ODT Signal: toggling according to Table 6; Pattern Details: see Table 6
IDDQ2NT (Optional)	Precharge Standby ODT IDDQ Current Same definition like for IDD2NT, however measuring IDDQ current instead of IDD current
IDD2NL	Precharge Standby Current with CAL enabled Same definition like for IDD2N, CAL enabled ³
IDD2NG	Precharge Standby Current with Gear Down mode enabled Same definition like for IDD2N, Gear Down mode enabled ³
IDD2ND	Precharge Standby Current with DLL disabled Same definition like for IDD2N, DLL disabled ³

IDD2N_par	Precharge Standby Current with CA parity enabled Same definition like for IDD2N, CA parity enabled ³
IDD2P	Precharge Power-Down Current CKE: Low; External clock: On; tCK, CL: see Table 1; BL: 8 ¹ ; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: stable at 0; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers ² ; ODT Signal: stable at 0
IPP2P	Precharge Power-Down IPP Current Same condition with IDD2P
IDD2Q	Precharge Quiet Standby Current CKE: High; External clock: On; tCK, CL: see Table 1; BL: 8 ¹ ; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: stable at 0; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers ² ; ODT Signal: stable at 0
IDD3N	Active Standby Current CKE: High; External clock: On; tCK, CL: see Table 1; BL: 8 ¹ ; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling according to Table 5; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers ² ; ODT Signal: stable at 0; Pattern Details: see Table 5
IDD3NA	Active Standby Current (AL=CL-1) AL = CL-1, Other conditions: see IDD3N
IPP3N	Active Standby IPP Current Same condition with IDD3N
IDD3P	Active Power-Down Current CKE: Low; External clock: On; tCK, CL: see Table 1; BL: 8 ¹ ; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: stable at 0; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers ² ; ODT Signal: stable at 0
IPP3P	Active Power-Down IPP Current Same condition with IDD3P
IDD4R	Operating Burst Read Current CKE: High; External clock: On; tCK, CL: see Table 1; BL: 8 ² ; AL: 0; CS_n: High between RD; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling according to Table 7; Data IO: seamless read data burst with different data between one burst and the next one according to Table 7; DM_n: stable at 1; Bank Activity: all banks open, RD commands cycling through banks: 0,0,1,1,2,2,... (see Table 7); Output Buffer and RTT: Enabled in Mode Registers ² ; ODT Signal: stable at 0; Pattern Details: see Table 7
IDD4RA	Operating Burst Read Current (AL=CL-1) AL = CL-1, Other conditions: see IDD4R
IDD4RB	Operating Burst Read Current with Read DBI Read DBI enabled³, Other conditions: see IDD4R
IPP4R	Operating Burst Read IPP Current Same condition with IDD4R
IDDQ4R (Optional)	Operating Burst Read IDDQ Current Same definition like for IDD4R, however measuring IDDQ current instead of IDD current
IDDQ4RB (Optional)	Operating Burst Read IDDQ Current with Read DBI Same definition like for IDD4RB, however measuring IDDQ current instead of IDD current

IDD4W	Operating Burst Write Current CKE: High; External clock: On; tCK, CL: see Table 1; BL: 8 ¹ ; AL: 0; CS_n: High between WR; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling according to Table 8; Data IO: seamless write data burst with different data between one burst and the next one according to Table 8; DM_n: stable at 1; Bank Activity: all banks open, WR commands cycling through banks: 0,0,1,1,2,2,... (see Table 8); Output Buffer and RTT: Enabled in Mode Registers ² ; ODT Signal: stable at HIGH; Pattern Details: see Table 8
IDD4WA	Operating Burst Write Current (AL=CL-1) AL = CL-1, Other conditions: see IDD4W
IDD4WB	Operating Burst Write Current with Write DBI Write DBI enabled³, Other conditions: see IDD4W
IDD4WC	Operating Burst Write Current with Write CRC Write CRC enabled³, Other conditions: see IDD4W
IDD4W_par	Operating Burst Write Current with CA Parity CA Parity enabled³, Other conditions: see IDD4W
IPP4W	Operating Burst Write IPP Current Same condition with IDD4W
IDD5B	Burst Refresh Current (1X REF) CKE: High; External clock: On; tCK, CL, nRFC: see Table 1; BL: 8 ¹ ; AL: 0; CS_n: High between REF; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling according to Table 9; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: REF command every nRFC (see Table 9); Output Buffer and RTT: Enabled in Mode Registers ² ; ODT Signal: stable at 0; Pattern Details: see Table 9
IPP5B	Burst Refresh Write IPP Current (1X REF) Same condition with IDD5B
IDD5F2	Burst Refresh Current (2X REF) tRFC=tRFC_x2, Other conditions: see IDD5B
IPP5F2	Burst Refresh Write IPP Current (2X REF) Same condition with IDD5F2
IDD5F4	Burst Refresh Current (4X REF) tRFC=tRFC_x4, Other conditions: see IDD5B
IPP5F4	Burst Refresh Write IPP Current (4X REF) Same condition with IDD5F4
IDD6N	Self Refresh Current: Normal Temperature Range T_{CASE}: 0 - 85°C; Low Power Array Self Refresh (LP ASR) : Normal ⁴ ; CKE: Low; External clock: Off; CK_t and CK_c#: LOW; CL: see Table 1; BL: 8 ¹ ; AL: 0; CS_n#, Command, Address, Bank Group Address, Bank Address, Data IO: High; DM_n: stable at 1; Bank Activity: Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers ² ; ODT Signal: MID-LEVEL
IPP6N	Self Refresh IPP Current: Normal Temperature Range Same condition with IDD6N
IDD6E	Self-Refresh Current: Extended Temperature Range⁵⁾ T_{CASE}: 0 - 95°C; Low Power Array Self Refresh (LP ASR) : Extended ⁴ ; CKE: Low; External clock: Off; CK_t and CK_c: LOW; CL: see Table 1; BL: 8 ¹ ; AL: 0; CS_n, Command, Address, Bank Group Address, Bank Address, Data IO: High; DM_n: stable at 1; Bank Activity: Extended Temperature Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers ² ; ODT Signal: MID-LEVEL
IPP6E	Self Refresh IPP Current: Extended Temperature Range Same condition with IDD6E

IDD6R	Self-Refresh Current: Reduced Temperature Range T_{CASE} : 0 - TBD (~35-45)°C; Low Power Array Self Refresh (LP ASR) : Reduced ⁴ ; CKE : Low; External clock : Off; CK_t and CK_c# : LOW; CL : see Table 1; BL : 8 ¹ ; AL : 0; CS_n# , Command , Address , Bank Group Address , Bank Address , Data IO : High; DM_n :stable at 1; Bank Activity : Extended Temperature Self-Refresh operation; Output Buffer and RTT : Enabled in Mode Registers ² ; ODT Signal : MID-LEVEL
IPP6R	Self Refresh IPP Current: Reduced Temperature Range Same condition with IDD6R
IDD6A	Auto Self-Refresh Current T_{CASE} : 0 - 95°C; Low Power Array Self Refresh (LP ASR) : Auto ⁴ ; CKE : Low; External clock : Off; CK_t and CK_c# : LOW; CL : see Table 1; BL : 8 ¹ ; AL : 0; CS_n# , Command , Address , Bank Group Address , Bank Address , Data IO : High; DM_n :stable at 1; Bank Activity : Auto Self-Refresh operation; Output Buffer and RTT : Enabled in Mode Registers ² ; ODT Signal : MID-LEVEL
IPP6A	Auto Self-Refresh IPP Current Same condition with IDD6A
IDD7	Operating Bank Interleave Read Current CKE : High; External clock : On; tCK , nRC , nRAS , nRCD , nRRD , nFAW , CL : see Table 1; BL : 8 ¹ ; AL : CL-1; CS_n : High between ACT and RDA; Command , Address , Bank Group Address , Bank Address Inputs : partially toggling according to Table 10; Data IO : read data bursts with different data between one burst and the next one according to Table 10; DM_n : stable at 1; Bank Activity : two times interleaved cycling through banks (0, 1, ...7) with different addressing, see Table 10; Output Buffer and RTT : Enabled in Mode Registers ² ; ODT Signal : stable at 0; Pattern Details : see Table 10
IPP7	Operating Bank Interleave Read IPP Current Same condition with IDD7
IDD8	Maximum Power Down Current TBD
IPP8	Maximum Power Down IPP Current Same condition with IDD8

Table 3 - IDD0, IDD0A and IPP0 Measurement-Loop Pattern¹

CK_t / CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/ A16	CAS_n/ A15	WE_n/ A14	ODT	C[2:0] ³	BG[1:0] ²	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data ⁴			
toggling	Static High	0	0	ACT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-		
			1,2	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-	
			3,4	D_#, D_#	1	1	1	1	1	1	0	0	3 ²	3	0	0	0	7	F	0	0	-	
			...	repeat pattern 1...4 until nRAS - 1, truncate if necessary																			
			nRAS	PRE	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			...	repeat pattern 1...4 until nRC - 1, truncate if necessary																			
		1	1*nRC	repeat Sub-Loop 0, use BG[1:0]² = 1, BA[1:0] = 1 instead																			
		2	2*nRC	repeat Sub-Loop 0, use BG[1:0]² = 0, BA[1:0] = 2 instead																			
		3	3*nRC	repeat Sub-Loop 0, use BG[1:0]² = 1, BA[1:0] = 3 instead																			
		4	4*nRC	repeat Sub-Loop 0, use BG[1:0]² = 0, BA[1:0] = 1 instead																			
		5	5*nRC	repeat Sub-Loop 0, use BG[1:0]² = 1, BA[1:0] = 2 instead																			
		6	6*nRC	repeat Sub-Loop 0, use BG[1:0]² = 0, BA[1:0] = 3 instead																			
		7	7*nRC	repeat Sub-Loop 0, use BG[1:0]² = 1, BA[1:0] = 0 instead																			
		8	8*nRC	repeat Sub-Loop 0, use BG[1:0]² = 2, BA[1:0] = 0 instead																			
		9	9*nRC	repeat Sub-Loop 0, use BG[1:0]² = 3, BA[1:0] = 1 instead																			
10	10*nRC	repeat Sub-Loop 0, use BG[1:0]² = 2, BA[1:0] = 2 instead																					
11	11*nRC	repeat Sub-Loop 0, use BG[1:0]² = 3, BA[1:0] = 3 instead																					
12	12*nRC	repeat Sub-Loop 0, use BG[1:0]² = 2, BA[1:0] = 1 instead																					
13	13*nRC	repeat Sub-Loop 0, use BG[1:0]² = 3, BA[1:0] = 2 instead																					
14	14*nRC	repeat Sub-Loop 0, use BG[1:0]² = 2, BA[1:0] = 3 instead																					
15	15*nRC	repeat Sub-Loop 0, use BG[1:0]² = 3, BA[1:0] = 0 instead																					

NOTE:

1. DQS_t, DQS_c are VDDQ.
2. BG1 is don't care for x16 device
3. C[2:0] are used only for 3DS device
4. DQ signals are VDDQ.

Table 4 - IDD1 Measurement-Loop Pattern^{a)}

CK_t, CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0] ³	BG[1:0] ²	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data ⁴			
toggling	Static High	0	0	ACT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-		
			1, 2	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-	
			3, 4	D#, D#	1	1	1	1	1	1	0	0	3 ^b	3	0	0	0	0	7	F	0	-	
			...	repeat pattern 1...4 until nRCD - AL - 1, truncate if necessary																			
			nRCD -AL	RD	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	D0=00, D1=FF D2=FF, D3=00 D4=FF, D5=00 D6=00, D7=FF
			...	repeat pattern 1...4 until nRAS - 1, truncate if necessary																			
			nRAS	PRE	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			...	repeat pattern 1...4 until nRC - 1, truncate if necessary																			
			1	1*nRC + 0	ACT	0	0	0	1	1	0	0	0	1	1	0	0	0	0	0	0	0	-
			1*nRC + 1, 2	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
		1*nRC + 3, 4	D#, D#	1	1	1	1	1	1	0	0	0	3 ^b	3	0	0	0	0	7	F	0	-	
		...	repeat pattern nRC + 1...4 until 1*nRC + nRAS - 1, truncate if necessary																				
		1*nRC + nRCD - AL	RD	0	1	1	0	1	0	0	0	1	1	1	0	0	0	0	0	0	0	D0=FF, D1=00 D2=00, D3=FF D4=00, D5=FF D6=FF, D7=00	
		...	repeat pattern 1...4 until nRAS - 1, truncate if necessary																				
		1*nRC + nRAS	PRE	0	1	0	1	0	0	0	0	1	1	0	0	0	0	0	0	0	0	-	
		...	repeat nRC + 1...4 until 2*nRC - 1, truncate if necessary																				
		2	2*nRC	repeat Sub-Loop 0, use BG[1:0]² = 0, BA[1:0] = 2 instead																			
		3	3*nRC	repeat Sub-Loop 1, use BG[1:0]² = 1, BA[1:0] = 3 instead																			
		4	4*nRC	repeat Sub-Loop 0, use BG[1:0]² = 0, BA[1:0] = 1 instead																			
		5	5*nRC	repeat Sub-Loop 1, use BG[1:0]² = 1, BA[1:0] = 2 instead																			
6	6*nRC	repeat Sub-Loop 0, use BG[1:0]² = 0, BA[1:0] = 3 instead																					
8	7*nRC	repeat Sub-Loop 1, use BG[1:0]² = 1, BA[1:0] = 0 instead																					
9	9*nRC	repeat Sub-Loop 1, use BG[1:0]² = 2, BA[1:0] = 0 instead																					
10	10*nRC	repeat Sub-Loop 0, use BG[1:0]² = 3, BA[1:0] = 1 instead																					
11	11*nRC	repeat Sub-Loop 1, use BG[1:0]² = 2, BA[1:0] = 2 instead																					
12	12*nRC	repeat Sub-Loop 0, use BG[1:0]² = 3, BA[1:0] = 3 instead																					
13	13*nRC	repeat Sub-Loop 1, use BG[1:0]² = 2, BA[1:0] = 1 instead																					
14	14*nRC	repeat Sub-Loop 0, use BG[1:0]² = 3, BA[1:0] = 2 instead																					
15	15*nRC	repeat Sub-Loop 1, use BG[1:0]² = 2, BA[1:0] = 3 instead																					
16	16*nRC	repeat Sub-Loop 0, use BG[1:0]² = 3, BA[1:0] = 0 instead																					

For x4 and x8 only

NOTE:

1. DQS_t, DQS_c are used according to RD Commands, otherwise VDDQ
2. BG1 is don't care for x16 device
3. C[2:0] are used only for 3DS device
4. Burst Sequence driven on each DQ signal by Read Command. Outside burst operation, DQ signals are VDDQ.

Table 5 - IDD2N, IDD2NA, IDD2NL, IDD2NG, IDD2ND, IDD2N_par, IPP2,IDD3N, IDD3NA and IDD3P

Measurement-Loop Pattern¹

CK_t, CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0] ³	BG[1:0] ²	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data ⁴		
toggling	Static High	0	0	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
			1	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
			2	D#, D#	1	1	1	1	1	1	0	0	3 ²	3	0	0	0	0	7	F	0	0
			3	D#, D#	1	1	1	1	1	1	0	0	3 ²	3	0	0	0	0	7	F	0	0
		1	4-7	repeat Sub-Loop 0, use BG[1:0]² = 1, BA[1:0] = 1 instead																		
		2	8-11	repeat Sub-Loop 0, use BG[1:0]² = 0, BA[1:0] = 2 instead																		
		3	12-15	repeat Sub-Loop 0, use BG[1:0]² = 1, BA[1:0] = 3 instead																		
		4	16-19	repeat Sub-Loop 0, use BG[1:0]² = 0, BA[1:0] = 1 instead																		
		5	20-23	repeat Sub-Loop 0, use BG[1:0]² = 1, BA[1:0] = 2 instead																		
		6	24-27	repeat Sub-Loop 0, use BG[1:0]² = 0, BA[1:0] = 3 instead																		
		7	28-31	repeat Sub-Loop 0, use BG[1:0]² = 1, BA[1:0] = 0 instead																		
		8	32-35	repeat Sub-Loop 0, use BG[1:0]² = 2, BA[1:0] = 0 instead																		
		9	36-39	repeat Sub-Loop 0, use BG[1:0]² = 3, BA[1:0] = 1 instead																		
		10	40-43	repeat Sub-Loop 0, use BG[1:0]² = 2, BA[1:0] = 2 instead																		
		11	44-47	repeat Sub-Loop 0, use BG[1:0]² = 3, BA[1:0] = 3 instead																		
		12	48-51	repeat Sub-Loop 0, use BG[1:0]² = 2, BA[1:0] = 1 instead																		
13	52-55	repeat Sub-Loop 0, use BG[1:0]² = 3, BA[1:0] = 2 instead																				
14	56-59	repeat Sub-Loop 0, use BG[1:0]² = 2, BA[1:0] = 3 instead																				
15	60-63	repeat Sub-Loop 0, use BG[1:0]² = 3, BA[1:0] = 0 instead																				

NOTE :

1. DQS_t, DQS_c are VDDQ.
2. BG1 is don't care for x16 device
3. C[2:0] are used only for 3DS device
4. DQ signals are VDDQ.

Table 6 - IDD2NT and IDDQ2NT Measurement-Loop Pattern¹

CK_t, CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0] ³	BG[1:0] ²	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data ⁴		
toggling	Static High	0	0	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-	
			1	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			2	D#, D#	1	1	1	1	1	1	0	0	3 ²	3	0	0	0	7	F	0	0	-
			3	D#, D#	1	1	1	1	1	1	0	0	3 ²	3	0	0	0	7	F	0	0	-
		1	4-7	repeat Sub-Loop 0, but ODT = 1 and BG[1:0]² = 1, BA[1:0] = 1 instead																		
		2	8-11	repeat Sub-Loop 0, but ODT = 0 and BG[1:0]² = 0, BA[1:0] = 2 instead																		
		3	12-15	repeat Sub-Loop 0, but ODT = 1 and BG[1:0]² = 1, BA[1:0] = 3 instead																		
		4	16-19	repeat Sub-Loop 0, but ODT = 0 and BG[1:0]² = 0, BA[1:0] = 1 instead																		
		5	20-23	repeat Sub-Loop 0, but ODT = 1 and BG[1:0]² = 1, BA[1:0] = 2 instead																		
		6	24-27	repeat Sub-Loop 0, but ODT = 0 and BG[1:0]² = 0, BA[1:0] = 3 instead																		
		7	28-31	repeat Sub-Loop 0, but ODT = 1 and BG[1:0]² = 1, BA[1:0] = 0 instead																		
		8	32-35	repeat Sub-Loop 0, but ODT = 0 and BG[1:0]² = 2, BA[1:0] = 0 instead																		
		9	36-39	repeat Sub-Loop 0, but ODT = 1 and BG[1:0]² = 3, BA[1:0] = 1 instead																		
		10	40-43	repeat Sub-Loop 0, but ODT = 0 and BG[1:0]² = 2, BA[1:0] = 2 instead																		
		11	44-47	repeat Sub-Loop 0, but ODT = 1 and BG[1:0]² = 3, BA[1:0] = 3 instead																		
12	48-51	repeat Sub-Loop 0, but ODT = 0 and BG[1:0]² = 2, BA[1:0] = 1 instead																				
13	52-55	repeat Sub-Loop 0, but ODT = 1 and BG[1:0]² = 3, BA[1:0] = 2 instead																				
14	56-59	repeat Sub-Loop 0, but ODT = 0 and BG[1:0]² = 2, BA[1:0] = 3 instead																				
15	60-63	repeat Sub-Loop 0, but ODT = 1 and BG[1:0]² = 3, BA[1:0] = 0 instead																				

For x4 and x8 only

NOTE :

1. DQS_t, DQS_c are VDDQ.
2. BG1 is don't care for x16 device
3. C[2:0] are used only for 3DS device
4. DQ signals are VDDQ.

Table 7 - IDD4R, IDDR4RA, IDD4RB and IDDQ4R Measurement-Loop Pattern¹

CK_t, CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0] ³	BG[1:0] ²	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data ⁴			
toggling	Static High	0	0	RD	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	D0=00, D1=FF D2=FF, D3=00 D4=FF, D5=00 D6=00, D7=FF		
			1	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-	
			2,3	D#, D#	1	1	1	1	1	1	0	0	3 ²	3	0	0	0	0	7	F	0	-	
		1	4	RD	0	1	1	0	1	0	0	0	1	1	0	0	0	0	7	F	0	D0=FF, D1=00 D2=00, D3=FF D4=00, D5=FF D6=FF, D7=00	
				5	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
				6,7	D#, D#	1	1	1	1	1	1	0	0	3 ²	3	0	0	0	0	7	F	0	-
		2	8-11	repeat Sub-Loop 0, use BG[1:0]² = 0, BA[1:0] = 2 instead																			
		3	12-15	repeat Sub-Loop 1, use BG[1:0]² = 1, BA[1:0] = 3 instead																			
		4	16-19	repeat Sub-Loop 0, use BG[1:0]² = 0, BA[1:0] = 1 instead																			
		5	20-23	repeat Sub-Loop 1, use BG[1:0]² = 1, BA[1:0] = 2 instead																			
		6	24-27	repeat Sub-Loop 0, use BG[1:0]² = 0, BA[1:0] = 3 instead																			
		7	28-31	repeat Sub-Loop 1, use BG[1:0]² = 1, BA[1:0] = 0 instead																			
		8	32-35	repeat Sub-Loop 0, use BG[1:0]² = 2, BA[1:0] = 0 instead																			
		9	36-39	repeat Sub-Loop 1, use BG[1:0]² = 3, BA[1:0] = 1 instead																			
		10	40-43	repeat Sub-Loop 0, use BG[1:0]² = 2, BA[1:0] = 2 instead																			
11	44-47	repeat Sub-Loop 1, use BG[1:0]² = 3, BA[1:0] = 3 instead																					
12	48-51	repeat Sub-Loop 0, use BG[1:0]² = 2, BA[1:0] = 1 instead																					
13	52-55	repeat Sub-Loop 1, use BG[1:0]² = 3, BA[1:0] = 2 instead																					
14	56-59	repeat Sub-Loop 0, use BG[1:0]² = 2, BA[1:0] = 3 instead																					
15	60-63	repeat Sub-Loop 1, use BG[1:0]² = 3, BA[1:0] = 0 instead																					

NOTE :

1. DQS_t, DQS_c are used according to RD Commands, otherwise VDDQ.
2. BG1 is don't care for x16 device
3. C[2:0] are used only for 3DS device
4. Burst Sequence driven on each DQ signal by Read Command.

Table 8 - IDD4W, IDD4WA, IDD4WB and IDD4W_par Measurement-Loop Pattern¹

CK_t, CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0] ³	BG[1:0] ²	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data ⁴		
toggling	Static High	0	0	WR	0	1	1	0	1	1	0	0	0	0	0	0	0	0	0	0	D0=00, D1=FF D2=FF, D3=00 D4=FF, D5=00 D6=00, D7=FF	
			1	D	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	-	
			2,3	D#, D#	1	1	1	1	1	1	0	3 ²	3	0	0	0	7	F	0	-		
		1	4	WR	0	1	1	0	1	1	0	1	1	0	0	0	7	F	0	0	0	D0=FF, D1=00 D2=00, D3=FF D4=00, D5=FF D6=FF, D7=00
				5	D	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	-	
				6,7	D#, D#	1	1	1	1	1	1	0	3 ²	3	0	0	0	7	F	0	-	
		2	8-11	repeat Sub-Loop 0, use BG[1:0]² = 0, BA[1:0] = 2 instead																		
		3	12-15	repeat Sub-Loop 1, use BG[1:0]² = 1, BA[1:0] = 3 instead																		
		4	16-19	repeat Sub-Loop 0, use BG[1:0]² = 0, BA[1:0] = 1 instead																		
		5	20-23	repeat Sub-Loop 1, use BG[1:0]² = 1, BA[1:0] = 2 instead																		
		6	24-27	repeat Sub-Loop 0, use BG[1:0]² = 0, BA[1:0] = 3 instead																		
		7	28-31	repeat Sub-Loop 1, use BG[1:0]² = 1, BA[1:0] = 0 instead																		
		8	32-35	repeat Sub-Loop 0, use BG[1:0]² = 2, BA[1:0] = 0 instead																		
		9	36-39	repeat Sub-Loop 1, use BG[1:0]² = 3, BA[1:0] = 1 instead																		
		10	40-43	repeat Sub-Loop 0, use BG[1:0]² = 2, BA[1:0] = 2 instead																		
11	44-47	repeat Sub-Loop 1, use BG[1:0]² = 3, BA[1:0] = 3 instead																				
12	48-51	repeat Sub-Loop 0, use BG[1:0]² = 2, BA[1:0] = 1 instead																				
13	52-55	repeat Sub-Loop 1, use BG[1:0]² = 3, BA[1:0] = 2 instead																				
14	56-59	repeat Sub-Loop 0, use BG[1:0]² = 2, BA[1:0] = 3 instead																				
15	60-63	repeat Sub-Loop 1, use BG[1:0]² = 3, BA[1:0] = 0 instead																				

NOTE :

1. DQS_t, DQS_c are used according to WR Commands, otherwise VDDQ.
2. BG1 is don't care for x16 device
3. C[2:0] are used only for 3DS device
4. Burst Sequence driven on each DQ signal by Write Command.

Table 9 - IDD4WC Measurement-Loop Pattern¹

CK_t, CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0] ^c	BG[1:0] ^b	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data ^d		
toggling	Static High	0	0	WR	0	1	1	0	1	1	0	0	0	0	0	0	0	0	0	0	D0=00, D1=FF D2=FF, D3=00 D4=FF, D5=00 D6=00, D7=FF D8=CRC	
		1,2	D, D	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	-	
		3,4	D#, D#	1	1	1	1	1	1	1	0	3 ²	3	0	0	0	0	7	F	0	-	
		5	WR	0	1	1	0	1	1	1	0	1	1	0	0	0	0	7	F	0	D0=FF, D1=00 D2=00, D3=FF D4=00, D5=FF D6=FF, D7=00 D8=CRC	
		6,7	D, D	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	-	
		8,9	D#, D#	1	1	1	1	1	1	1	0	3 ²	3	0	0	0	0	7	F	0	-	
		2	10-14	repeat Sub-Loop 0, use BG[1:0]² = 0, BA[1:0] = 2 instead																		
		3	15-19	repeat Sub-Loop 1, use BG[1:0]² = 1, BA[1:0] = 3 instead																		
		4	20-24	repeat Sub-Loop 0, use BG[1:0]² = 0, BA[1:0] = 1 instead																		
		5	25-29	repeat Sub-Loop 1, use BG[1:0]² = 1, BA[1:0] = 2 instead																		
		6	30-34	repeat Sub-Loop 0, use BG[1:0]² = 0, BA[1:0] = 3 instead																		
		7	35-39	repeat Sub-Loop 1, use BG[1:0]² = 1, BA[1:0] = 0 instead																		
		8	40-44	repeat Sub-Loop 0, use BG[1:0]² = 2, BA[1:0] = 0 instead																		
		9	45-49	repeat Sub-Loop 1, use BG[1:0]² = 3, BA[1:0] = 1 instead																		
		10	50-54	repeat Sub-Loop 0, use BG[1:0]² = 2, BA[1:0] = 2 instead																		
11	55-59	repeat Sub-Loop 1, use BG[1:0]² = 3, BA[1:0] = 3 instead																				
12	60-64	repeat Sub-Loop 0, use BG[1:0]² = 2, BA[1:0] = 1 instead																				
13	65-69	repeat Sub-Loop 1, use BG[1:0]² = 3, BA[1:0] = 2 instead																				
14	70-74	repeat Sub-Loop 0, use BG[1:0]² = 2, BA[1:0] = 3 instead																				
15	75-79	repeat Sub-Loop 1, use BG[1:0]² = 3, BA[1:0] = 0 instead																				

For x4 and x8 only

NOTE :

1. DQS_t, DQS_c are VDDQ.
2. BG1 is don't care for x16 device.
3. C[2:0] are used only for 3DS device.
4. Burst Sequence driven on each DQ signal by Write Command.

Table 10 - IDD5B Measurement-Loop Pattern¹

CK_t, CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0] ³	BG[1:0] ²	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data ⁴		
toggling	Static High	0	0	REF	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-		
		1	1	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-	
				2	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
				3	D#, D#	1	1	1	1	1	0	0	3 ²	3	0	0	0	7	F	0	0	-
				4	D#, D#	1	1	1	1	1	0	0	3 ²	3	0	0	0	7	F	0	0	-
				4-7	repeat pattern 1...4, use BG[1:0]² = 1, BA[1:0] = 1 instead																	
				8-11	repeat pattern 1...4, use BG[1:0]² = 0, BA[1:0] = 2 instead																	
				12-15	repeat pattern 1...4, use BG[1:0]² = 1, BA[1:0] = 3 instead																	
				16-19	repeat pattern 1...4, use BG[1:0]² = 0, BA[1:0] = 1 instead																	
				20-23	repeat pattern 1...4, use BG[1:0]² = 1, BA[1:0] = 2 instead																	
				24-27	repeat pattern 1...4, use BG[1:0]² = 0, BA[1:0] = 3 instead																	
				28-31	repeat pattern 1...4, use BG[1:0]² = 1, BA[1:0] = 0 instead																	
				32-35	repeat pattern 1...4, use BG[1:0]² = 2, BA[1:0] = 0 instead																	
				36-39	repeat pattern 1...4, use BG[1:0]² = 3, BA[1:0] = 1 instead																	
				40-43	repeat pattern 1...4, use BG[1:0]² = 2, BA[1:0] = 2 instead																	
				44-47	repeat pattern 1...4, use BG[1:0]² = 3, BA[1:0] = 3 instead																	
				48-51	repeat pattern 1...4, use BG[1:0]² = 2, BA[1:0] = 1 instead																	
				52-55	repeat pattern 1...4, use BG[1:0]² = 3, BA[1:0] = 2 instead																	
				56-59	repeat pattern 1...4, use BG[1:0]² = 2, BA[1:0] = 3 instead																	
				60-63	repeat pattern 1...4, use BG[1:0]² = 3, BA[1:0] = 0 instead																	
				2	64 ... nRFC - 1	repeat Sub-Loop 1, Truncate, if necessary																

NOTE :

1. DQS_t, DQS_c are VDDQ.
2. BG1 is don't care for x16 device.
3. C[2:0] are used only for 3DS device.
4. DQ signals are VDDQ.

Table 11 - IDD7 Measurement-Loop Pattern¹

CK_t, CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0] ³	BG[1:0] ²	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data ⁴			
toggling	Static High	0	0	ACT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-			
		1	1	RDA	0	1	1	0	1	0	0	0	0	0	0	0	1	0	0	0	D0=00, D1=FF D2=FF, D3=00 D4=FF, D5=00 D6=00, D7=FF		
			2	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-	
			3	D#	1	1	1	1	1	1	0	0	3 ²	3	0	0	0	0	7	F	0	-	
			...	repeat pattern 2...3 until nRRD - 1, if nRRD > 4. Truncate if necessary																			
			1	nRRD	ACT	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	-
			nRRD + 1	RDA	0	1	1	0	1	0	0	0	0	1	1	0	0	1	0	0	0	0	D0=FF, D1=00 D2=00, D3=FF D4=00, D5=FF D6=FF, D7=00
			...	repeat pattern 2 ... 3 until 2*nRRD - 1, if nRRD > 4. Truncate if necessary																			
			2	2*nRRD	repeat Sub-Loop 0, use BG[1:0]² = 0, BA[1:0] = 2 instead																		
			3	3*nRRD	repeat Sub-Loop 1, use BG[1:0]² = 1, BA[1:0] = 3 instead																		
			4	4*nRRD	repeat pattern 2 ... 3 until nFAW - 1, if nFAW > 4*nRRD. Truncate if necessary																		
			5	nFAW	repeat Sub-Loop 0, use BG[1:0]² = 0, BA[1:0] = 1 instead																		
			6	nFAW + nRRD	repeat Sub-Loop 1, use BG[1:0]² = 1, BA[1:0] = 2 instead																		
			7	nFAW + 2*nRRD	repeat Sub-Loop 0, use BG[1:0]² = 0, BA[1:0] = 3 instead																		
			8	nFAW + 3*nRRD	repeat Sub-Loop 1, use BG[1:0]² = 1, BA[1:0] = 0 instead																		
			9	nFAW + 4*nRRD	repeat Sub-Loop 4																		
			10	2*nFAW	repeat Sub-Loop 0, use BG[1:0]² = 2, BA[1:0] = 0 instead																		
			11	2*nFAW + nRRD	repeat Sub-Loop 1, use BG[1:0]² = 3, BA[1:0] = 1 instead																		
			12	2*nFAW + 2*nRRD	repeat Sub-Loop 0, use BG[1:0]² = 2, BA[1:0] = 2 instead																		
			13	2*nFAW + 3*nRRD	repeat Sub-Loop 1, use BG[1:0]² = 3, BA[1:0] = 3 instead																		
	14	2*nFAW + 4*nRRD	repeat Sub-Loop 4																				
	15	3*nFAW	repeat Sub-Loop 0, use BG[1:0]² = 2, BA[1:0] = 1 instead																				
	16	3*nFAW + nRRD	repeat Sub-Loop 1, use BG[1:0]² = 3, BA[1:0] = 2 instead																				
	17	3*nFAW + 2*nRRD	repeat Sub-Loop 0, use BG[1:0]² = 2, BA[1:0] = 3 instead																				
	18	3*nFAW + 3*nRRD	repeat Sub-Loop 1, use BG[1:0]² = 3, BA[1:0] = 0 instead																				
	19	3*nFAW + 4*nRRD	repeat Sub-Loop 4																				
	20	4*nFAW	repeat pattern 2 ... 3 until nRC - 1, if nRC > 4*nFAW. Truncate if necessary																				

NOTE :

1. DQS_t, DQS_c are VDDQ.
2. BG1 is don't care for x16 device.
3. C[2:0] are used only for 3DS device.
4. Burst Sequence driven on each DQ signal by Read Command. Outside burst operation, DQ signals are VDDQ

IDD Specifications

IDD and IPP values are for full operating range of voltage and temperature unless otherwise noted. IDD and IPP values are for full operating range of voltage and temperature unless otherwise noted.

I_{DD} and I_{DDQ} Specification

Symbol	2133			2400			2666			3200		Unit	NOTE
	x4	x8	x16	x4	x8	x16	x4	x8	x16	x8	x16		
I_{DD0}	30	30	39	32	32	41	34	34	42	38	43	mA	
I_{DD0A}	30	30	39	32	32	41	34	34	42	38	43	mA	
I_{DD1}	38	39	50	41	42	52	43	44	54	52	56	mA	
I_{DD1A}	39	41	52	41	43	56	43	45	57	54	59	mA	
I_{DD2N}	21	21	21	22	22	22	23	23	23	26	26	mA	
I_{DD2NA}	21	21	21	22	22	22	23	23	23	26	26	mA	
I_{DD2NT}	28	28	28	30	30	30	32	32	32	36	36	mA	
I_{DD2NL}	13	13	13	14	14	14	15	15	15	16	16	mA	
I_{DD2NG}	21	21	21	22	22	22	23	23	23	24	24	mA	
I_{DD2ND}	20	20	20	21	21	21	22	22	22	25	25	mA	
I_{DD2N_par}	23	23	23	24	24	24	25	25	25	28	28	mA	
I_{DD2P}	13	13	13	14	14	14	15	15	15	17	17	mA	
I_{DD2Q}	19	19	19	20	20	20	21	21	21	24	24	mA	
I_{DD3N}	25	25	25	26	26	26	27	27	27	30	30	mA	
I_{DD3NA}	25	25	25	26	26	26	27	27	27	30	30	mA	
I_{DD3P}	17	17	17	18	18	18	19	19	19	22	22	mA	
I_{DD4R}	82	94	129	93	105	143	100	112	155	180	180	mA	
I_{DD4RA}	85	97	134	95	107	146	104	116	161	184	184	mA	
I_{DD4RB}	90	102	131	99	111	145	109	121	158	175	175	mA	
I_{DD4W}	76	91	119	84	99	131	92	107	144	126	166	mA	
I_{DD4WA}	78	93	122	86	101	135	94	109	148	130	172	mA	
I_{DD4WB}	70	85	107	78	93	119	85	100	130	114	142	mA	
I_{DD4WC}	73	88	117	82	97	130	91	106	142	122	162	mA	
I_{DD4W_par}	89	104	132	101	116	152	110	125	166	150	192	mA	
I_{DD5B}	160	160	160	160	160	160	160	160	160	160	162	mA	
I_{DD5F2}	140	140	140	140	140	140	140	140	140	140	142	mA	
I_{DD5F4}	120	120	120	120	120	120	120	120	120	120	122	mA	
I_{DD6N}	10	10	10	10	10	10	10	10	10	10	10	mA	
I_{DD6E}^1	14	14	14	14	14	14	14	14	14	14	14	mA	
I_{DD6R}	7	7	7	7	7	7	7	7	7	7	7	mA	
I_{DD6A}	14	14	14	14	14	14	14	14	14	14	14	mA	
I_{DD7}	170	130	164	172	132	172	174	134	175	155	188	mA	
I_{DD8}	7	7	7	7	7	7	7	7	7	7	7	mA	

NOTE :

1. Users should refer to the DRAM supplier data sheet and/or the DIMM SPD to determine if DDR4 SDRAM devices support the following options or requirements referred to in this material.

I_{PP} Specification

Symbol	2133			2400			2666			3200		Unit	NOTE
	x4	x8	x16	x4	x8	x16	x4	x8	x16	x8	x16		
I_{PP0}	6	6	8	6	6	8	6	6	8	6	7	mA	
I_{PP1}	7	7	8.5	7	7	8.5	7	7	8.5	7	7.5	mA	
I_{PP2N}	1.5	1.5	1.5	1.5	1.5	1.5	1.5	1.5	1.5	1.5	1.5	mA	
I_{PP2P}	1.5	1.5	1.5	1.5	1.5	1.5	1.5	1.5	1.5	1.5	1.5	mA	
I_{PP3N}	9	9	14	9	9	14	9	9	14	12	16	mA	
I_{PP3P}	9	9	14	9	9	14	9	9	14	12	16	mA	
I_{PP4R}	11	11	18	11	11	18	11	11	18	15	22	mA	
I_{PP4W}	11	11	18	11	11	18	11	11	18	16	23	mA	
I_{PP5B}	47	47	47	47	47	47	47	47	47	47	40	mA	
I_{PP5F2}	41	41	41	41	41	41	41	41	41	41	32	mA	
I_{PP5F4}	33	33	33	33	33	33	33	33	33	33	27	mA	
I_{PP6N}	2.5	2.5	2.5	2.5	2.5	2.5	2.5	2.5	2.5	2.5	2.5	mA	
I_{PP6E}^1	3	3	3	3	3	3	3	3	3	3	3	mA	
I_{PP6R}	1.5	1.5	1.5	1.5	1.5	1.5	1.5	1.5	1.5	1.5	1.5	mA	
I_{PP6A}	3	3	3	3	3	3	3	3	3	3	3	mA	
I_{PP7}	25	19	24	25	19	24	25	21	28	21	23	mA	
I_{PP8}	1.5	1.5	1.5	1.5	1.5	1.5	1.5	1.5	1.5	1.5	1.5	mA	

NOTE :

1. Users should refer to the DRAM supplier data sheet and/or the DIMM SPD to determine if DDR4 SDRAM devices support the following options or requirements referred to in this material.

I_{DD6} Specification

Symbol	Temperature Range	2133			2400			2666			3200		Unit	NOTE
		x4	x8	x16	x4	x8	x16	x4	x8	x16	x8	x16		
I_{DD6N}	0 - 85 °C	10	10	10	10	10	10	10	10	10	10	10	mA	3,4
I_{DD6E}	0 - 95 °C	14	14	14	14	14	14	14	14	14	14	14	mA	4,5,6
I_{DD6R}	0 - 45 °C	7	7	7	7	7	7	7	7	7	7	7	mA	4,6,8
I_{DD6A}	0 - 45 °C	14	14	14	14	14	14	14	14	14	14	14	mA	4,6,7

NOTE :

- Some I_{DD} currents are higher for x16 organization due to larger page-size architecture.
- Max. values for I_{DD} currents considering worst case conditions of process, temperature and voltage.
- Applicable for MR2 settings A6=0 and A7=0.
- Supplier data sheets include a max value for I_{DD6} .
- Applicable for MR2 settings A6=0 and A7=1. I_{DD6E} is only specified for devices which support the Extended Temperature Range feature.
- Refer to the supplier data sheet for the value specification method (e.g. max, typical) for I_{DD6E} and I_{DD6A}
- Applicable for MR2 settings A6=1 and A7=0. I_{DD6A} is only specified for devices which support the Auto Self Refresh feature.
- Applicable for MR2 settings MR2 [A7:A6 = 01] : Reduced Temperature range. I_{DD6R} is verified by design and characterization, and may not be subject to production test

Input/Output Capacitance

Silicon pad I/O Capacitance

Symbol	Parameter	DDR4-1600,1866,2133		DDR4-2400,2666		DDR4-2933		DDR4-3200		Unit	NOTE
		min	max	min	max	min	max	min	max		
C _{IO}	Input/output capacitance	0.55	1.4	0.55	1.15	0.55	1.00	0.55	1.00	pF	1,2,3
C _{DIO}	Input/output capacitance delta	-0.1	0.1	-0.1	0.1	-0.1	0.1	-0.1	0.1	pF	1,2,3,11
C _{DDQS}	Input/output capacitance delta DQS _t and DQS _c	-	0.05	-	0.05	-	0.05	-	0.05	pF	1,2,3,5
C _{CK}	Input capacitance, CK _t and CK _c	0.2	0.8	0.2	0.7	0.2	0.7	0.2	0.7	pF	1,3
C _{DCK}	Input capacitance delta CK _t and CK _c	-	0.05	-	0.05	-	0.05	-	0.05	pF	1,3,4
C _I	Input capacitance (CTRL, ADD, CMD pins only)	0.2	0.8	0.2	0.7	0.2	0.6	0.2	0.55	pF	1,3,6
C _{DI_CTRL}	Input capacitance delta (All CTRL pins only)	-0.1	0.1	-0.1	0.1	-0.1	0.1	-0.1	0.1	pF	1,3,7,8
C _{DI_ADD_CMD}	Input capacitance delta (All ADD/CMD pins only)	-0.1	0.1	-0.1	0.1	-0.1	0.1	-0.1	0.1	pF	1,2,9,10
C _{ALERT}	Input/output capacitance of ALERT	0.5	1.5	0.5	1.5	0.5	1.5	0.5	1.5	pF	1,3
C _{ZQ}	Input/output capacitance of ZQ	-	2.3	-	2.3	-	2.3	-	2.3	pF	1,3,12
C _{TEN}	Input capacitance of TEN	0.2	2.3	0.2	2.3	0.2	2.3	0.2	2.3	pF	1,3,13

NOTE :

1. This parameter is not subject to production test. It is verified by design and characterization. The silicon only capacitance is validated by de-embedding the package L & C parasitic. The capacitance is measured with VDD, VDDQ, VSS, VSSQ applied with all other signal pins floating. Measurement procedure tbd.
2. DQ, DM_n, DQS_T, DQS_C, TDQS_T, TDQS_C. Although the DM, TDQS_T and TDQS_C pins have different functions, the loading matches DQ and DQS
3. This parameter applies to monolithic devices only; stacked/dual-die devices are not covered here
4. Absolute value CK_T-CK_C
5. Absolute value of CIO(DQS_T)-CIO(DQS_C)
6. CI applies to ODT, CS_n, CKE, A0-A17, BA0-BA1, BG0-BG1, RAS_n/A16, CAS_n/A15, WE_n/A14, ACT_n and PAR.
7. CDI_CTRL applies to ODT, CS_n and CKE
8. CDI_CTRL = CI(CTRL)-0.5*(CI(CLK_T)+CI(CLK_C))
9. CDI_ADD_CMD applies to, A0-A17, BA0-BA1, BG0-BG1, RAS_n/A16, CAS_n/A15, WE_n/A14, ACT_n and PAR.
10. CDI_ADD_CMD = CI(ADD_CMD)-0.5*(CI(CLK_T)+CI(CLK_C))
11. CDIO = CIO(DQ,DM)-0.5*(CIO(DQS_T)+CIO(DQS_C))
12. Maximum external load capacitance on ZQ pin: tbd pF.
13. TEN pis may be DRAM internally pulled low through a weak pull-down resistor to VSS. In this case C_{TEN} might not be valid and system shall verify TEN signal with Vendor specific information.

DRAM package electrical specifications (x4/x8)

Symbol	Parameter	DDR4-1600,1866,2133,2400,2666		DDR4-2933		DDR4-3200		Unit	NOTE
		min	max	min	max	min	max		
Z _{IO}	Input/output Zpkg	45	85	48	85	48	85	Ω	1,2,4,5,10,11
T _{DIO}	Input/output Pkg Delay	14	42	14	40	14	40	ps	1,3,4,5,11
L _{IO}	Input/output Lpkg	-	3.3	-	3.3	-	3.3	nH	11,12
C _{IO}	Input/output Cpkg	-	0.78	-	0.78	-	0.78	pF	11,13
Z _{IO DQS}	DQS_t, DQS_c Zpkg	45	85	48	85	48	85	Ω	1,2,5,10,11
T _{dIO DQS}	DQS_t, DQS_c Pkg Delay	14	42	14	40	14	40	ps	1,3,5,10,11
L _{IO DQS}	DQS Lpkg	-	3.3	-	3.3	-	3.3	nH	11,12
C _{IO DQS}	DQS Cpkg	-	0.78	-	0.78	-	0.78	pF	11,13
DZ _{DIO DQS}	Delta Zpkg DQS_t, DQS_c	-	10	-	10	-	10	Ω	1,2,5,7,10
D _{TdDIO DQS}	Delta Delay DQS_t, DQS_c	-	5	-	5	-	5	ps	1,3,5,7,10
Z _{I CTRL}	Input- CTRL pins Zpkg	50	90	50	90	50	90	Ω	1,2,5,9,10,11
T _{dI CTRL}	Input- CTRL pins Pkg Delay	14	42	14	40	14	40	ps	1,3,5,9,10,11
L _{I CTRL}	Input CTRL Lpkg	-	3.4	-	3.4	-	3.4	nH	11,12
C _{I CTRL}	Input CTRL Cpkg	-	0.7	-	0.7	-	0.7	pF	11,13
Z _{IADD CMD}	Input- CMD ADD pins Zpkg	50	90	50	90	50	90	Ω	1,2,5,8,10,11
T _{dIADD CMD}	Input- CMD ADD pins Pkg Delay	14	45	14	40	14	40	ps	1,3,5,8,10,11
L _{I ADD CMD}	Input CMD ADD Lpkg	-	3.6	-	3.6	-	3.6	nH	11,12
C _{I ADD CMD}	Input CMD ADD Cpkg	-	0.74	-	0.74	-	0.74	pF	11,13
Z _{CK}	CLK_t & CLK_c Zpkg	50	90	50	90	50	90	Ω	1,2,5,10,11
T _{dCK}	CLK_t & CLK_c Pkg Delay	14	42	14	42	14	42	ps	1,3,5,10,11
L _{I CLK}	Input CLK Lpkg	-	3.4	-	3.4	-	3.4	nH	11,12
C _{I CLK}	Input CLK Cpkg	-	0.7	-	0.7	-	0.7	pF	11,13
DZ _{DLK}	Delta Zpkg CLK_t & CLK_c	-	10	-	10	-	10	Ω	1,2,5,6,10
D _{TdDLK}	Delta Delay CLK_t & CLK_c	-	5	-	5	-	5	ps	1,3,5,6,10
Z _{O ZQ}	ZQ Zpkg	-	100	-	100	-	100	Ω	1,2,5,10,11
T _{dO ZQ}	ZQ Delay	20	90	20	90	20	90	ps	1,3,5,10,11
Z _{O ALERT}	ALERT Zpkg	40	100	40	100	40	100	Ω	1,2,5,10,11
T _{dO ALERT}	ALERT Delay	20	55	20	55	20	55	ps	1,3,5,10,11

NOTE :

1. This parameter is not subject to production test. It is verified by design and characterization. The package parasitic(L & C) are validated using package only samples. The capacitance is measured with VDD, VDDQ, VSS, VSSQ shorted with all other signal pins floating. The inductance is measured with VDD, VDDQ, VSS and VSSQ shorted and all other signal pins shorted at the die side(not pin). Measurement procedure tbd
2. Package only impedance (Zpkg) is calculated based on the Lpkg and Cpkg total for a given pin where:

$$Z_{pkg}(\text{total per pin}) = \sqrt{L_{pkg}/C_{pkg}}$$

3. Package only delay(Tpkg) is calculated based on Lpkg and Cpkg total for a given pin where:

$$T_{d/pkg}(\text{total per pin}) = \sqrt{L_{pkg} * C_{pkg}}$$

4. Z & Td IO applies to DQ, DM, TDQS_T and TDQS_C
5. This parameter applies to monolithic devices only; stacked/dual-die devices are not covered here
6. Absolute value of ZCK_t-ZCK_c for impedance(Z) or absolute value of TdCK_t-TdCK_c for delay(Td).
7. Absolute value of ZIO(DQS_t)-ZIO(DQS_c) for impedance(Z) or absolute value of TdIO(DQS_t)-TdIO(DQS_c) for delay(Td)
8. ZI & Td ADD CMD applies to A0-A13, ACT_n, BA0-BA1, BG0-BG1, RAS_n/A16, CAS_n/A15, WE_n/A14 and PAR.
9. ZI & Td CTRL applies to ODT, CS_n and CKE
10. This table applies to monolithic X4 and X8 devices.
11. Package implementations shall meet spec if the Zpkg and Pkg Delay fall within the ranges shown, and the maximum Lpkg and Cpkg do not exceed the maximum values shown.
12. It is assumed that Lpkg can be approximated as $L_{pkg} = Z_o * T_d$.
13. It is assumed that Cpkg can be approximated as $C_{pkg} = T_d / Z_o$.

DRAM package electrical specifications (x16)

Symbol	Parameter	DDR4-1600,1866,2133,2400,2666,2933,3200		Unit	NOTE
		min	max		
Z _{IO}	Input/output Zpkg	45	85	Ω	1
T _{DIO}	Input/output Pkg Delay	14	45	ps	1
L _{IO}	Input/output Lpkg	-	3.4	nH	1,2
C _{IO}	Input/output Cpkg	-	0.82	pF	1,3
Z _{IO DQS}	DQS_t, DQS_c Zpkg	45	85	Ω	1
T _{dIO DQS}	DQS_t, DQS_c Pkg Delay	14	45	ps	1
L _{IO DQS}	DQS Lpkg	-	3.4	nH	1,2
C _{IO DQS}	DQS Cpkg	-	0.82	pF	1,3
DZ _{DIO DQS}	Delta Zpkg DQSU_t, DQSU_c	-	10	Ω	-
	Delta Zpkg DQSL_t, DQSL_c	-	10	Ω	-
D _{TdDIO DQS}	Delta Delay DQSU_t, DQSU_c	-	5	ps	-
	Delta Delay DQSL_t, DQSL_c	-	5	ps	-
Z _{I CTRL}	Input- CTRL pins Zpkg	50	90	Ω	1
T _{dI CTRL}	Input- CTRL pins Pkg Delay	14	42	ps	1
L _{I CTRL}	Input CTRL Lpkg	-	3.4	nH	1,2
C _{I CTRL}	Input CTRL Cpkg	-	0.7	pF	1,3
Z _{I ADD CMD}	Input- CMD ADD pins Zpkg	50	90	Ω	1
T _{dI ADD CMD}	Input- CMD ADD pins Pkg Delay	14	52	ps	1
L _{I ADD CMD}	Input CMD ADD Lpkg	-	3.9	nH	1,2
C _{I ADD CMD}	Input CMD ADD Cpkg	-	0.86	pF	1,3
Z _{CK}	CLK_t & CLK_c Zpkg	50	90	Ω	1
T _{dCK}	CLK_t & CLK_c Pkg Delay	14	42	ps	1
L _{I CLK}	Input CLK Lpkg	-	3.4	nH	1,2
C _{I CLK}	Input CLK Cpkg	-	0.7	pF	1,3
DZ _{DLK}	Delta Zpkg CLK_t & CLK_c	-	10	Ω	-
D _{TdLK}	Delta Delay CLK_t & CLK_c	-	5	ps	-
Z _{O ZQ}	ZQ Zpkg	-	100	Ω	-
T _{dO ZQ}	ZQ Delay	20	90	ps	-
Z _{O ALERT}	ALERT Zpkg	40	100	Ω	-
T _{dO ALERT}	ALERT Delay	20	55	ps	-

NOTE :

1. Package implementations shall meet spec if the Zpkg and Pkg Delay fall within the ranges shown, and the maximum Lpkg and Cpkg do not exceed the maximum values shown.
2. It is assumed that Lpkg can be approximated as $L_{pkg} = Z_o * T_d$.
3. It is assumed that Cpkg can be approximated as $C_{pkg} = T_d / Z_o$.

Standard Speed Bins

DDR4-1600 Speed Bins and Operations

Speed Bin			DDR4-1600K		Unit	NOTE	
CL-nRCD-nRP			11-11-11				
Parameter	Symbol		min	max			
Internal read command to first data	tAA		13.75 ¹⁴ (13.50) ^{5,12}	18.00	ns	12	
Internal read command to first data with read DBI enabled	tAA_DBI		tAA(min) + 2nCK	tAA(max) + 2nCK	ns	12	
ACT to internal read or write delay time	tRCD		13.75 (13.50) ^{5,12}	-	ns	12	
PRE command period	tRP		13.75 (13.50) ^{5,12}	-	ns	12	
ACT to PRE command period	tRAS		35	9 x tREFI	ns	12	
ACT to ACT or REF command period	tRC		48.75 (48.50) ^{5,12}	-	ns	12	
	Normal	Read DBI					
CWL = 9	CL = 9	CL = 11 (Optional) 5	tCK(AVG)	1.5	1.6	ns	1,2,3,4, 11,14
	CL = 10	CL = 12	tCK(AVG)	Reserved		ns	1,2,3,4, 11
CWL = 9,11	CL = 10	CL = 12	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 11	CL = 13	tCK(AVG)	1.25	<1.5	ns	1,2,3,4
	CL = 12	CL = 14	tCK(AVG)	1.25	<1.5	ns	1,2,3
Supported CL Settings				(9),11,12		nCK	13,14
Supported CL Settings with read DBI				(11),13,14		nCK	13
Supported CWL Settings				9,11		nCK	

DDR4-1866 Speed Bins and Operations

Speed Bin			DDR4-1866M		Unit	NOTE	
CL-nRCD-nRP			13-13-13				
Parameter	Symbol		min	max			
Internal read command to first data	tAA		13.92 ¹⁴ (13.50) ^{5,12}	18.00	ns	12	
Internal read command to first data with read DBI enabled	tAA_DBI		tAA(min) + 2nCK	tAA(max) + 2nCK	ns	12	
ACT to internal read or write delay time	tRCD		13.92 (13.50) ^{5,12}	-	ns	12	
PRE command period	tRP		13.92 (13.50) ^{5,12}	-	ns	12	
ACT to PRE command period	tRAS		34	9 x tREFI	ns	12	
ACT to ACT or REF command period	tRC		47.92 (47.50) ^{5,12}	-	ns	12	
	Normal	Read DBI					
CWL = 9	CL = 9	CL = 11 (Optional) ⁵	tCK(AVG)	1.5	1.6	ns	1,2,3,4, 11,14
	CL = 10	CL = 12	tCK(AVG)	Reserved		ns	1,2,3,4, 11
CWL = 9,11	CL = 10	CL = 12	tCK(AVG)	Reserved		ns	4
	CL = 11	CL = 13	tCK(AVG)	1.25	<1.5	ns	1,2,3,4, 6
	CL = 12	CL = 14	tCK(AVG)	1.25	<1.5	ns	1,2,3,6
CWL = 10,12	CL = 12	CL = 14	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 13	CL = 15	tCK(AVG)	1.071	<1.25	ns	1,2,3,4
	CL = 14	CL = 16	tCK(AVG)	1.071	<1.25	ns	1,2,3
Supported CL Settings			9,11,12,13,14		nCK	13,14	
Supported CL Settings with read DBI			11,13,14 15,16		nCK	13	
Supported CWL Settings			9,10,11,12		nCK		

DDR4-2133 Speed Bins and Operations

Speed Bin			DDR4-2133P		Unit	NOTE
CL-nRCD-nRP			15-15-15			
Parameter	Symbol		min	max		
Internal read command to first data	tAA		14.06 ¹⁴ (13.50) ^{5,12}	18.00	ns	12
Internal read command to first data with read DBI enabled	tAA_DBI		tAA(min) + 3nCK	tAA(max) + 3nCK	ns	12
ACT to internal read or write delay time	tRCD		14.06 (13.50) ^{5,12}	-	ns	12
PRE command period	tRP		14.06 (13.50) ^{5,12}	-	ns	12
ACT to PRE command period	tRAS		33	9 x tREFI	ns	12
ACT to ACT or REF command period	tRC		47.06 (46.50) ^{5,12}	-	ns	12
	Normal	Read DBI				
CWL = 9	CL = 9	CL = 11	tCK(AVG)	1.5	1.6	ns 1,2,3,4, 11,14
	CL = 10	CL = 12	tCK(AVG)	Reserved		ns 1,2,3,11
CWL = 9,11	CL = 11	CL = 13	tCK(AVG)	1.25	<1.5	ns 1,2,3,4, 7
	CL = 12	CL = 14	tCK(AVG)	1.25	<1.5	ns 1,2,3,7
CWL = 10,12	CL = 13	CL = 15	tCK(AVG)	1.071	<1.25	ns 1,2,3,4, 7
	CL = 14	CL = 16	tCK(AVG)	1.071	<1.25	ns 1,2,3,7
CWL = 11,14	CL = 14	CL = 17	tCK(AVG)	Reserved		ns 1,2,3,4
	CL = 15	CL = 18	tCK(AVG)	0.937	<1.071	ns 1,2,3,4
	CL = 16	CL = 19	tCK(AVG)	0.937	<1.071	ns 1,2,3
Supported CL Settings			(9),(11),12,(13),14,15,16		nCK	13,14
Supported CL Settings with read DBI			(11),(13),14,(15),16,18,19		nCK	
Supported CWL Settings			9,10,11,12,14		ns	12

DDR4-2400 Speed Bins and Operations

Speed Bin			DDR4-2400T		Unit	NOTE	
CL-nRCD-nRP			17-17-17				
Parameter	Symbol		min	max			
Internal read command to first data	tAA		14.16 (13.75) ^{5,12}	18.00	ns	12	
Internal read command to first data with read DBI enabled	tAA_DBI		tAA(min) + 3nCK	tAA(max) + 3nCK	ns	12	
ACT to internal read or write delay time	tRCD		14.16 (13.75) ^{5,12}	-	ns	12	
PRE command period	tRP		14.16 (13.75) ^{5,12}	-	ns	12	
ACT to PRE command period	tRAS		32	9 x tREFI	ns	12	
ACT to ACT or REF command period	tRC		46.16 (45.75) ^{5,12}	-	ns	12	
	Normal	Read DBI					
CWL = 9	CL = 9	CL = 11 (Optional) ⁵	tCK(AVG)	Reserved		ns	1,2,3,4,11
	CL = 10	CL = 12		1.5	1.6	ns	1,2,3,4,11
CWL = 9,11	CL = 10	CL = 12	tCK(AVG)	Reserved		ns	4
	CL = 11	CL = 13	tCK(AVG)	1.25	<1.5	ns	1,2,3,4,8
	CL = 12	CL = 14	tCK(AVG)	1.25	<1.5	ns	1,2,3,8
CWL = 10,12	CL = 12	CL = 14	tCK(AVG)	Reserved		ns	4
	CL = 13	CL = 15	tCK(AVG)	1.071	<1.25	ns	1,2,3,4,8
	CL = 14	CL = 16	tCK(AVG)	1.071	<1.25	ns	1,2,3,8
CWL = 11,14	CL = 14	CL = 17	tCK(AVG)	Reserved		ns	4
	CL = 15	CL = 18	tCK(AVG)	0.937	<1.071	ns	1,2,3,4,8
	CL = 16	CL = 19	tCK(AVG)	0.937	<1.071	ns	1,2,3,8
CWL = 12,16	CL = 15	CL = 18	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 16	CL = 19	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 17	CL = 20	tCK(AVG)	0.833	<0.937		
	CL = 18	CL = 21	tCK(AVG)	0.833	<0.937	ns	1,2,3
Supported CL Settings			10,11,12,13,14,15,16,17,18		nCK	13	
Supported CL Settings with read DBI			12,13,14,15,16,18,19,20,21		nCK		
Supported CWL Settings			9,10,11,12,14,16		nCK		

DDR4-2666 Speed Bins and Operations

Speed Bin			DDR4-2666V		Unit	NOTE	
CL-nRCD-nRP			19-19-19				
Parameter	Symbol		min	max			
Internal read command to first data	tAA		14.25 ¹⁴ (13.75) ^{5,12}	18.00	ns	12	
Internal read command to first data with read DBI enabled	tAA_DBI		tAA(min) + 3nCK	tAA(max) + 3nCK	ns	12	
ACT to internal read or write delay time	tRCD		14.25 (13.75) ^{5,12}	-	ns	12	
PRE command period	tRP		14.25 (13.75) ^{5,12}	-	ns	12	
ACT to PRE command period	tRAS		32	9 x tREFI	ns	12	
ACT to ACT or REF command period	tRC		46.25 (45.75) ^{5,12}	-	ns	12	
	Normal	Read DBI					
CWL = 9	CL = 9	CL = 11	tCK(AVG)	Reserved	ns	1,2,3,4,11	
	CL = 10	CL = 12	tCK(AVG)	1.5	1.6	ns	1,2,3,11
CWL = 9,11	CL = 10	CL = 12	tCK(AVG)	Reserved	ns	4	
	CL = 11	CL = 13	tCK(AVG)	1.25	<1.5	ns	1,2,3,4,9
	CL = 12	CL = 14	tCK(AVG)	1.25	<1.5	ns	1,2,3,9
CWL = 10,12	CL = 12	CL = 14	tCK(AVG)	Reserved	ns	4	
	CL = 13	CL = 15	tCK(AVG)	1.071	<1.25	ns	1,2,3,4,9
	CL = 14	CL = 16	tCK(AVG)	1.071	<1.25	ns	1,2,3,9
CWL = 11,14	CL = 14	CL = 17	tCK(AVG)	Reserved	ns	4	
	CL = 15	CL = 18	tCK(AVG)	0.937	<1.071	ns	1,2,3,4,9
	CL = 16	CL = 19	tCK(AVG)	0.937	<1.071	ns	1,2,3,9
CWL = 12,16	CL = 15	CL = 18	tCK(AVG)	Reserved	ns	4	
	CL = 16	CL = 19	tCK(AVG)	Reserved	ns	1,2,3,4,9	
	CL = 17	CL = 20	tCK(AVG)	0.833	<0.937	ns	1,2,3,4,9
	CL = 18	CL = 21	tCK(AVG)	0.833	<0.937	ns	1,2,3
CWL = 14,18	CL = 17	CL = 20	tCK(AVG)	Reserved	ns	1,2,3,4	
	CL = 18	CL = 21	tCK(AVG)	Reserved	ns	1,2,3,4	
	CL = 19	CL = 22	tCK(AVG)	0.75	<0.833	ns	1,2,3,4
	CL = 20	CL = 23	tCK(AVG)	0.75	<0.833	ns	1,2,3
Supported CL Settings			10,(11),12,(13),14,(15),16,(17),18,19,20		nCK	13	
Supported CL Settings with read DBI			12,(13),14,(15),17,(18),19,(20),21,22,23		nCK		
Supported CWL Settings			9,10,11,12,14,16,18		nCK		

DDR4-2933 Speed Bins and Operations

Speed Bin			DDR4-2933Y		Unit	NOTE	
CL-nRCD-nRP			21-21-21				
Parameter	Symbol		min	max			
Internal read command to first data	tAA		14.32 ¹⁴ (13.75) ^{5,12}	18.00	ns	12	
Internal read command to first data with read DBI enabled	tAA_DBI		tAA(min) + 4nCK	tAA(max) + 4nCK	ns	12	
ACT to internal read or write delay time	tRCD		14.32 (13.75) ^{5,12}	-	ns	12	
PRE command period	tRP		14.32 (13.75) ^{5,12}	-	ns	12	
ACT to PRE command period	tRAS		32	9 x tREFI	ns	12	
ACT to ACT or REF command period	tRC		46.32 (45.75) ^{5,12}	-	ns	12	
	Normal	Read DBI					
CWL = 9	CL = 9	CL = 11	tCK(AVG)	Reserved		ns	1,2,3,4,11
	CL = 10	CL = 12	tCK(AVG)	1.5	1.6	ns	1,2,3,11
CWL = 9,11	CL = 10	CL = 12	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 11	CL = 13	tCK(AVG)	1.25	<1.5	ns	1,2,3,4,13
	CL = 12	CL = 14	tCK(AVG)	1.25	<1.5	ns	1,2,3,15
CWL = 10,12	CL = 12	CL = 14	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 13	CL = 15	tCK(AVG)	1.071	<1.25	ns	1,2,3,4,15
	CL = 14	CL = 16	tCK(AVG)	1.071	<1.25	ns	1,2,3,15
CWL = 11,14	CL = 14	CL = 17	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 15	CL = 18	tCK(AVG)	0.937	<1.071	ns	1,2,3,4,15
	CL = 16	CL = 19	tCK(AVG)	0.937	<1.071	ns	1,2,3,15
CWL = 12,16	CL = 15	CL = 18	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 16	CL = 19	tCK(AVG)	Reserved		ns	1,2,3,4,15
	CL = 17	CL = 20	tCK(AVG)	0.833	0.937	ns	1,2,3,4,15
	CL = 18	CL = 21	tCK(AVG)	0.833	0.937	ns	1,2,3,15
CWL = 14,18	CL = 17	CL = 20	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 18	CL = 21	tCK(AVG)	Reserved		ns	1,2,3,4,15
	CL = 19	CL = 22	tCK(AVG)	0.75	<0.833	ns	1,2,3,4,15
	CL = 20	CL = 23	tCK(AVG)	0.75	<0.833	ns	1,2,3,15
CWL = 16,20	CL = 19	CL = 23	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 20	CL = 24	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 21	CL = 26	tCK(AVG)	0.682	<0.75	ns	1,2,3,4
	CL = 22	CL = 26	tCK(AVG)	0.682	<0.75	ns	1,2,3
Supported CL Settings			10,(11),12,(13),14,(15),16,(17),18,(19),20,21,22		nCK	13	
Supported CL Settings with read DBI			12,(13),14,(15),16,(18),19,(20),21,(22),23,25,26		nCK	13	
Supported CWL Settings			9,10,11,12,14,15,16,18,20		nCK		

DDR4-3200 Speed Bins and Operations

Speed Bin			DDR4-3200AA		Unit	NOTE	
CL-nRCD-nRP			22-22-22				
Parameter	Symbol		min	max			
Internal read command to first data	tAA		13.75	18.00	ns	12	
Internal read command to first data with read DBI enabled	tAA_DBI		tAA(min) + 4nCK	tAA(max) + 4nCK	ns	12	
ACT to internal read or write delay time	tRCD		13.75	-	ns	12	
PRE command period	tRP		13.75	-	ns	12	
ACT to PRE command period	tRAS		32	9 x tREFI	ns	12	
ACT to ACT or REF command period	tRC		45.75	-	ns	12	
	Normal	Read DBI					
CWL = 9	CL = 9	CL = 11	tCK(AVG)	Reserved	ns	1,2,3,4,11	
	CL = 10	CL = 12	tCK(AVG)	Reserved	ns	1,2,3,4,11	
CWL = 9,11	CL = 10	CL = 12	tCK(AVG)	Reserved	ns	1,2,3,4	
	CL = 11	CL = 13	tCK(AVG)	1.25	<1.5	ns	1,2,3,4,10
	CL = 12	CL = 14	tCK(AVG)	1.25	<1.5	ns	1,2,3,10
CWL = 10,12	CL = 12	CL = 14	tCK(AVG)	Reserved	ns	1,2,3,4	
	CL = 13	CL = 15	tCK(AVG)	1.071	<1.25	ns	1,2,3,4,10
	CL = 14	CL = 16	tCK(AVG)	1.071	<1.25	ns	1,2,3,10
CWL = 11,14	CL = 14	CL = 17	tCK(AVG)	Reserved	ns	1,2,3,4	
	CL = 15	CL = 18	tCK(AVG)	0.937	<1.071	ns	1,2,3,4,10
	CL = 16	CL = 19	tCK(AVG)	0.937	<1.071	ns	1,2,3,10
CWL = 12,16	CL = 15	CL = 18	tCK(AVG)	Reserved	ns	1,2,3,4	
	CL = 16	CL = 19	tCK(AVG)	Reserved	ns	1,2,3,4,10	
	CL = 17	CL = 20	tCK(AVG)	0.833	<0.937	ns	1,2,3,4,10
	CL = 18	CL = 21	tCK(AVG)	0.833	<0.937	ns	1,2,3,10
CWL = 14,18	CL = 17	CL = 20	tCK(AVG)	Reserved	ns	1,2,3,4	
	CL = 18	CL = 21	tCK(AVG)	Reserved	ns	1,2,3,4,10	
	CL = 19	CL = 22	tCK(AVG)	0.75	<0.833	ns	1,2,3,4,10
	CL = 20	CL = 23	tCK(AVG)	0.75	<0.833	ns	1,2,3,10
CWL = 16,20	CL = 20	CL = 24	tCK(AVG)	Reserved	ns	1,2,3,4	
	CL = 22	CL = 26	tCK(AVG)	0.625	<0.75	ns	1,2,3,4
	CL = 24	CL = 28	tCK(AVG)	0.625	<0.75	ns	1,2,3
Supported CL Settings			10,11,12,13,14,15, 16,17,18,19,20,22, 24		nCK	13	
Supported CL Settings with read DBI			12,13,14,15,16,18, 19,20,21,22,23,24, 26, 28		nCK		
Supported CWL Settings			9,10,11,12,14,16, 18,20		nCK		

Speed Bin Table Note

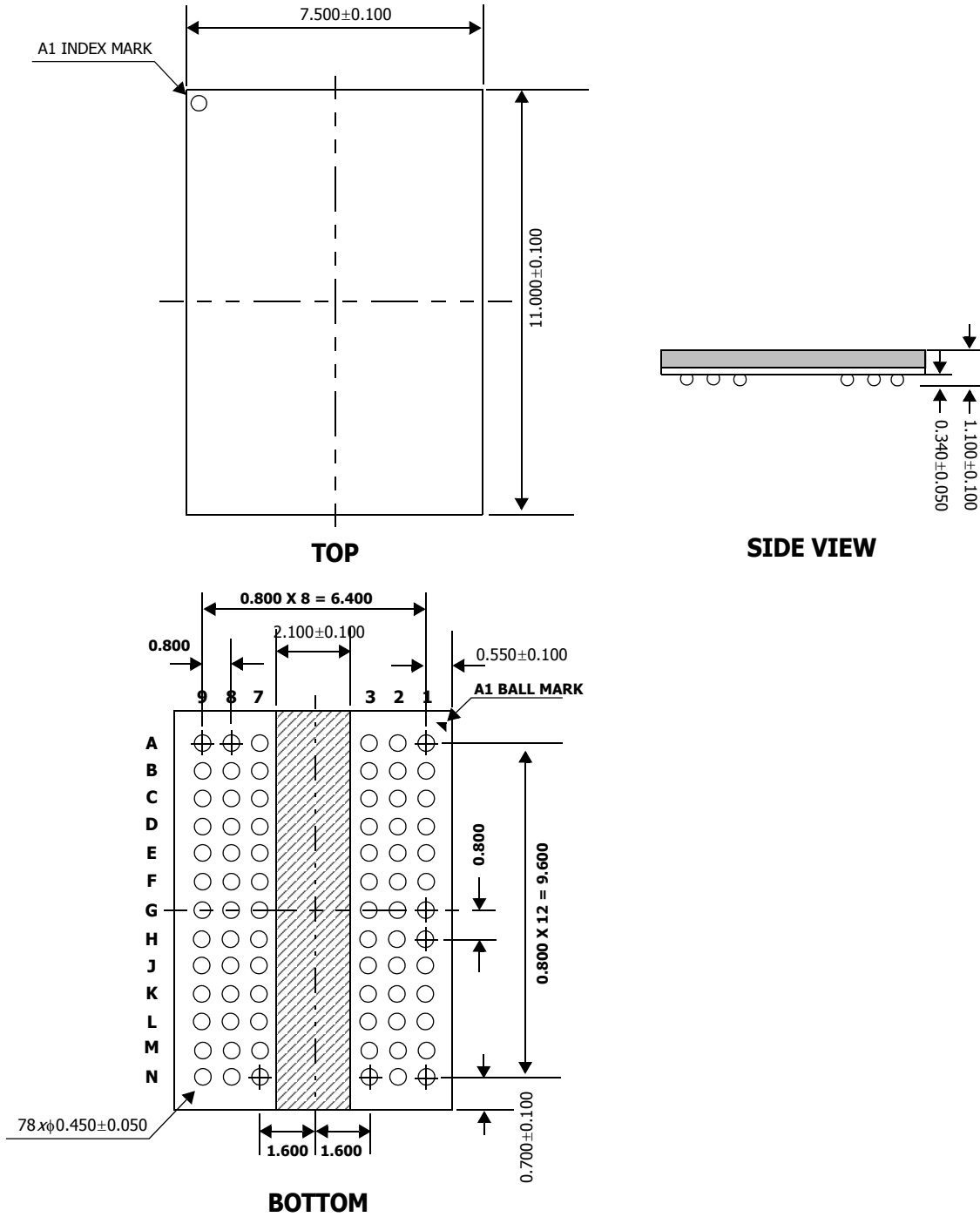
Absolute Specification

- VDDQ = VDD = 1.20V +/- 0.06 V
- VPP = 2.5V +0.25/-0.125 V
- The values defined with above-mentioned table are DLL ON case.
- DDR4-1600, 1866, 2133, 2400, 2933 and 3200 Speed Bin Tables are valid only when Geardown Mode is disabled.

1. The CL setting and CWL setting result in tCK(avg).MIN and tCK(avg).MAX requirements. When making a selection of tCK(avg), both need to be fulfilled: Requirements from CL setting as well as requirements from CWL setting.
2. tCK(avg).MIN limits: Since CAS Latency is not purely analog - data and strobe output are synchronized by the DLL - all possible intermediate frequencies may not be guaranteed. CL in clock cycle is calculated from tAA following rounding algorithm defined in Section 13.5.
3. tCK(avg).MAX limits: Calculate $tCK(avg) = tAA.MAX / CL\ SELECTED$ and round the resulting tCK(avg) down to the next valid speed bin (i.e. 1.5ns or 1.25ns or 1.071 ns or 0.937 ns or 0.833 ns). This result is tCK(avg).MAX corresponding to CL SELECTED.
4. 'Reserved' settings are not allowed. User must program a different value.
5. 'Optional' settings allow certain devices in the industry to support this setting, however, it is not a mandatory feature. Refer to supplier's data sheet and/or the DIMM SPD information if and how this setting is supported.
6. Any DDR4-1866 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
7. Any DDR4-2133 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
8. Any DDR4-2400 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
9. Any DDR4-2666 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
10. Any DDR4-3200 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
11. DDR4-1600 AC timing apply if DRAM operates at lower than 1600 MT/s data rate.
12. Parameters apply from tCK(avg)min to tCK(avg)max at all standard JEDEC clock period values as stated in the Speed Bin Tables.
13. CL number in parentheses, it means that these numbers are optional.
14. DDR4 SDRAM supports CL=9 as long as a system meets tAA(min).
15. Each speed bin lists the timing requirements that need to be supported in order for a given DRAM to be JEDEC compliant. JEDEC compliance does not require support for all speed bins within a given speed. JEDEC compliance requires meeting the parameters for a least one of the listed speed bins.

Package Dimensions

Package Dimension(x8): 78Ball Fine Pitch Ball Grid Array Outline



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