

DATA SHEET

SE5012T: 5 GHz Front-End Module with Power Detector

Applications

- 5 GHz WLAN (IEEE 802.11a/g/n)
- Access points, PCMCIA, PC cards

Features

- 5 GHz front-end module with PA, LNA, and T/R switch
- Integrated power amplifier enable pin (VEN)
- · Buffered, temperature-compensated power detector
- 5 V or direct-to-battery operation
- 3% EVM, 64 QAM, 54 Mbps: +17 dBm @ 3.3 V or +21 dBm @ 5 V
- 30 dB typical gain
- Lead free, halogen-free, ROHS compliant QFN (16-pin, 3 mm × 3 mm × 0.55 mm) package (MSL1, 260 °C per JEDEC J-STD-020)



Skyworks GreenTM products are compliant with all applicable legislation and are halogen-free. For additional information, refer to *Skyworks Definition of Green*TM, document number SQ04–0074.

Description

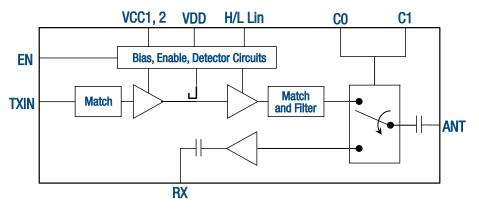
The SE5012T is a 5 GHz front-end module offering high linear power for wireless LAN applications. It incorporates a power detector for control of the output power.

The SE5012T offers a high level of integration for a simplified design, providing quicker time to market and higher application board production yield. The device integrates the input match, inter-stage match, a temperature-compensated, load-insensitive power detector with 20 dB of dynamic range, a 3.8 GHz notch filter, a T/R switch, and LNA.

For wireless LAN applications, the device meets the requirements of IEEE 802.11a and delivers approximately +17 dBm of linear output power at Vcc = 3.3 V or 21 dBm at Vcc = 5.0 V.

The SE5012T integrates the reference voltage generator, allowing for a true 1.8 V CMOS compatible digital EN (enable) function to turn the power amplifier on and off.

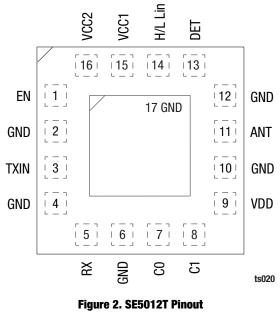
A block diagram of the SE5012T is shown in Figure 1. The device package and pinout for the 16-pin QFN are shown in Figure 2. Signal pin assignments and functional pin descriptions are described in Table 1.



Note: The TXIN has a DC short to ground. An external blocking capacitor is recommended at the TXIN port.

ts009

Figure 1. SE5012T Block Diagram



(Top View

Table 1. SE5012T Signal Descriptions

| Pin | Name | Description | Pin | Name | Description | |
|-----|------|--------------------------|-----|---------|--------------------------------|--|
| 1 | EN | PA enable | 9 | VDD | LNA supply voltage | |
| 2 | GND | Ground | 10 | GND | Ground | |
| 3 | TXIN | 5 GHz TX RF input signal | 11 | ANT | 5 GHz antenna output | |
| 4 | GND | Ground | 12 | GND | Ground | |
| 5 | RX | 5 GHz LNA output signal | 13 | DET | Power detector output | |
| 6 | GND | Ground | 14 | H/L Lin | High-low linearity control | |
| 7 | CO | Switch control logic 1 | 15 | VCC1 | Power amplifier supply voltage | |
| 8 | C1 | Switch control logic 2 | 16 | VCC2 | Power stage supply voltage | |

Electrical and Mechanical Specifications

The absolute maximum ratings of the SE5012T are provided in Table 2. Recommended operating conditions are specified in

Table 3. Electrical specifications are provided in Tables 4 through 9. Figure 3 shows the power detector characteristics.

| Table 2. SE5012T A | bsolute Maximum | Ratings (| (Note 1) |
|--------------------|-----------------|-----------|----------|
|--------------------|-----------------|-----------|----------|

| Parameter | Symbol | Minimum | Maximum | Units |
|--|--------|---------|---------|-------|
| Supply voltage on pins VCC1, VCC2 | Vcc | -0.3 | +5.5 | V |
| Supply voltage on pin VDD | Vdd | -0.3 | +3.6 | V |
| DC input on Enable | Ven | -0.3 | +3.6 | V |
| RF input power, RFout into 50 Ω match | TXIN | | 12 | dBm |
| Storage temperature range | Тѕтс | -40 | +150 | °C |
| Junction temperature | TJ | | +150 | °C |
| Electrostatic discharge: | ESD | | | |
| Human Body Model (HBM), Class 1B | | | 500 | V |

Note 1: Exposure to maximum rating conditions for extended periods may reduce device reliability. There is no damage to device with only one parameter set at the limit and all other parameters set at or below their nominal value. Exceeding any of the limits listed here may result in permanent damage to the device.

Note 2: These are stress ratings only. Exposure to stresses beyond these maximum ratings for a long period of time may cause permanent damage to, or affect the reliability of the device. Avoid operating the device outside the recommended operating conditions defined below.

CAUTION: Although this device is designed to be as robust as possible, electrostatic discharge (ESD) can damage this device. This device must be protected at all times from ESD. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD precautions should be used at all times.

Table 3. SE5012T Recommended Operating Conditions

| Parameter | Symbol | Minimum | Maximum | Units |
|-----------------------------------|--------|---------|---------|-------|
| Supply voltage on pins VCC1, VCC2 | Vcc | 3.0 | 5.5 | V |
| Supply voltage on pin VDD | Vdd | 3.0 | 3.6 | V |
| Ambient temperature | Та | -40 | +85 | °C |

Table 4. SE5012T Electrical Specifications: Control Logic Characteristics (Note 1) (Vcc = 5.0 V, Vdd = Ven = 3.3 V, TA = +25 °C as Measured on the SE5012T-EK1 Evaluation Board, Unless Otherwise Noted)

| Parameter | Symbol | Test Condition | Min | Typical | Мах | Units |
|----------------------------------|-------------|---|------|---------|-----|-------|
| Supply surrent transmit mode | 100,000,110 | Pout = 21 dBm, 54 Mbps, 64 QAM, Vcc = 5.0 V, H/L Lin = 3.3 V | | 270 | 350 | mA |
| Supply current, transmit mode | | Pout = 17 dBm, 54 Mbps, 64 QAM, Vcc = 3.3 V, H/L Lin = 3.3 V | | 195 | | mA |
| LNA supply current | Idd | Ven = C0 = 0 V, C1 = 3.3 V | | 13 | | mA |
| Supply current | loff | VEN = 0 V, no RF, $C0 = C1 = 0 V$ measured on VCC, VDD pins | | 20 | 50 | μΑ |
| Logic high voltage | Venh | | 2.8 | | 3.6 | V |
| Logic low voltage | Venl | | -0.3 | | 0.3 | V |
| Input current logic high voltage | IENH | 10 k Ω on chip pull down resistor | | 330 | 400 | μA |
| Input current logic low voltage | IENL | | | <1 | | μA |

Note 1: Performance is guaranteed only under the conditions listed in this table.

Table 5. SE5012T Electrical Specifications: Switch Logic Characteristics (Note 1) (Vcc = 3.0 V to 5.5 V, Vdd = Ven = 3.3 V, TA = +25 °C as Measured on the SE5012T-EK1 Evaluation Board, All Unused Ports Terminated with 50 Ω , Unless Otherwise Noted)

| Parameter | Symbol | Test Condition | Min | Typical | Мах | Units |
|----------------------------------|--------|---------------------------------|-----|---------|-----|-------|
| Low loss switch control voltage | ON | High state = VCTL_ON - VCTL_OFF | 2.8 | | 3.6 | V |
| High loss switch control voltage | 0FF | Low state = VCTL_OFF - VCTL_OFF | 0 | | 0.3 | V |
| Control input capacitance | CCTL | | | | 100 | pF |
| Control line current | ICTL | Vctl = Vctl_on | | 2 | 10 | μА |

Note 1: Performance is guaranteed only under the conditions listed in this table.

Table 6. Switch Control Logic Table

| CO | C1 | EN | Hi/L Lin | ANT |
|------------------|------------------|-------------------|--------------|-----------|
| All other states | OFF | ON | ON | Тх |
| OFF | OFF | OFF | D/C (Note 1) | Rx bypass |
| OFF | All other states | OFF | D/C (Note 1) | Rx LNA ON |
| All other states | All other states | Unsupported state | | |

Note 1: D/C = don't care

Table 7. SE5012T Electrical Specifications: AC Characteristics (Transmit Characteristics) (Note 1)

(Vcc = 5.0 V, Vdd = Ven = C0 = H/L Lin = 3.3 V, C1 = 0 V, TA = +25 °C, as Measured on the SE5012T-EK1 Evaluation Board, Unless Otherwise Noted)

| Parameter | | Symbol | Test Condition | Min | Typical | Мах | Units |
|--|----------------------------------|-------------|---|---|-----------|---------|---------|
| Frequency range | | fL_U | | 5.15 | | 5.85 | GHz |
| | EVM = 3% | | Vcc = 5.0 V | 19 | 21 | | dBm |
| Output power | EVIVI = 3% | Роит | Vcc = 3.3 V | | 17 | | dBm |
| OFDM signal, 64 QAM, | EVM ≤ 1.5% | P001 | Vcc = 5.0 V | | 12 | | dBm |
| | EVIVI ≤ 1.3% | | Vcc = 3.3 V | | 9 | | dBm |
| Output 1 dB con | npression point, | P1dB | Vcc = 5.0 V | | 27 | | dBm |
| no modulation | | PIOB | Vcc = 3.3 V | | 24 | | dBm |
| Input return loss | | S11 | PIN = -25 dBm | | 12 | | dB |
| Small signal gai | Small signal gain, PIN = −25 dBm | | | 29 | | 36 | dB |
| Small signal gai | Small signal gain variation | | Gain variation over single 40 MHz channel | | | 0.5 | dB |
| Silidii Siyildi yali | II Vallauoli | | Gain variation over band | | 4 | | dB |
| Out of band gair | 1 | S21_3.8 | Gain at 3.8 GHz | | | 15 | dB |
| Harmonic | | 2f | Pout = 17 dBm, OFDM | | -50 | -45.2 | dBm/MHz |
| Haillollic | | 3f | | | -50 | -45.2 | dBm/MHz |
| Rise and fall tim | e | tR, tF | | | 0.5 | | μS |
| Stability S | | STAB | POUT = 17 dBm, 54 Mbps, 64QAM, VSWR = 6:1, all phases | All non-harmonically related outputs less than -50 dBc/100 kHz | | ss than | |
| Tolerance to output load Finance field for the field for t | | Rugged-ness | Constant PIN equal to POUT = 21 dBm at 50 Ω , 54 Mbps, 64QAM, Vcc = 5.5 V, VSWR = 6:1, all phases | No damage | | | |
| Robustness to ir | put power | Robust | PIN = 12 dBm, CW, VSWR = 6:1, all phases | No damage | No damage | | |

Note 1: Performance is guaranteed only under the conditions listed in this table.

| Parameter | Symbol | Test Condition | Min | Typical | Max | Units |
|------------------------------|-----------|---|------|---------|------|-------|
| Frequency range | fout | | 5.15 | | 5.85 | GHz |
| Insertion loss | DV | Bypass mode: $C0 = C1 = 0 V$ | | -5 | | dB |
| Rx gain | RX | High gain mode | 11 | 14 | | dB |
| Noise figure | NF | High gain mode | | 2.5 | 3.5 | dB |
| Input return loss | DVat | At the antenna port | | 12 | | dB |
| Output return loss | RXRL | At RX RF output | | 8 | | dB |
| Innut D4 ID | | Measured at ANT port, high gain mode | -6 | -5 | | dBm |
| Input P1dB | RX_IP1dB | LNA bypass mode | | 10 | | dBm |
| Max 2.4 GHz interferer power | RX_2.4int | 1 dB degradation of IP1dB | | | 0 | dBm |
| Transmit power at Rx output | TXLEAK | Ven = C0 = H/L Lin = 3.3 V, C1 = 0 V, 24 dBm at the ANT port | | -13 | | dBm |
| T/R on/off switching speed | ton/off | C0, C1 (50%) to RF output (10% or 90%) | | 300 | | ns |

Table 8. SE5012T Electrical Specifications: AC Characteristics (Receive Characteristics) (Note 1)

(Vcc = 3.0 V to 5.5 V, VDD = C1 = 3.3 V, VEN = C0 = 0 V, TA = +25 °C as Measured on the SE5012T-EK1 Evaluation Board, All Unused Ports Terminated with 50 Ω . Unless Otherwise Noted)

Note 1: Performance is guaranteed only under the conditions listed in this table.

Table 9. SE5012T Electrical Specifications: Power Detector Characteristics (Note 1)

(Vcc = 3.0 V to 5.5 V, VDD = VEN = C0 = 3.3, C1 = 0 V, f = 5.4 GHz, TA = +25 °C as Measured on the SE5012T-EK1 Evaluation Board, Unless **Otherwise Noted)**

| Parameter | Symbol | Test Condition | Min | Typical | Max | Units |
|-------------------|--------|----------------|------|---------|------|-------|
| Pout detect range | Pdr | | 0 | | P1dB | dBm |
| Detector voltage | VDET22 | Pout = 22 dBm | 0.80 | | 0.95 | V |
| Detector voltage | VDET16 | Pout = 16 dBm | 0.60 | | 0.65 | V |
| Detector voltage | VDET2 | Pout = 2 dBm | 0.25 | | 0.35 | V |
| Output impedance | PDZout | | | 5 | | kΩ |

Note 1: Performance is guaranteed only under the conditions listed in this table.

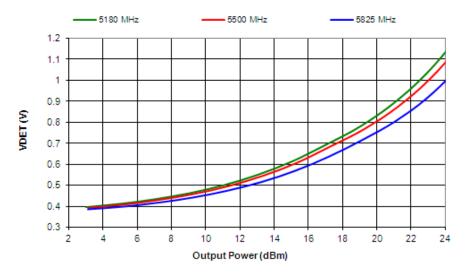


Figure 3. Power Detector Performance vs Frequency

Package Dimensions

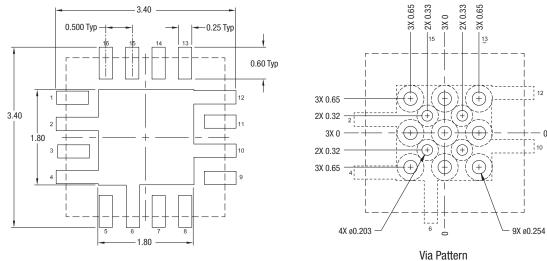
The PCB layout footprint for the SE5012T is provided in Figure 4. Typical part markings are shown in Figure 5. Package dimensions are shown in Figure 6, and carrier tape dimensions are provided in Figure 7.

Package Handling Information

Instructions on the shipping container label regarding exposure to moisture after the container seal is broken must be followed. Otherwise, problems related to moisture absorption may occur when the part is subjected to high temperature during solder assembly.

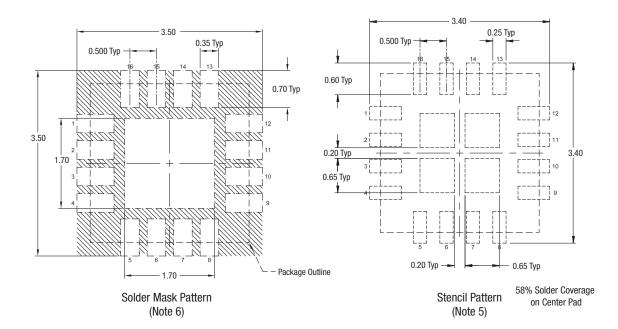
The SE5012T is rated to Moisture Sensitivity Level 1 (MSL1) at 260 °C. It can be used for lead or lead-free soldering. For additional information, refer to the Skyworks Application Note, *Solder Reflow Information*, document number 200164.

Care must be taken when attaching this product, whether it is done manually or in a production solder reflow environment. Production quantities of this product are shipped in a standard tape and reel format.



(Note 4)

Board Metal



Notes:

- All dimensions are in millimeters.
 Dimensions and tolerances according to ASME Y14.5M-1994.
 Unless specified, dimensions are symmetrical about center lines.
 Via hole recommendations:

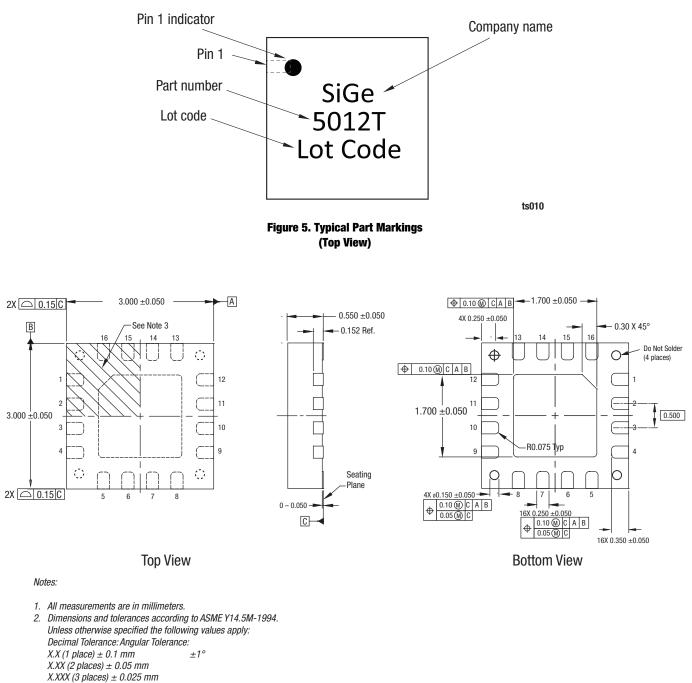
 0.025 mm Cu via wall plating (minimum), solder mask on the far side should tent or plug via holes.

 Stencil recommendations:

 Lencing the should tent or plug via holes.
 Stencil recommendations:
- 0.125 mm stencil thickness, laser cut apertures, trapezoidal walls and
- Contact board fabricator for recommended solder mask offset and tolerance.

Figure 4. PCB Layout Footprint for the SE5012T

Y1642

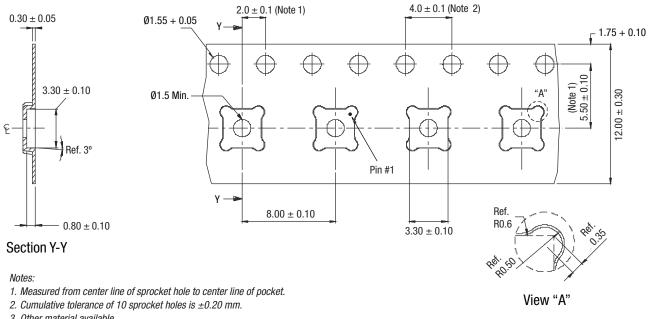


3. Terminal #1 identification mark located within marked area.

Unless specified, dimensions are symmetrical about center lines.

Y0630

Figure 6. SE5012T Package Dimensions



3. Other material available.

4. Typical SR of form tape from 10^5 to $10^{11} \Omega/SQ$.

5. All measurements are in millimeters unless otherwise stated.

Figure 7. SE5012T 16-pin QFN Carrier Tape Dimensions

ts012

Ordering Information

| Model Name |) | Manu | facturing Part Number | Evaluation Board Part Number |
|---------------------------------|---------------------|---------|-----------------------|------------------------------|
| SE5012T: 5 GHz Front-End Module | with Power Detector | SE5012T | | SE5012T-EK1 |

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