UG478: Si34071 Isolated 12 V/6 A Output EVB

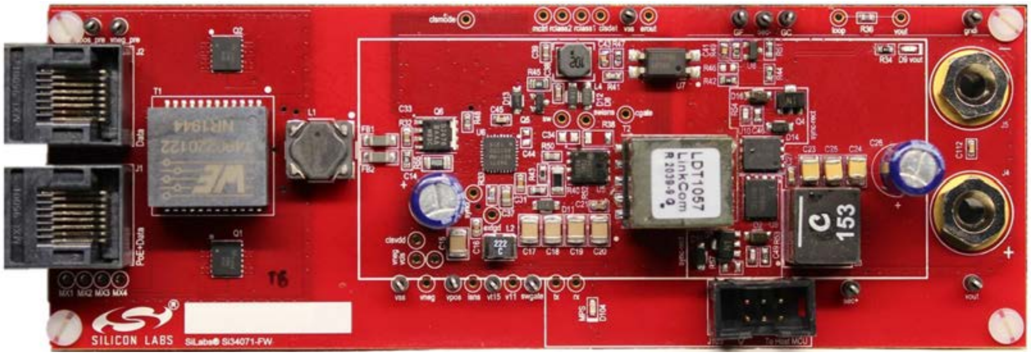
The Si34071 isolated Forward topology evaluation board is a reference design for a power supply in a Power over Ethernet (PoE) Powered Device (PD) application.

The Si34071-FW-12V-C8 board provides an isolated output: 12 V/6 A.

The Si34071-FW-12V-C8 board is shown below. The Si34071 IC integrates an IEEE 802.03bt compatible PoE interface as well as a current-control based dc/dc converter.

KEY FEATURES

- IEEE 802.3bt Compliant
- EMI Compliant
- 91% Efficiency
- High Integration
- Simple 9600-baud UART interface
- Autoclass Feature
- Integrated Transient Overvoltage Protection
- Thermal Shutdown Protection
- 5 x 5 mm 32-pin QFN



Parameter	Condition	Specifications
Ordering Part Number	—	Si34071AC12V8KIT
PSE input voltage range	Connector J1	41.1 V to 57 V
PoE Type/Class	IEEE 802.3bt	Type 4 / Class 8
Output voltage/current	Connectors J4-J5	12 V / 6 A
Peak efficiency, end-to-end	V_{IN} = 50 V, 12 V output	91.2 %
Switching frequency	R33 = 95.3 kΩ	200 kHz
Radiated EMI Test	EN 55032 Class B (30 MHz to 1 GHz)	Passed

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1. Kit Description and Powering up the Si34071-FW-12V-C8 Board

The Si34071-FW-12V-C8 Forward evaluation board is a 12V/6A output power Powered Device reference design for Power over Ethernet (PoE) applications. It provides IEEE 802.3bt interfacing and power supply control in a single chip solution with Si34071. The dc/dc converter utilizes two different operation modes:

- Reset winding forward in low power mode
- Active clamp forward in high power mode

Switching between operation modes is done automatically by the Si34071 dc/dc converter. Input FET bridges are used in order to further improve overall efficiency.

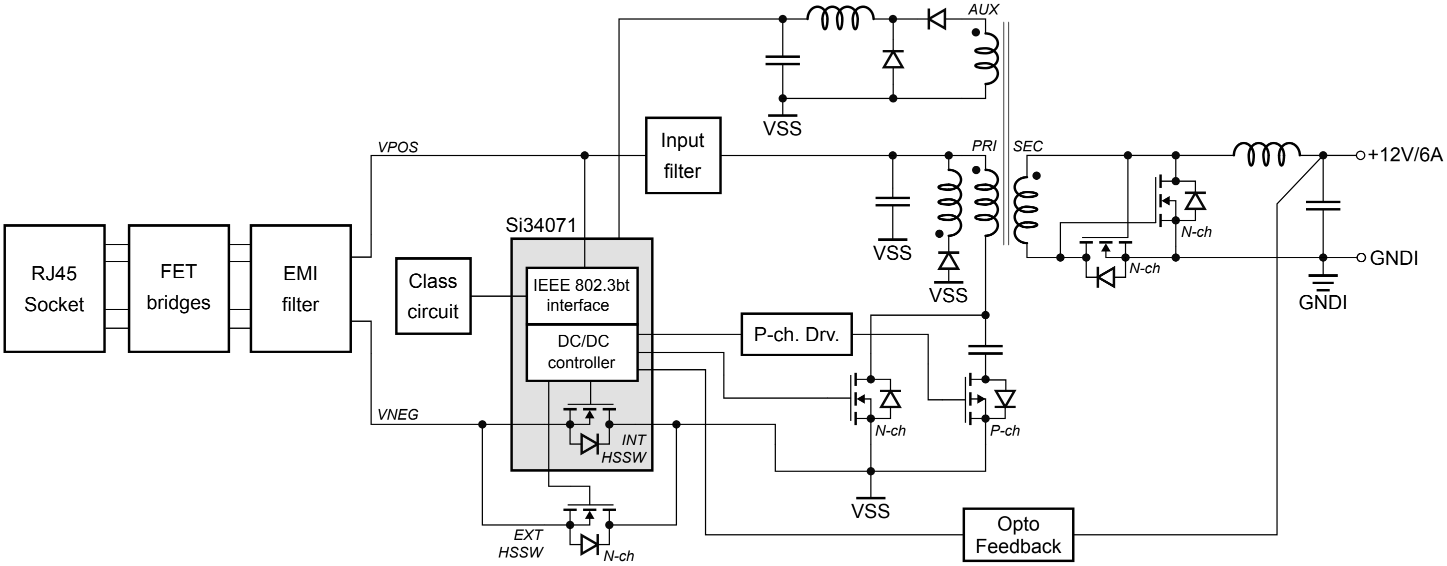


Figure 1.1. Simplified Block Diagram of the Si34071-FW-12V-C8

2. Schematics

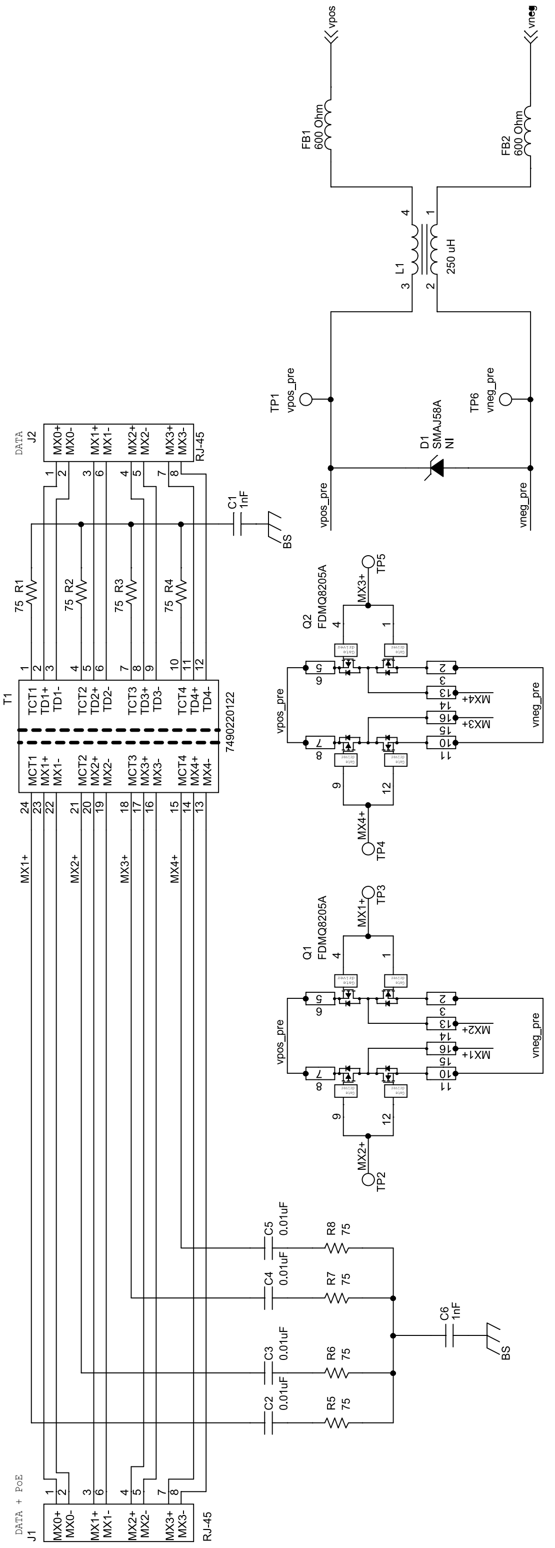


Figure 2.1. Si34071-FW-12V-C8 Schematic: Input interface

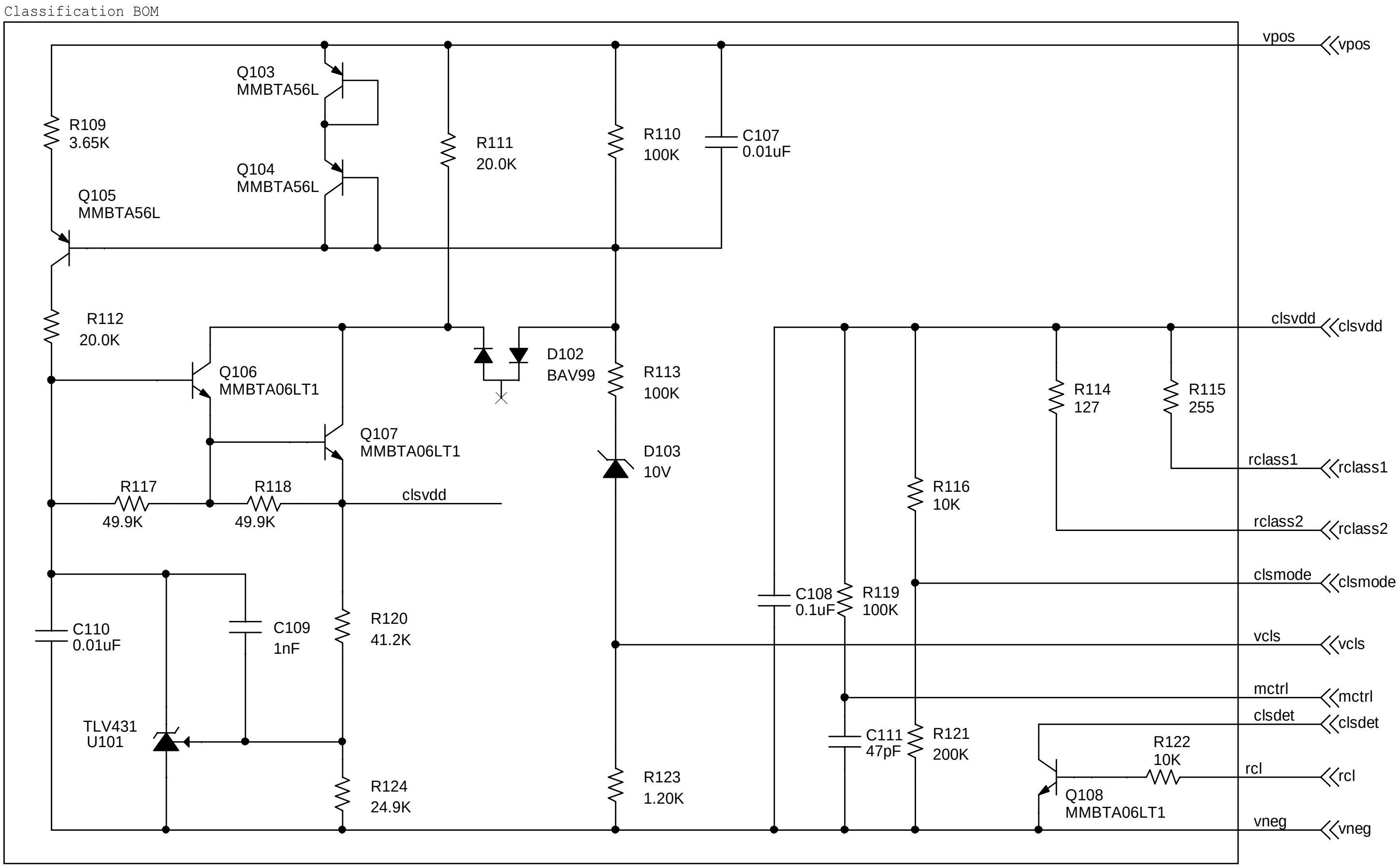


Figure 2.2. Si34071-FW-12V-C8 Schematic: Classification Circuit

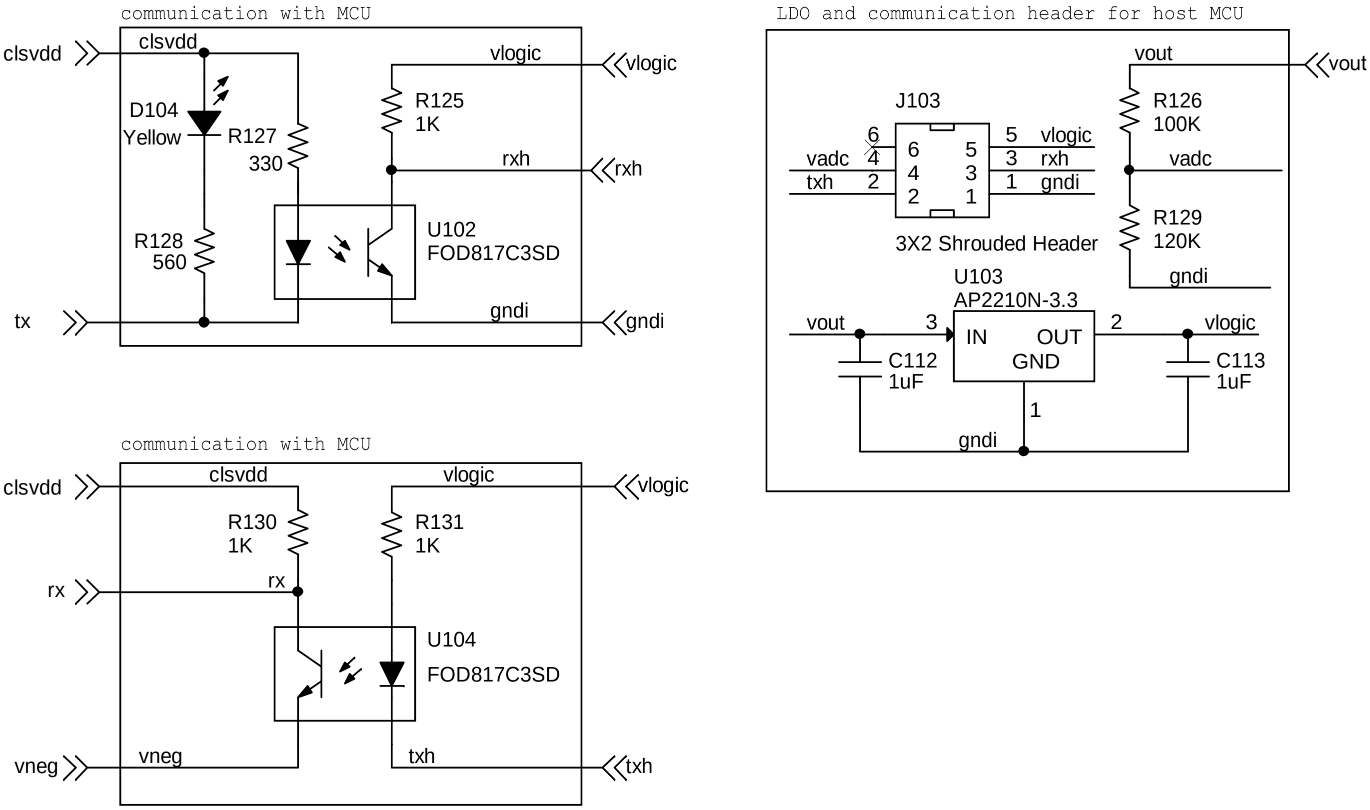


Figure 2.3. Si34071-FW-12V-C8 Schematic: UART Communication (Optional Circuit)

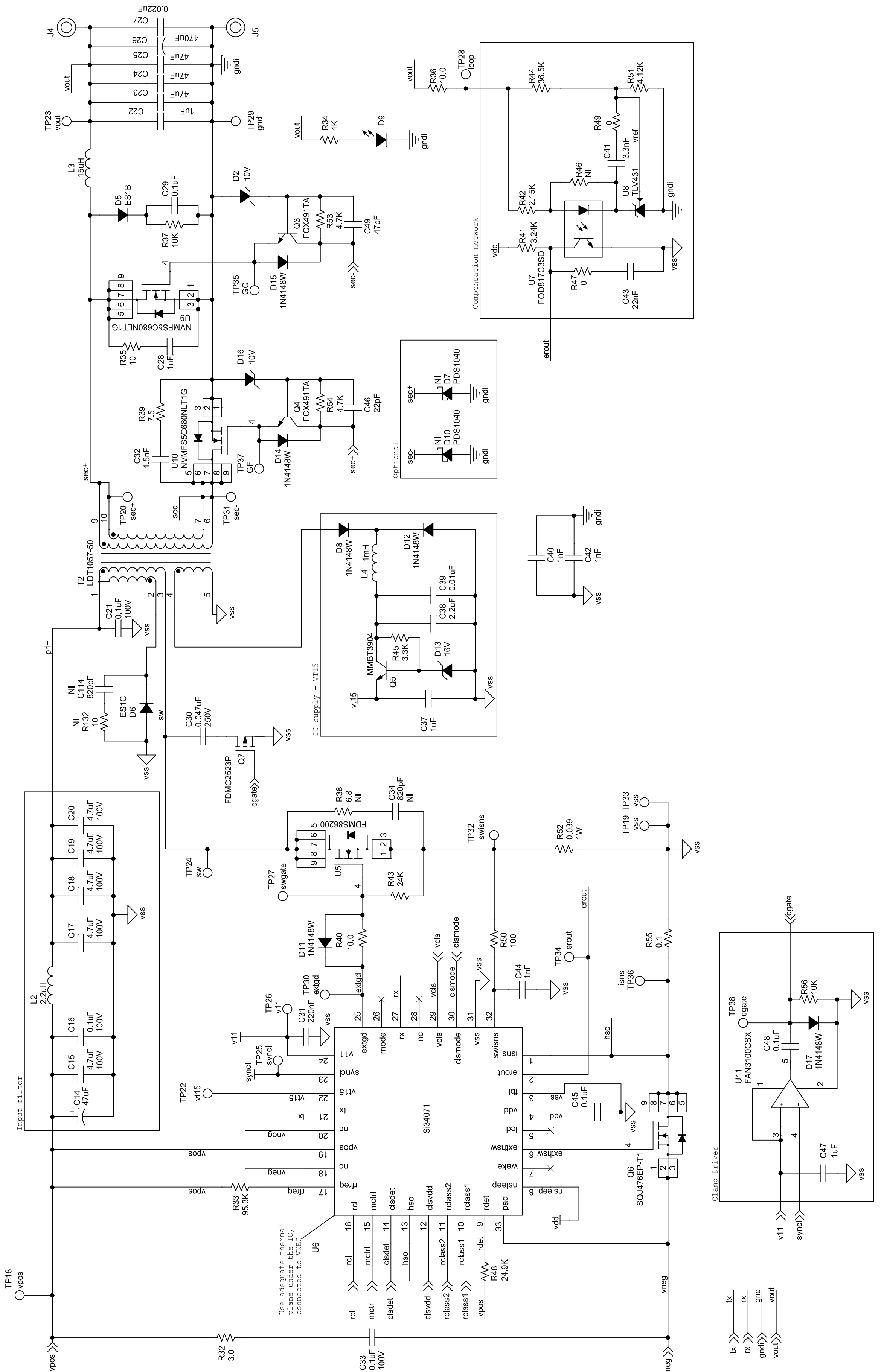


Figure 2.4. Si34071-FW-12V-C8 Schematic: DC-DC Converter

3. Getting Started: Powering Up the Si34071-FW-12V-C8 Board

Ethernet data and power are applied to the board through the PoE+Data RJ45 connector (J1). The board itself has no Ethernet data transmission functionality, but, as a convenience, the Ethernet transformer secondary-side data is connected to the Data RJ45 connector (J2). The design can be used in Gigabit (10/100/1000) systems as well.

Power may be applied in the following ways:

- Using an IEEE 802.3bt-compliant (4 pair), PoE-capable PSE, or
- Using a laboratory power supply unit (PSU). The PSU connection is shown below:

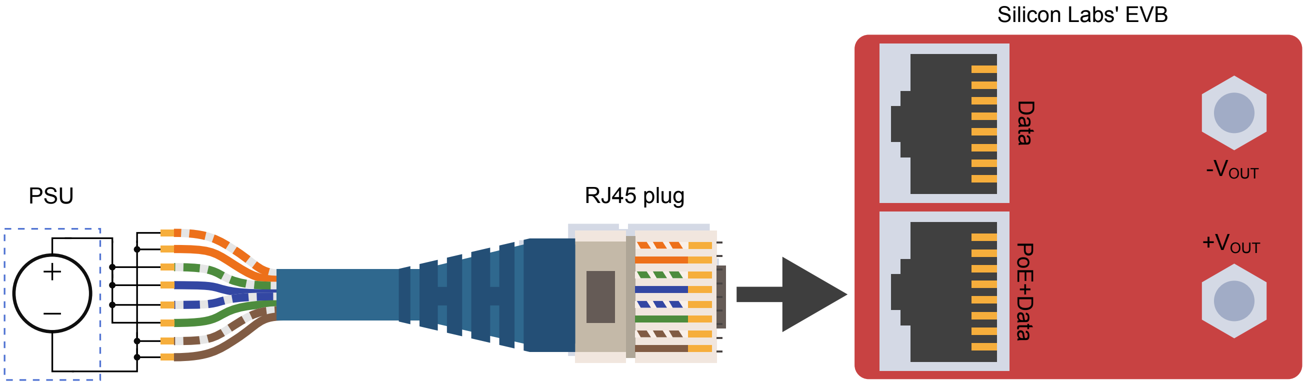


Figure 3.1. Four Pair Connection Using Laboratory Power Supply

Note: 4-pair connection is required for maximum power and highest conversion efficiency.

4. Conversion Efficiency of the Si34071-FW-12V-C8 Board

The end-to-end efficiency measurement data of the Si34071-FW-12V-C8 are shown below. Efficiency was measured from PoE (RJ45 connector) input to the 12 V output. The efficiency was measured on three different input voltage levels, 41.1 V, 50 V and 57 V.

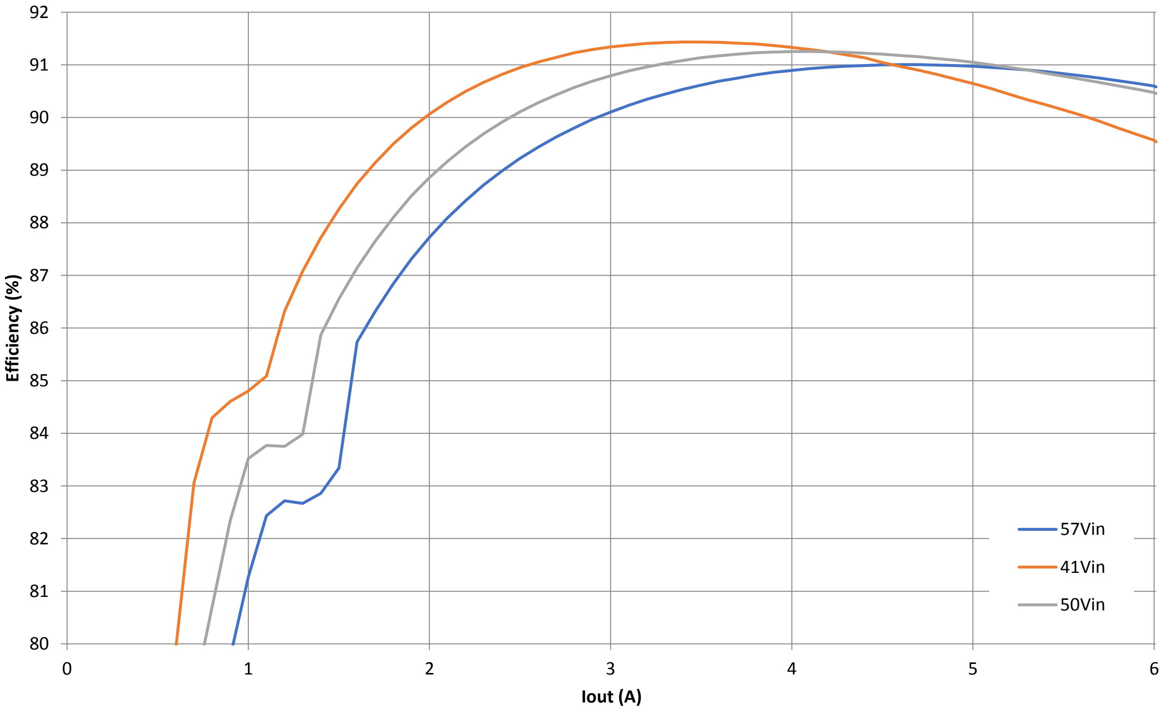


Figure 4.1. Si34071-FW-12V-C8 EVB End-to-End Conversion Efficiency Chart

Note: During the efficiency measurements, LED D9 was removed since it is merely an indicator and not a required part of the design.

5. SIFOS PoE Compatibility Test Results

The PDA-604A Powered Device Analyzer is a single-box comprehensive solution for testing IEEE 802.3at and IEEE 802.3bt PoE Powered Devices. Si34071-FW-12V-C8 EVB board has been successfully tested with the PDA-604A Powered Device Analyzer from SIFOS Technologies. Table 1 below shows the test results of the Sifos Technologies 802.3bt Conformance Test Suite version 1.17.

Table 5.1. Si34071-FW-12V-C8 EVB SIFOS Test Results

ALT A MDI ALT B MDI									
Detection								**Det Cycles**	**3**
Parameter	**Cycle**	**1**	**Units**	**Min**	**Max**	**Average**	**Low Lim**	**High Lim**	**P/F**
SigType		SINGLE	—	—	—	—	SINGLE	SINGLE	P
Rdet_A		24.97	kΩ	24.97	24.97	24.97	23.50	26.60	P
Rdet_final_A		24.88	kΩ	24.88	24.88	24.88	23.50	26.60	P
Rdet_unpwr_A		–1.00	kΩ	–1.00	0.00	–1.00	<12.00	>45.00	P
Rdet_at_Vmin_A		25.01	kΩ	25.01	25.01	25.01	23.50	26.60	P
Rdet_at_Vmax_A		24.94	kΩ	24.94	24.94	24.94	23.50	26.60	P
Rdet_Voffset_A		1.2	VDC	1.2	1.2	1.2	0.0	1.9	P
Cdet_A		0.10	μF	0.10	0.10	0.10	0.04	0.13	P
Cdet_final_A		0.10	μF	0.10	0.10	0.10	0.04	0.13	P
Rdet_B		24.88	kΩ	24.88	24.88	24.88	23.50	26.60	P
Rdet_final_B		24.91	kΩ	24.91	24.91	24.91	23.50	26.60	P
Rdet_unpwr_B		–1.00	kΩ	–1.00	0.00	–1.00	<12.00	>45.00	P
Rdet_at_Vmin_B		25.00	kΩ	25.00	25.00	25.00	23.50	26.60	P
Rdet_at_Vmax_B		25.04	kΩ	25.04	25.04	25.04	23.50	26.60	P
Rdet_Voffset_B		1.2	VDC	1.2	1.2	1.2	0.0	1.9	P
Cdet_B		0.10	μF	0.10	0.10	0.10	0.04	0.13	P
Cdet_final_B		0.10	μF	0.10	0.10	0.10	0.04	0.13	P
Classification									
ClassNum		8		8	8	—	8	8	P
class_sig_EV1-2_min		36.0	mA	36.0	36.0	36.0	35.3	44.8	P
class_sig_EV1-2_max		41.3	mA	41.3	41.3	41.3	35.3	44.8	P
class_sig_EV3-5_min		28.0	mA	28.0	28.0	28.0	25.5	30.6	P
class_sig_EV3-5_max		29.2	mA	29.2	29.2	29.2	25.5	30.6	P
MarkI		2.34	mA	2.34	2.34	2.34	0.25	4.00	P
Tclass_max		3.4	ms	3.4	3.4	3.4	0.2	5.0	P
Iclass_EV1_at_Vmin		39.8	mA	39.8	39.8	39.8	35.5	44.7	P
Iclass_EV1_at_Vmax		40.0	mA	40.0	40.0	40.0	35.5	44.7	P
Class_Reset		1		1	1	—	1	1	P
Autoclass		1		1	1	—	1	1	P
Tacs		84.6	ms	84.6	84.6	84.6	75.5	87.5	P

ALT A MDI-X ALT B MDI									
Detection								**Det Cycles**	3
Parameter	**Cycle**	**1**	**Units**	**Min**	**Max**	**Average**	**Low Lim**	**High Lim**	**P/F**
SigType		SINGLE	—	—	—	—	SINGLE	SINGLE	P
Rdet_A		24.95	kΩ	24.95	24.95	24.95	23.50	26.60	P
Rdet_final_A		24.88	kΩ	24.88	24.88	24.88	23.50	26.60	P
Rdet_unpwr_A		>99.00	kΩ	99.00	99.00	99.00	<12.00	>45.00	P
Rdet_at_Vmin_A		25.04	kΩ	25.04	25.04	25.04	23.50	26.60	P
Rdet_at_Vmax_A		25.00	kΩ	25.00	25.00	25.00	23.50	26.60	P
Rdet_Voffset_A		1.2	VDC	1.2	1.2	1.2	0.0	1.9	P
Cdet_A		0.10	µF	0.10	0.10	0.10	0.04	0.13	P
Cdet_final_A		0.10	µF	0.10	0.10	0.10	0.04	0.13	P
Rdet_B		24.93	kΩ	24.93	24.93	24.93	23.50	26.60	P
Rdet_final_B		24.95	kΩ	24.95	24.95	24.95	23.50	26.60	P
Rdet_unpwr_B		>99.00	kΩ	99.00	99.00	99.00	<12.00	>45.00	P
Rdet_at_Vmin_B		24.98	kΩ	24.98	24.98	24.98	23.50	26.60	P
Rdet_at_Vmax_B		25.07	kΩ	25.07	25.07	25.07	23.50	26.60	P
Rdet_Voffset_B		1.2	VDC	1.2	1.2	1.2	0.0	1.9	P
Cdet_B		0.10	µF	0.10	0.10	0.10	0.04	0.13	P
Cdet_final_B		0.10	µF	0.10	0.10	0.10	0.04	0.13	P
Classification									
ClassNum		8		8	8	—	8	8	P
class_sig_EV1-2_min		37.2	mA	37.2	37.2	37.2	35.3	44.8	P
class_sig_EV1-2_max		41.3	mA	41.3	41.3	41.3	35.3	44.8	P
class_sig_EV3-5_min		28.0	mA	28.0	28.0	28.0	25.5	30.6	P
class_sig_EV3-5_max		29.2	mA	29.2	29.2	29.2	25.5	30.6	P
MarkI		2.34	mA	2.34	2.34	2.34	0.25	4.00	P
Tclass_max		3.4	ms	3.4	3.4	3.4	0.2	5.0	P
Iclass_EV1_at_Vmin		39.8	mA	39.8	39.8	39.8	35.5	44.7	P
Iclass_EV1_at_Vmax		39.8	mA	39.8	39.8	39.8	35.5	44.7	P
Class_Reset		1		1	1	—	1	1	P
Autoclass		1		1	1	—	1	1	P
Tacs		84.6	ms	84.6	84.6	84.6	75.5	87.5	P
Power-Up / Down									
Parameter	**Cycle:**	**1**	**Units**	**Min**	**Max**	**Average**	**Low Lim**	**High Lim**	**P/F**
Iinrush		170.7	mA	170.7	170.7	170.7	0.0	800.0	P
Tinrush_energy		0.305	J	0.305	0.305	0.305	0.000	2.084	P
Iinrush_A		83.5	mA	83.5	83.5	83.5	0.0	600.0	P

Tinrush_energy_A		0.204	J	0.204	0.204	0.204	0.000	1.563	P
Imax_Tdelay_A		8.3	mA	8.3	8.3	8.3	0.0	600.0	P
Iinrush_B		87.2	mA	87.2	87.2	87.2	0.0	600.0	P
Tinrush_energy_B		0.213	J	0.213	0.213	0.213	0.000	1.560	P
Imax_Tdelay_B		38.9	mA	38.9	38.9	38.9	0.0	600.0	P
Vrefl		1.3	VDC	1.3	1.3	1.3	0.0	2.8	P
Von		36.4	VDC	36.4	36.4	36.4	30.0	42.0	P
Voff		32.5	VDC	32.5	32.5	32.5	30.0	42.0	P
Vhyst		3.9	VDC	3.9	3.9	3.9	0.0	12.0	P
2 Pair Powered Type-1 PHY		***PSE Emulation***		**On Time**	**10 sec**	**Off Time**	**10 sec**	**Vport**	**48.0**
Parameter	**Cycle**	**1**	**Units**	**Min**	**Max**	**Average**	**Low Lim**	**High Lim**	**P/F**
MinI_1		37.0	mA	37.0	37.0	37.0	0.0	299.0	P
Vport_1		48.2	VDC	48.2	48.2	48.2	37.0	57.0	INFO
Ppeak_1		1.90	W	1.90	1.90	1.90	0.0	14.4	P
Pport_1		1.81	W	1.81	1.81	1.81	0.0	13.0	P
PeakViolation_1		0		0	0	—	0	0	P
MPSViolation_1		0		0	0	—	0	0	P
TcutWindowViolation_1		0		0	0	—	0	0	P
DutyCycleViolation_1		0		0	0	—	0	0	P
2 Pair Powered Type-2 PHY		***PSE Emulation***		**On Time**	**10 sec**	**Off Time**	**10 sec**	**Vport**	**50.0**
Parameter	**Cycle**	**1**	**Units**	**Min**	**Max**	**Average**	**Low Lim**	**High Lim**	**P/F**
MinI_2		7.8	mA	7.8	7.8	7.8	0.0	564.9	P
Vport_2		50.2	VDC	50.2	50.2	50.2	42.5	57.0	INFO
Ppeak_2		5.84	W	5.84	5.84	5.84	0.0	28.3	P
Pport_2		2.24	W	2.24	2.24	2.24	0.0	25.5	P
PeakViolation_2		0		0	0	—	0	0	P
MPSViolation_2		0		0	0	—	0	0	P
TcutWindowViolation_2		0		0	0	—	0	0	P
DutyCycleViolation_2		0		0	0	—	0	0	P
4 Pair Powered Type-3 PHY		***PSE Emulation***		**On Time**	**10 sec**	**Off Time**	**10 sec**	**Vport**	**50.0**
Parameter	**Cycle**	**1**	**Units**	**Min**	**Max.**	**Average**	**Low Lim**	**High Lim**	**P/F**
MinI_3		9.4	mA	9.4	9.4	9.4	0.0	1070.0	P
Vport-2P_3_A		50.0	VDC	50.0	50.0	50.0	42.5	57.0	INFO
Vport-2P_3_B		49.9	VDC	49.9	49.9	49.9	42.5	57.0	INFO
Ppeak_3		5.78	W	5.78	5.78	5.78	0.0	53.5	P
Pport_3		2.34	W	2.34	2.34	2.34	0.0	2.4	P

PeakViolation_3		0		0	0	—	0	0	P
MPSViolation_3		0		0	0	—	0	0	P
TcutWindowViolation_3		0		0	0	—	0	0	P
DutyCycleViolation_3		0		0	0	—	0	0	P
4 Pair Powered Type-4 PHY		***PSE Emulation***		**On Time**	**30 sec**	**Off Time**	**10 sec**	**Vport**	**52.0**
Parameter	**Cycle**	**1**	**Units**	**Min.**	**Max.**	**Average**	**Low Lim**	**High Lim**	**P/F**
MinI_4		9.4	mA	9.4	9.4	9.4	0.0	1440.4	P
Vport-2P_4_A		52.0	VDC	52.0	52.0	52.0	41.1	57.0	INFO
Vport-2P_4_B		52.0	VDC	52.0	52.0	52.0	41.1	57.0	INFO
Ppeak_4		5.84	W	5.84	5.84	5.84	0.0	74.9	P
Pport_4		2.72	W	2.72	2.72	2.72	0.0	2.8	P
PeakViolation_4		0		0	0	—	0	0	P
MPSViolation_4		0		0	0	—	0	0	P
TcutWindowViolation_4		0		0	0	—	0	0	P
DutyCycleViolation_4		0		0	0	—	0	0	P
ALT A MDI ALT B MDI-X									
Detection								**Det_Cycles**	**3**
Parameter	**Cycle**	**1**	**Units**	**Min**	**Max**	**Average**	**Low Lim**	**High Lim**	**P/F**
SigType		SINGLE	—	—	—	—	SINGLE	SINGLE	P
Rdet_A		24.90	kΩ	24.90	24.90	24.90	23.50	26.60	P
Rdet_final_A		24.93	kΩ	24.93	24.93	24.93	23.50	26.60	P
Rdet_unpwr_A		–1.00	kΩ	–1.00	0.00	–1.00	<12.00	>45.00	P
Rdet_at_Vmin_A		25.08	kΩ	25.08	25.08	25.08	23.50	26.60	P
Rdet_at_Vmax_A		24.91	kΩ	24.91	24.91	24.91	23.50	26.60	P
Rdet_Voffset_A		1.2	VDC	1.2	1.2	1.2	0.0	1.9	P
Cdet_A		0.10	μF	0.10	0.10	0.10	0.04	0.13	P
Cdet_final_A		0.10	μF	0.10	0.10	0.10	0.04	0.13	P
Rdet_B		24.91	kΩ	24.91	24.91	24.91	23.50	26.60	P
Rdet_final_B		24.88	kΩ	24.88	24.88	24.88	23.50	26.60	P
Rdet_unpwr_B		–1.00	kΩ	–1.00	0.00	–1.00	<12.00	>45.00	P
Rdet_at_Vmin_B		25.17	kΩ	25.17	25.17	25.17	23.50	26.60	P
Rdet_at_Vmax_B		25.12	kΩ	25.12	25.12	25.12	23.50	26.60	P
Rdet_Voffset_B		1.1	VDC	1.1	1.1	1.1	0.0	1.9	P
Cdet_B		0.10	μF	0.10	0.10	0.10	0.04	0.13	P
Cdet_final_B		0.10	μF	0.10	0.10	0.10	0.04	0.13	P
Classification									
ClassNum		8		8	8	—	8	8	P

class_sig_EV1-2_min	36.0	mA	36.0	36.0	36.0	35.3	44.8	P
class_sig_EV1-2_max	41.3	mA	41.3	41.3	41.3	35.3	44.8	P
class_sig_EV3-5_min	28.0	mA	28.0	28.0	28.0	25.5	30.6	P
class_sig_EV3-5_max	29.2	mA	29.2	29.2	29.2	25.5	30.6	P
MarkI	2.35	mA	2.35	2.35	2.35	0.25	4.00	P
Tclass_max	3.4	ms	3.4	3.4	3.4	0.2	5.0	P
Iclass_EV1_at_Vmin	39.6	mA	39.6	39.6	39.6	35.5	44.7	P
Iclass_EV1_at_Vmax	39.6	mA	39.6	39.6	39.6	35.5	44.7	P
Class_Reset	1		1	1	—	1	1	P
Autoclass	1		1	1	—	1	1	P
Tacs	84.6	ms	84.6	84.6	84.6	75.5	87.5	P
ALT A MDI-X ALT B MDI-X								
Detection							**Det_Cycles**	**3**
Parameter Cycle	**1**	**Units**	**Min**	**Max**	**Average**	**Low Lim**	**High Lim**	**P/F**
SigType	SINGLE	—	—	—	—	SINGLE	SINGLE	P
Rdet_A	24.81	kΩ	24.81	24.81	24.81	23.50	26.60	P
Rdet_final_A	24.81	kΩ	24.81	24.81	24.81	23.50	26.60	P
Rdet_unpwr_A	–1.00	kΩ	–1.00	0.00	–1.00	<12.00	>45.00	P
Rdet_at_Vmin_A	25.09	kΩ	25.09	25.09	25.09	23.50	26.60	P
Rdet_at_Vmax_A	24.97	kΩ	24.97	24.97	24.97	23.50	26.60	P
Rdet_Voffset_A	1.2	VDC	1.2	1.2	1.2	0.0	1.9	P
Cdet_A	0.10	µF	0.10	0.10	0.10	0.04	0.13	P
Cdet_final_A	0.10	µF	0.10	0.10	0.10	0.04	0.13	P
Rdet_B	24.81	kΩ	24.81	24.81	24.81	23.50	26.60	P
Rdet_final_B	24.95	kΩ	24.95	24.95	24.95	23.50	26.60	P
Rdet_unpwr_B	–1.00	kΩ	–1.00	0.00	–1.00	<12.00	>45.00	P
Rdet_at_Vmin_B	25.05	kΩ	25.05	25.05	25.05	23.50	26.60	P
Rdet_at_Vmax_B	25.03	kΩ	25.03	25.03	25.03	23.50	26.60	P
Rdet_Voffset_B	1.1	VDC	1.1	1.1	1.1	0.0	1.9	P
Cdet_B	0.10	µF	0.10	0.10	0.10	0.04	0.13	P
Cdet_final_B	0.10	µF	0.10	0.10	0.10	0.04	0.13	P
Classification								
ClassNum	8		8	8	—	8	8	P
class_sig_EV1-2_min	37.6	mA	37.6	37.6	37.6	35.3	44.8	P
class_sig_EV1-2_max	41.3	mA	41.3	41.3	41.3	35.3	44.8	P
class_sig_EV3-5_min	28.0	mA	28.0	28.0	28.0	25.5	30.6	P
class_sig_EV3-5_max	29.2	mA	29.2	29.2	29.2	25.5	30.6	P
MarkI	2.34	mA	2.34	2.34	2.34	0.25	4.00	P

Tclass_max	3.4	ms	3.4	3.4	3.4	0.2	5.0	P
Iclass_EV1_at_Vmin	40.0	mA	40.0	40.0	40.0	35.5	44.7	P
Iclass_EV1_at_Vmax	39.8	mA	39.8	39.8	39.8	35.5	44.7	P
Class_Reset	1		1	1	—	1	1	P
Autoclass	1		1	1	—	1	1	P
Tacs	84.6	ms	84.6	84.6	84.6	75.5	87.5	P

6. Feedback Loop Phase and Gain Measurement Results (Bode Plots)

The Si34071 device integrates a current mode-controlled switching mode power supply controller circuit. Therefore, the application is a closed-loop system. To guarantee a stable output voltage of a power supply and to reduce the influence of input supply voltage variations and load changes on the output voltage, the feedback loop should be stable. To verify the stability of the loop, the loop gain and loop phase has been measured.

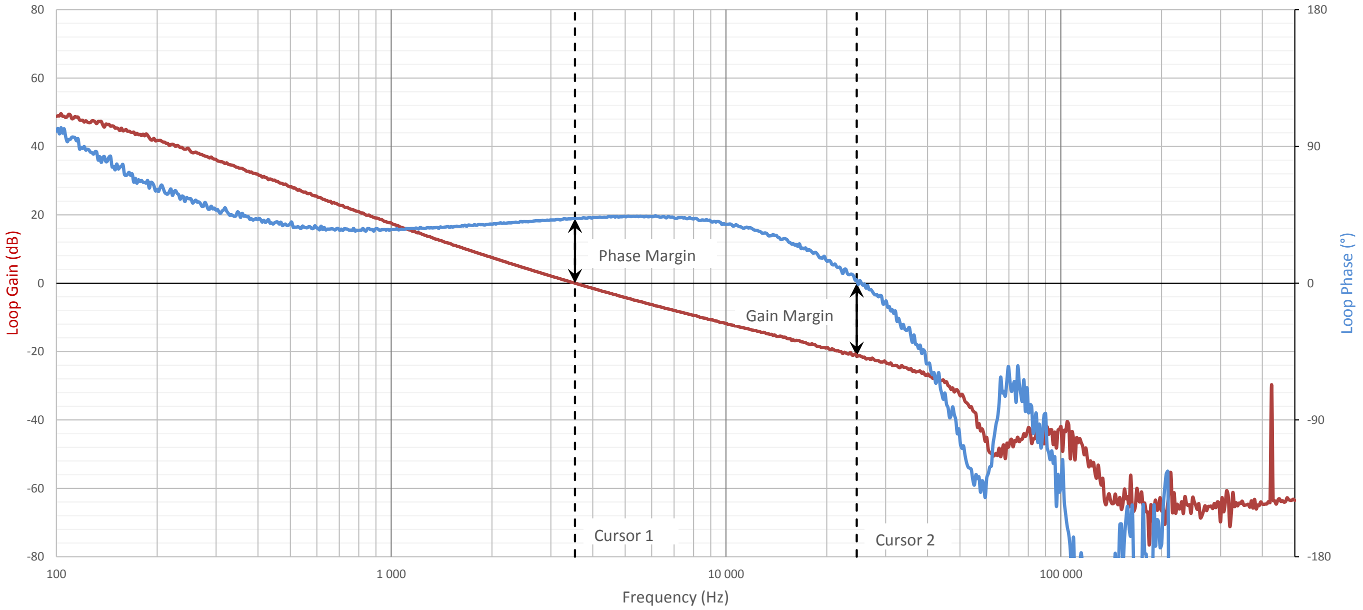


Figure 6.1. Si34071-FW-12V-C8 EVB Measured Loop-Gain and Phase with 72 W Load

	Frequency	Gain	Phase
Phase Margin (Cursor 1)	3.5 kHz	0 dB	42°
Gain Margin (Cursor 2)	24.7 kHz	–21.3 dB	0 °

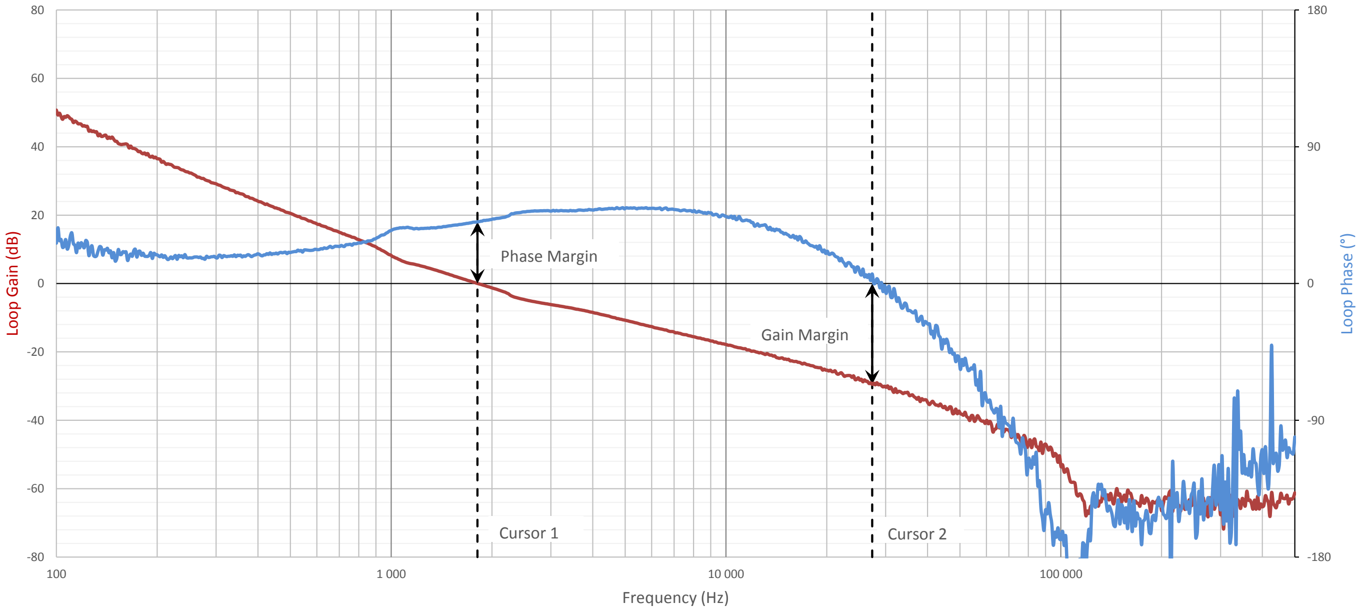


Figure 6.2. Si34071-FW-12V-C8 EVB Measured Loop-Gain and Phase with Unloaded Output

	Frequency	Gain	Phase
Phase Margin (Cursor 1)	1.8 kHz	0 dB	40°
Gain Margin (Cursor 2)	27.6 kHz	–29.0 dB	0 °

7. Load Step Transient Measurement Results

The Si34071-FW-12V-C8 output has been tested with a load step function to verify the converter's output dynamic response. The output was tested with 10%→90% and 90%→10% load steps.

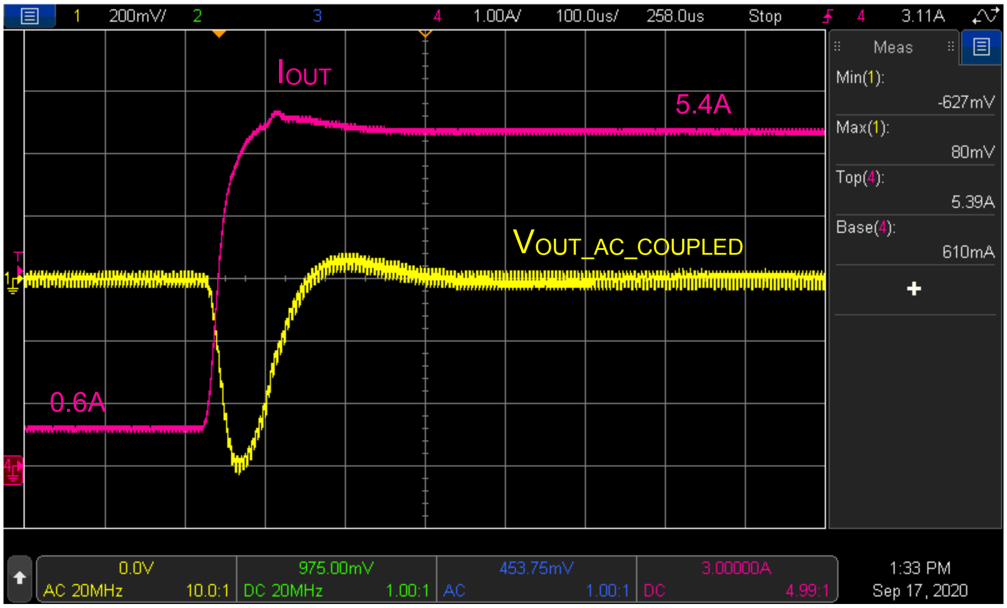


Figure 7.1. 12 V Output Load-Step Response (Current Step: 0.6 A ↔ 5.4 A)

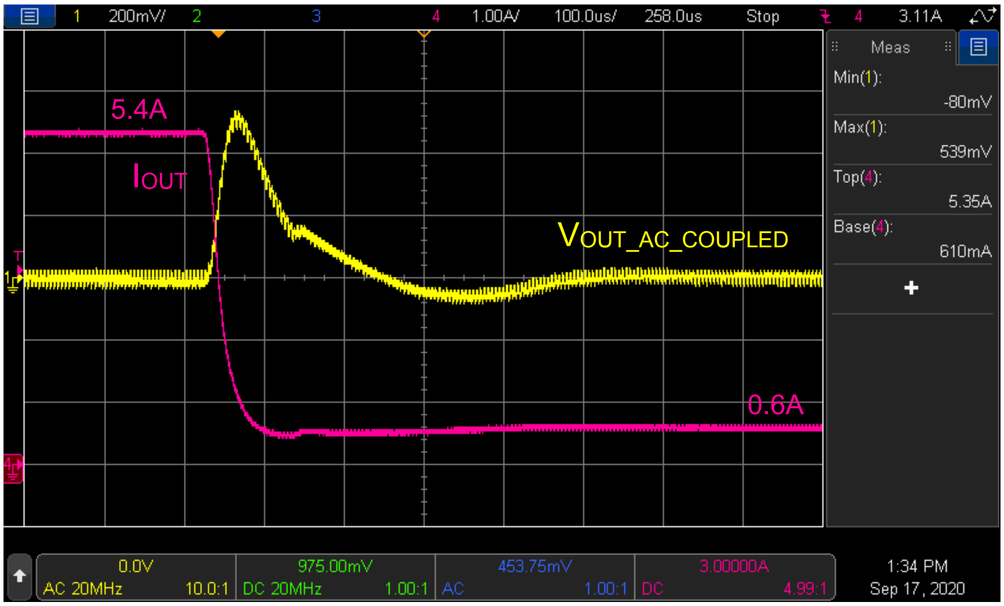
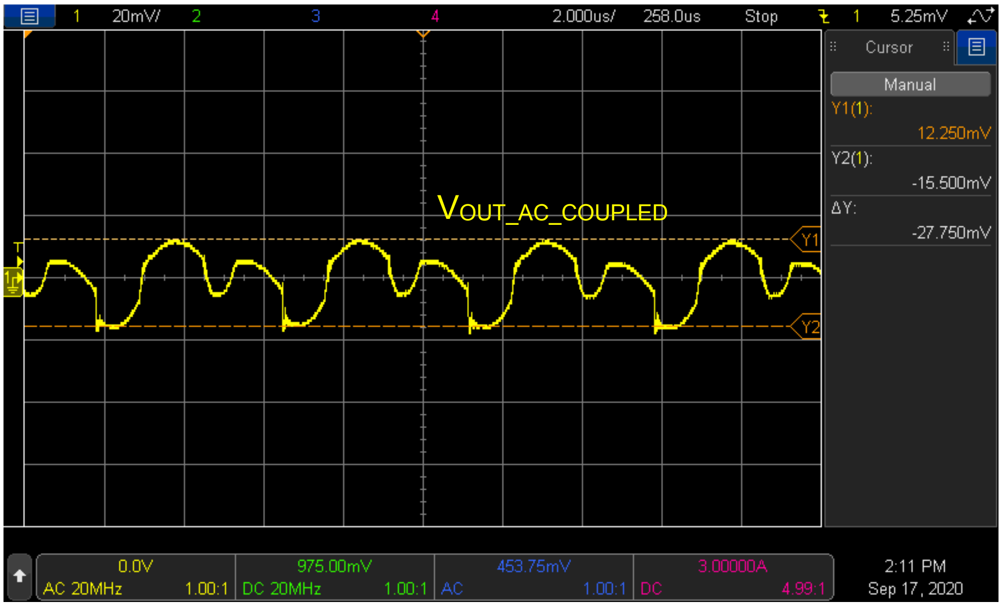


Figure 7.2. 12 V Output Load-Step Response (Current Step: 5.4 A ↔ 0.6 A)

Current Step	Undershoot/Overshoot
10% to 90%	–627 mV
90% to 10%	+539 mV

8. Output Voltage Ripple

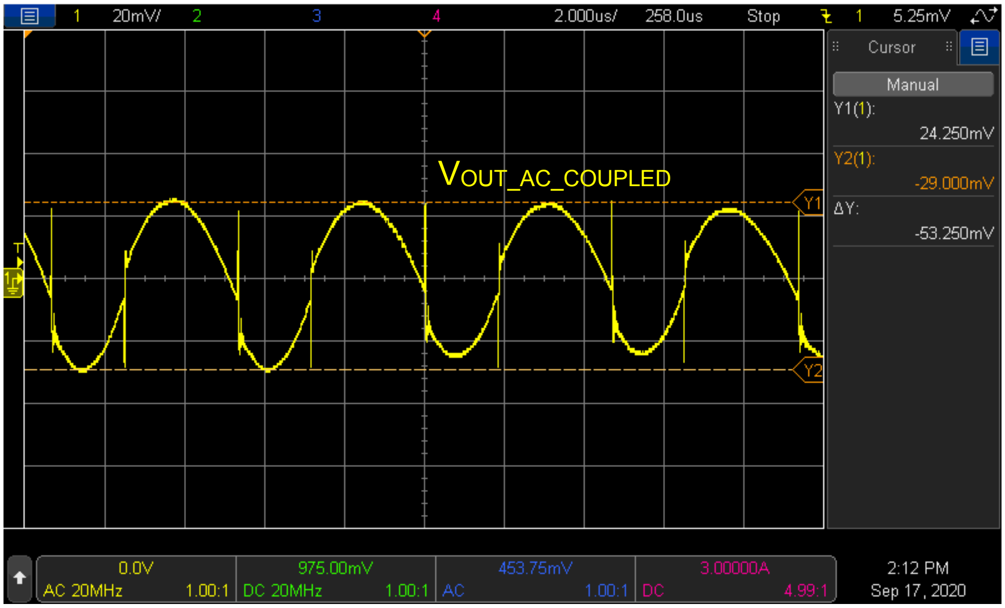
The Si34071-FW-12V-C8 board`s output voltage ripple has been measured at no-load and full-load conditions with 50V input voltage. The following figures show the respective results.



Y1(1): 12.250mV
Y2(1): -15.500mV
ΔY: -27.750mV

0.0V AC 20MHz 1.00:1 | 975.00mV DC 20MHz 1.00:1 | 453.75mV AC 1.00:1 | 3.00000A DC 4.99:1

Figure 8.1. Si34071-FW-12V-C8 Output Voltage Ripple at No-Load Condition (28 mV)



Y1(1): 24.250mV
Y2(1): -29.000mV
ΔY: -53.250mV

0.0V AC 20MHz 1.00:1 | 975.00mV DC 20MHz 1.00:1 | 453.75mV AC 1.00:1 | 3.00000A DC 4.99:1

Figure 8.2. Si34071-FW-12V-C8 Output Voltage Ripple at Full-Load Condition (53 mV)

9. Soft Start Protection

The Si34071 device has an integrated dynamic soft-start protection mechanism to avoid stressing the components by the sudden current or voltage changes associated with the initial chargingof the output capacitors.

The Si34071 intelligent adaptive soft-start mechanism does not require any external component to install. The controller continuously measures the input current of the PD and dynamically adjusts the internal IPEAK limit during soft-start, that way adjusting the output voltage ramping up time in a function of the attached load.

The controller lets the output voltage to rise faster in no load (or light load) condition. With heavy load at the output, the controller slows down the output voltage ramp to avoid exceeding the desired regulated output voltage value.

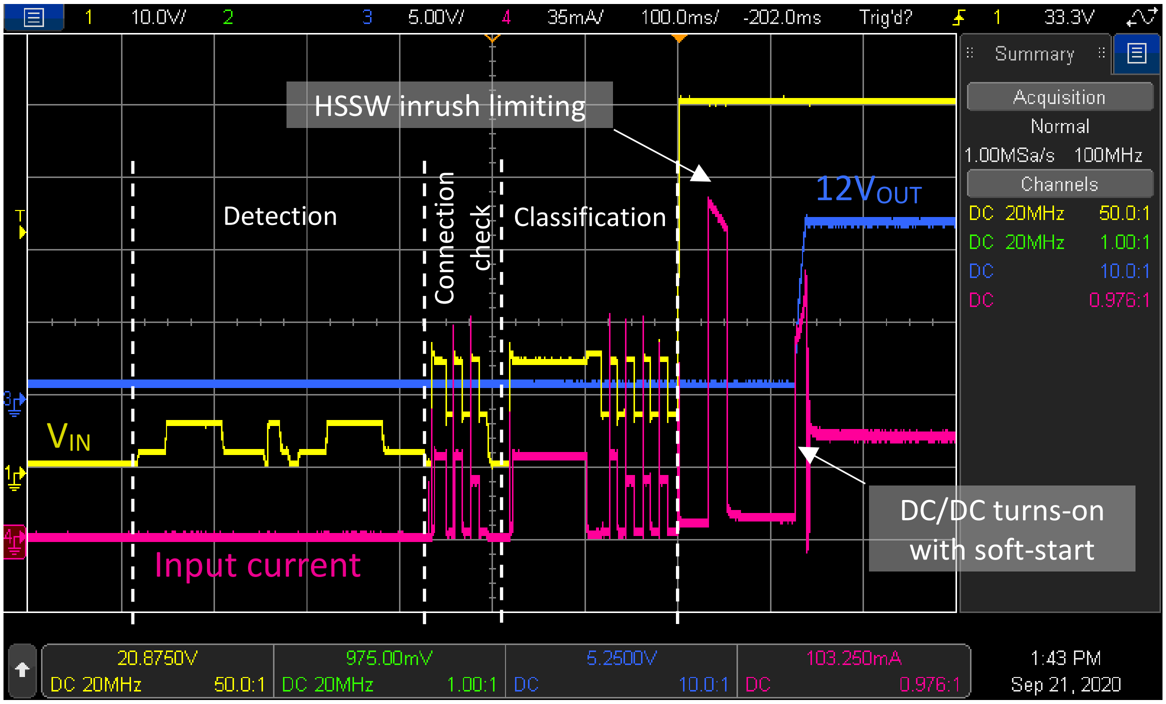


Figure 9.1. Soft Start Waveforms at No Load Condition

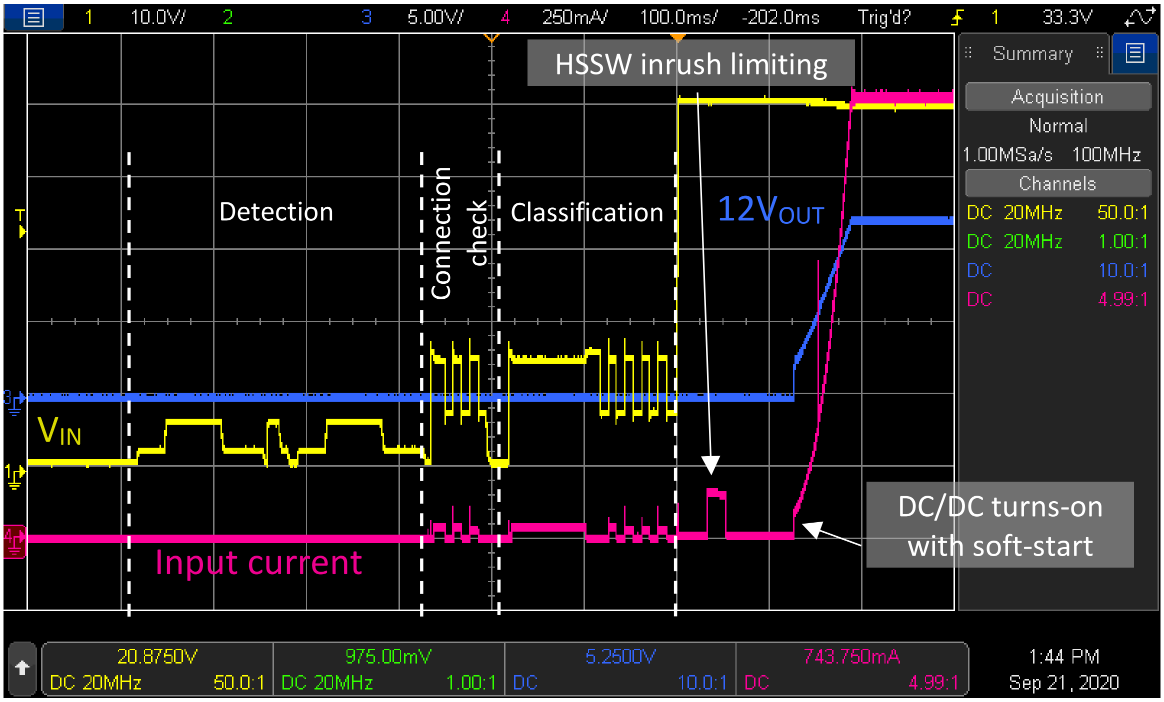


Figure 9.2. Soft Start Waveforms at Full Load Condition

10. Output Short Protection

The Si34071 device has an integrated output short-protection mechanism that protects the IC itself and the surrounding external components from overheating, overvoltage, overcurrent in case of an electrical short on the output. In case of short the energy is not reducing from the output filter inductor because the voltage on the inductor is very low. To avoid overstressing the components in output short the Si34071 sequentially resets itself and restarts with soft-start as long as the output short persists. The figure below shows both primary forward switch (U5) drain to source voltage and main XFMR (T2) secondary voltage stays at safe level under output short.

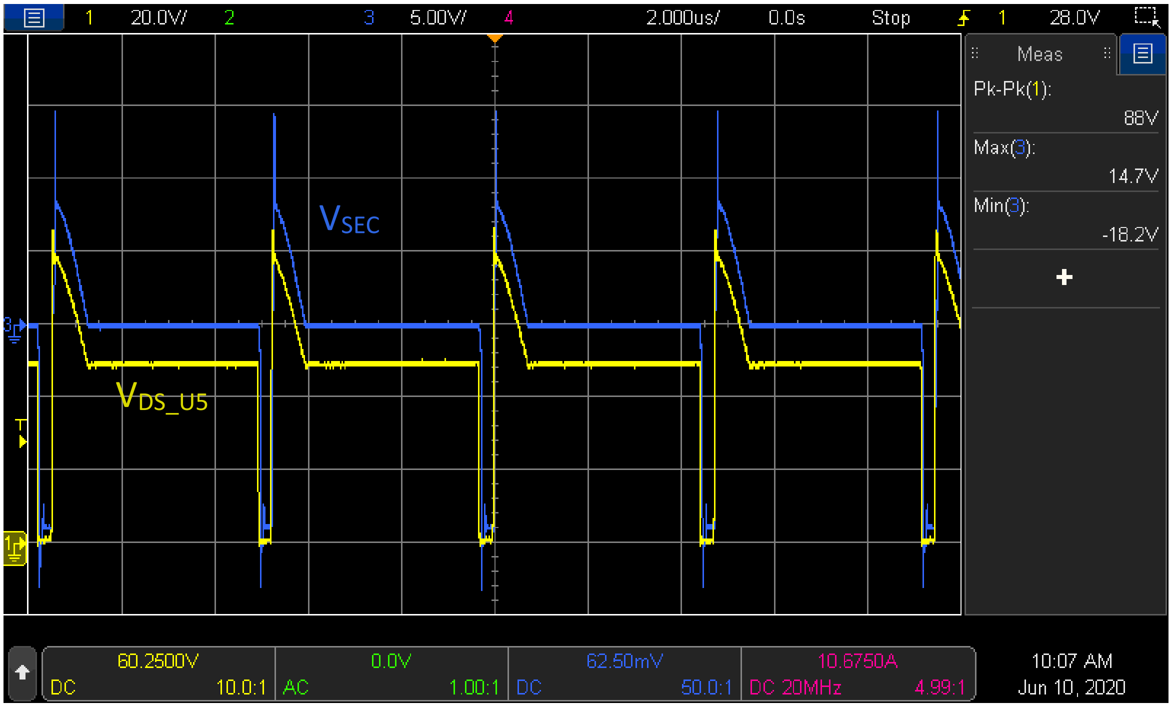


Figure 10.1. Si34071-FW-12V-C8 Output Short Protection Mechanism

11. High-Power and Low-Power Modes

The Si34071 senses the average input current via the R_{SENSE} external current sense resistor (R55) connected between the ISNS pin and V_{SS}. Attention must be paid that the sensed voltage on the ISNS pin goes below V_{SS}. Depending on the voltage on the current sense resistor (V_{SENSE}) the Si34071 automatically switches between low-power and high-power mode. The Si34071 compares V_{SENSE} with its internally fixed V_{ISNS_LC} (–30 mV typ.) threshold, and depending on the comparison, the converter can switch to:

- Low-power mode, if $V_{SENSE} < |-30\text{ mV}|$
- High-power mode, if $V_{SENSE} > |-30\text{ mV}|$

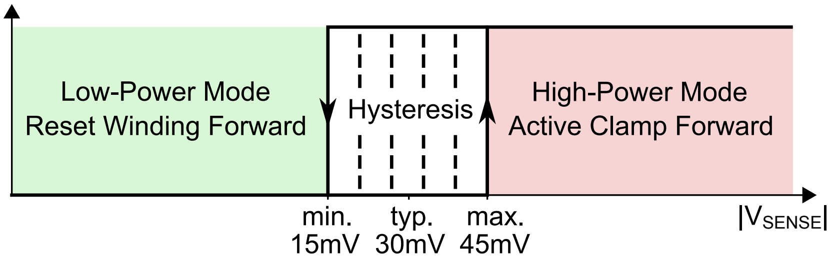


Figure 11.1. Operating Modes of the Si34071

In low-power mode, both the SYNCL and EXTHSW output remain low, and the transformer core reset is performed by the reset winding circuitry. In this mode, input current can flow only on the Si34071's internal hot swap switch. In high-power mode, the EXTHSW output turns on the external hot swap switch (Q6) and input current will be shared between the Si34071's internal and the external hot swap switch. In addition, SYNCL starts switching, so core reset is performed by the active clamp circuitry. The following figures show switching between low-power and high-power modes as the output load changes.

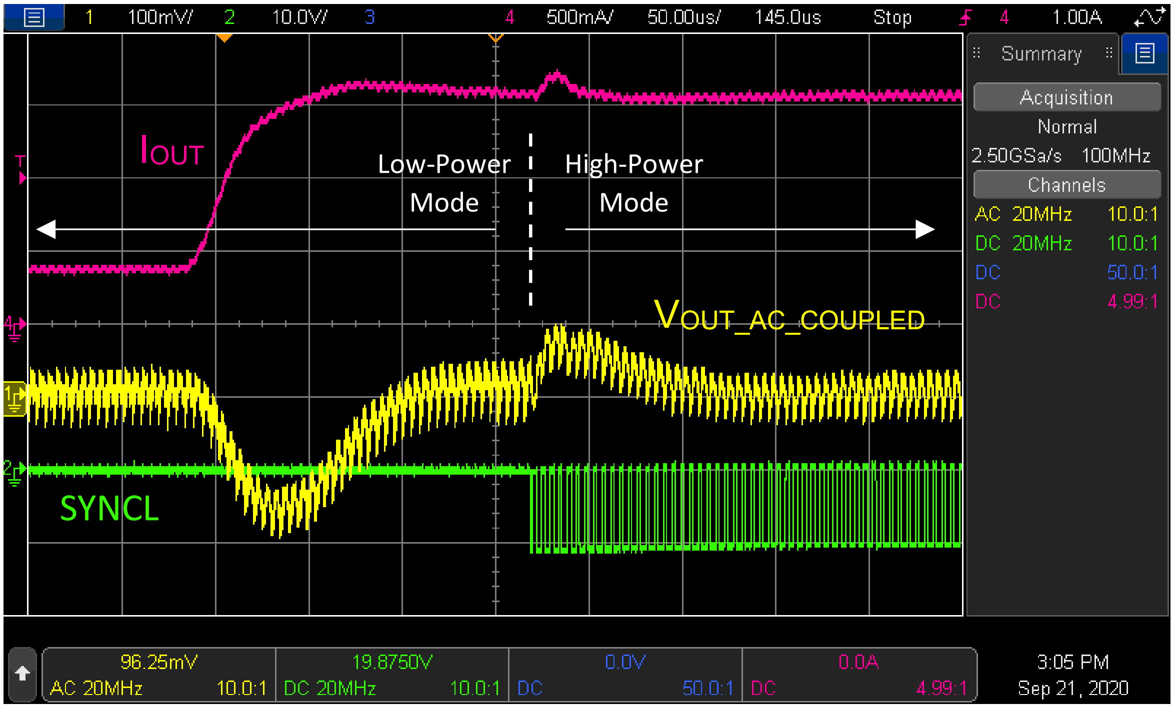


Figure 11.2. Low-Power Mode to High-Power Mode Transition (I_{OUT} changes from 0.4 A to 1.6 A)

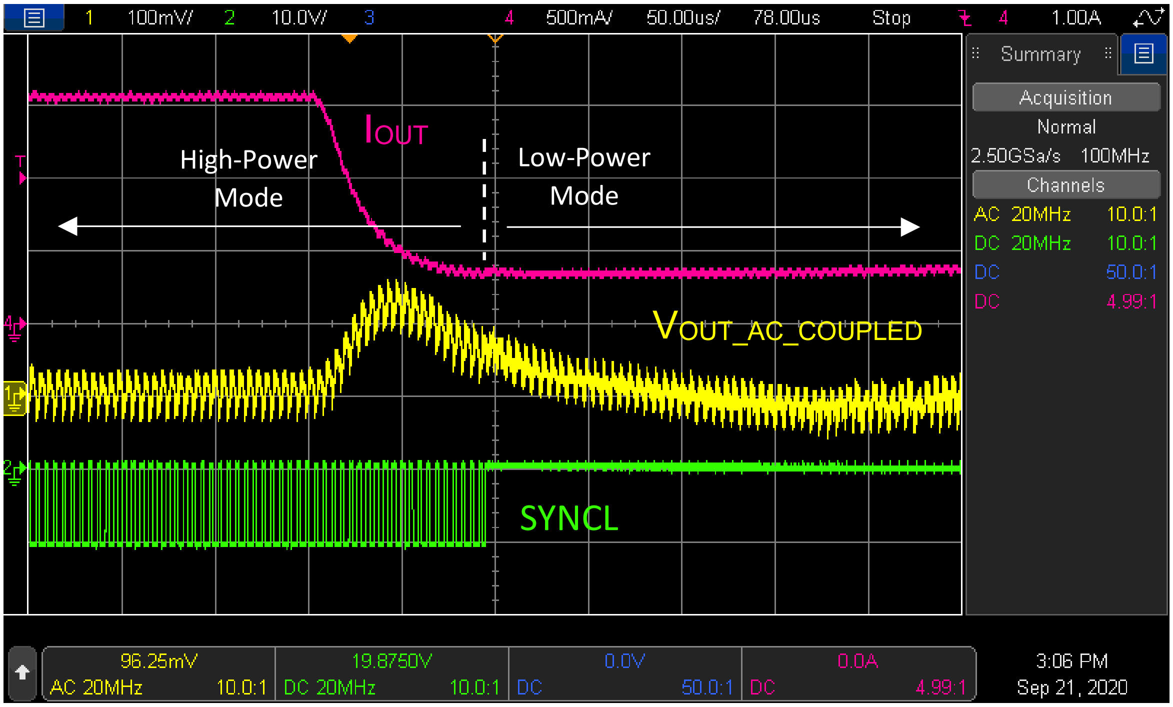


Figure 11.3. High-Power Mode to Low-Power Mode Transition (I_{OUT} changes from 1.6 A to 0.4 A)

12. Adjustable EVB Current Limit

The Si34071 has an adjustable average input current limit feature controlled by R_{SENSE} (R55). When the voltage on R_{SENSE} reaches the internally fixed –270 mV (referenced to V_{SS}), the current limit circuit restarts the controller with soft-start to protect the application from overcurrent. In a Class 8 application, the recommended value for R_{SENSE} is 100 mΩ. Based on this value the average input current limit is given by the following formula:

$$R_{SENSE} = 100m\Omega$$

$$I_{LIMIT} = \frac{270mV}{100m\Omega} = \quad 2.7A$$

Equation 1. Average Input Current Limit

As can be seen in the previous chapter R_{SENSE} determines both external hotswap switch and SYNCL turn-on threshold. To not to exceed the internal hotswap switch continuous operating current limit ($I_{MAXHSSW}$) the R_{SENSE} must be higher than 75 mΩ. The worst-case calculation is shown below using the minimum value of V_{ISNS_LC}:

$$R_{SENSE\ MIN} = \frac{|V_{ISNS\_LC\_MIN}|}{I_{MAXHSSW}} = \frac{45mV}{600mA} = 75m\Omega$$

Equation 2. Minimum R_{SENSE} Calculation

If the voltage reaches the V_{ISNS_LC} limit, the controller enters high-power mode. It turns on the external hotswap switch connected in parallel with the internal hotswap switch, and they share the input current, inversely proportional to its R_{DSON}.

13. Tunable Switching Frequency

The switching frequency of the oscillator is selected by choosing an external resistor R33 connected between the RFREQ and VPOS pins. The following figure will aid in selecting the R_{FREQ} value to achieve the desired switching frequency

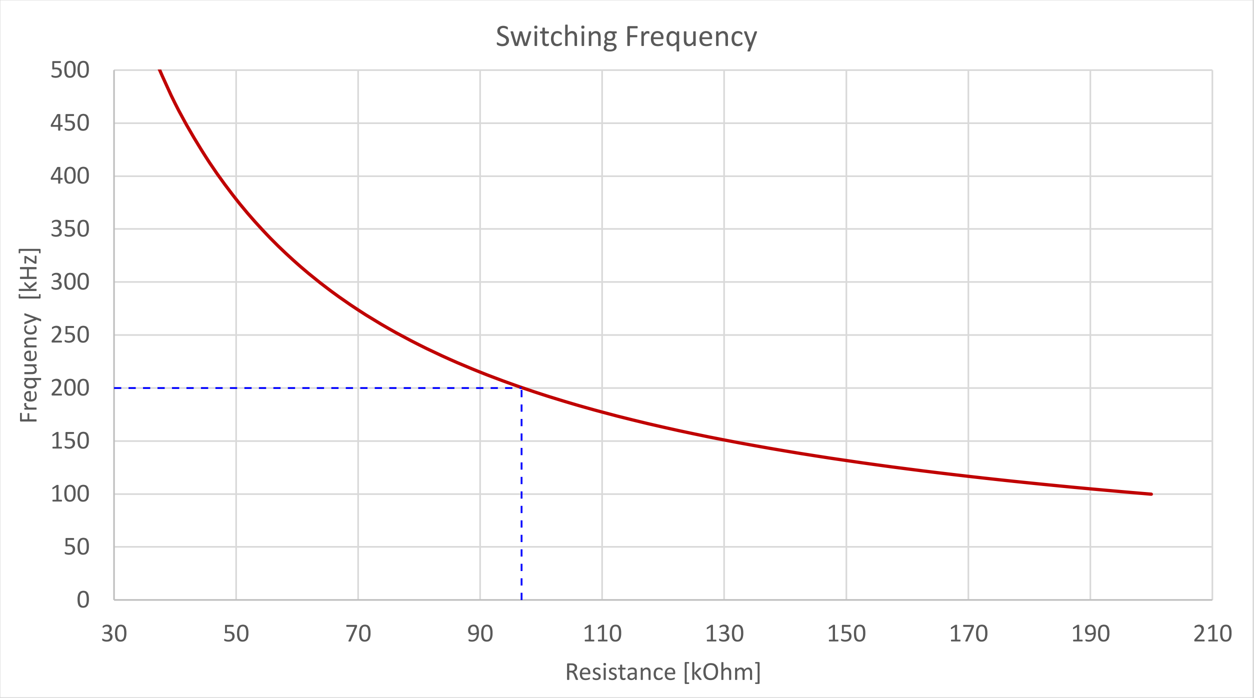


Figure 13.1. Switching Frequency vs. RFREQ

The selected switching frequency for Si34071-FW-12V-C8 is 200 kHz, which is achieved by setting resistor R33 to 95.3 kΩ.

14. Synchronous Rectification

The Si34071-FW-12V-C8 EVB uses self-driven synchronous rectification on the secondary side of the transformer. This eliminates the extra active drive circuit both for the secondary forward switch (U10) and the secondary freewheeling switch (U9). The figure below shows the self-driven synchronous rectification related part of the schematic. The gates of the secondary switches are driven by the secondary winding of the power transformer (T2). The amplitude of the secondary voltage is much higher than needed for direct gate driving, so voltage clamp circuits (Q4-D16-R54-C46 and Q3/D2/R53/C49) are required to protect the gates of U10 and U9 from excessive voltages.

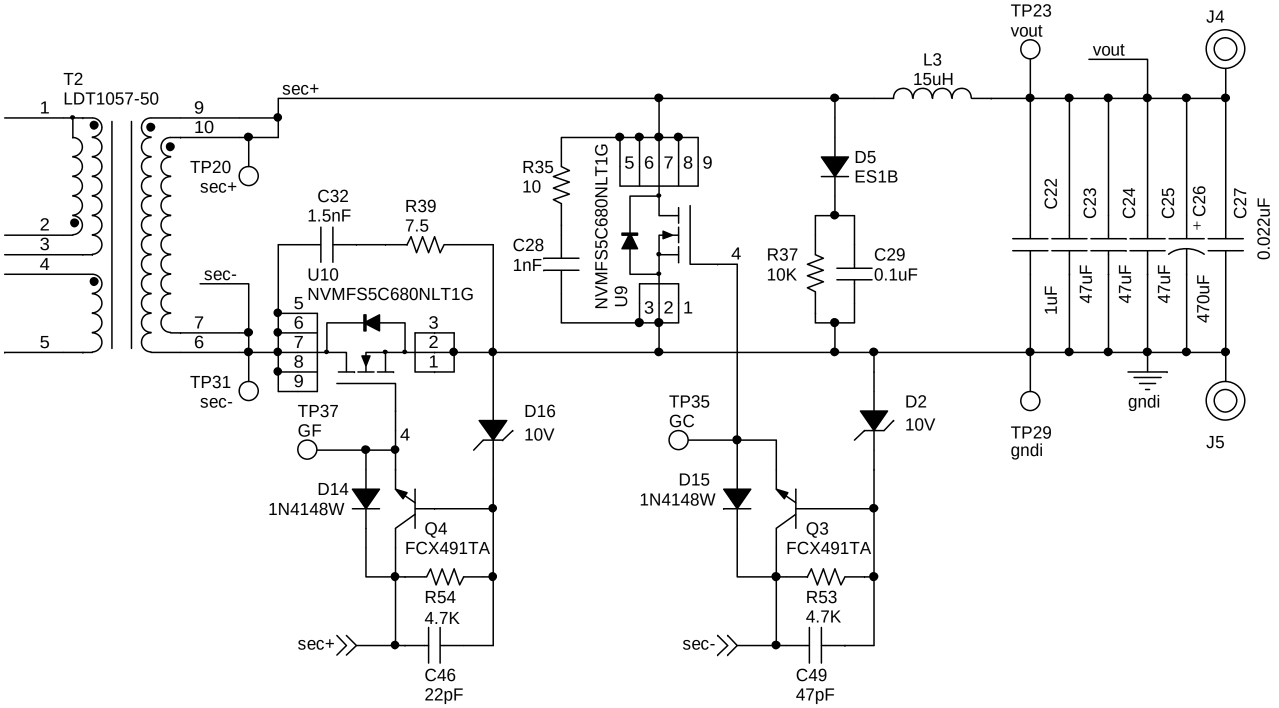


Figure 14.1. Self-Driven Synchronous Rectification

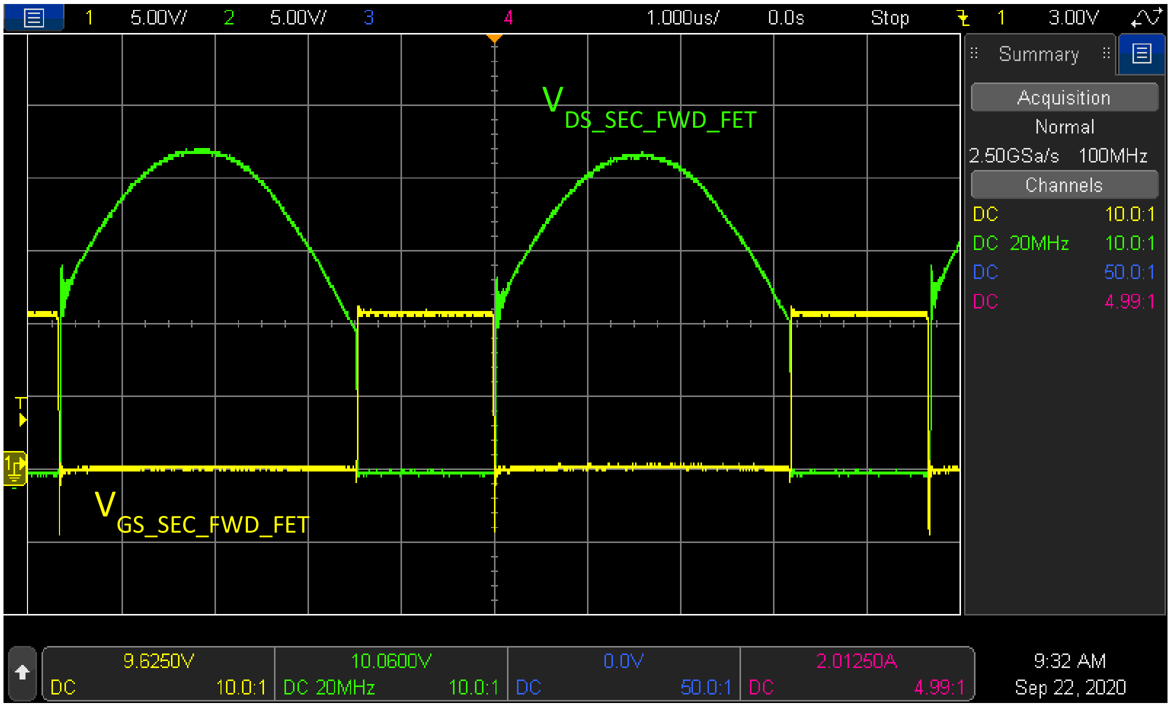


Figure 14.2. Voltages of Secondary Forward Switch (U10) in High-Power Mode

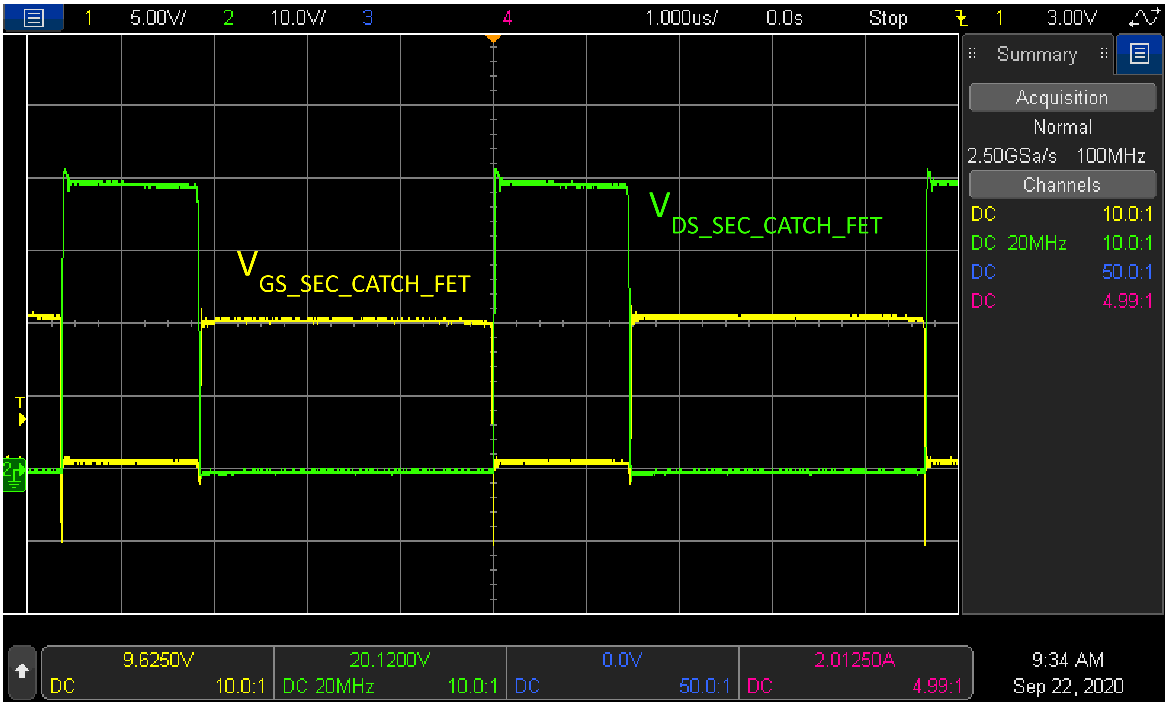


Figure 14.3. Voltages of Secondary Catch Switch (U9) in High-Power Mode

15. Maintain Power Signature

The Si34071-FW-12V-C8 EVB offers both 802.3at and 802.3bt compliant MPS signature generation. For more information, see AN1179.

16. Radiated Emissions Measurement Results—EN55032 Class B

The Si34071-FW-12V-C8 board's radiated emissions, with a 50 V input voltage and full load connected to the output, are shown below. The Si34071-FW-12V-C8 is fully compliant with the international EN 55032 Class B emissions standard.

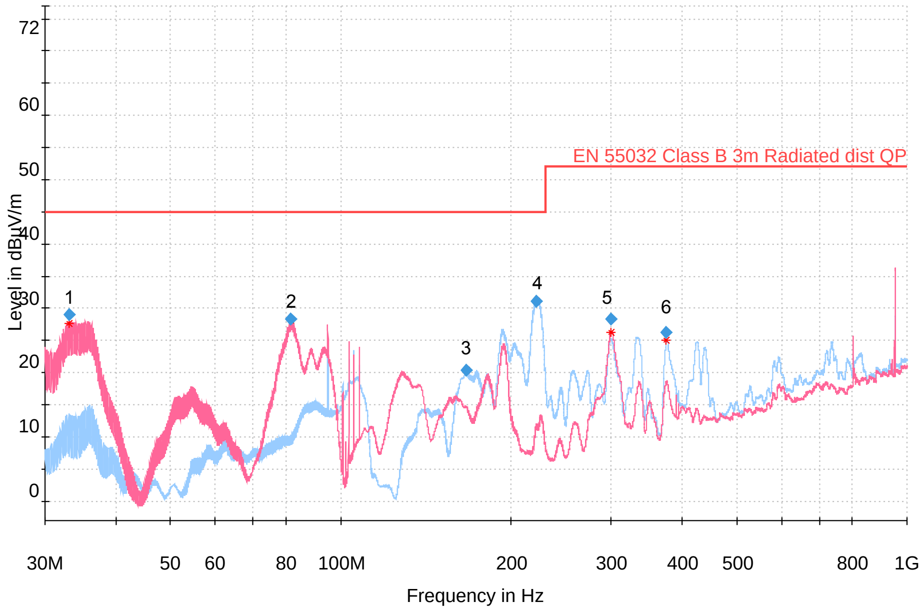


Figure 16.1. Si34071-FW-12V-C8 Radiated Emission Measurement Results

Marker	Frequency (MHz)	Quasi Peak (dBµV/m)	Limit (dBµV/m)	Margin (dB)	Polarization (V/H)
1	33.030000	29.36	40.00	16.04	V
2	81.630000	23.39	40.00	16.61	V
3	166.650000	15.44	40.00	24.56	H
4	220.830000	26.14	40.00	13.86	H
5	300.360000	23.36	47.00	23.64	V
6	375.840000	21.21	47.00	25.79	H

Radiated EMI Measurement Process:

The EVB is measured at full load with peak detection in both vertical and horizontal polarizations. This is a relatively fast process that produces a red curve (vertical polarization) and a blue curve (horizontal polarization).

Next, specific frequencies are selected (red stars) for quasi-peak measurements. The board is measured again at those specific frequencies with a quasi-peak detector, which is a very slow but accurate measurement. The results of this quasi-peak detector measurement are the blue rhombuses.

The blue rhombuses represent the final result of the measurement process. To have passing results, the blue rhombuses should be below the highlighted EN 55032 Class B limit.

17. Conducted Emissions Measurement Results—EN55032

The Si34071-FW-5V-C8 board's conducted emissions have been measured with both peak and average detectors. The following figures show the conducted EMI measurement setup and results.

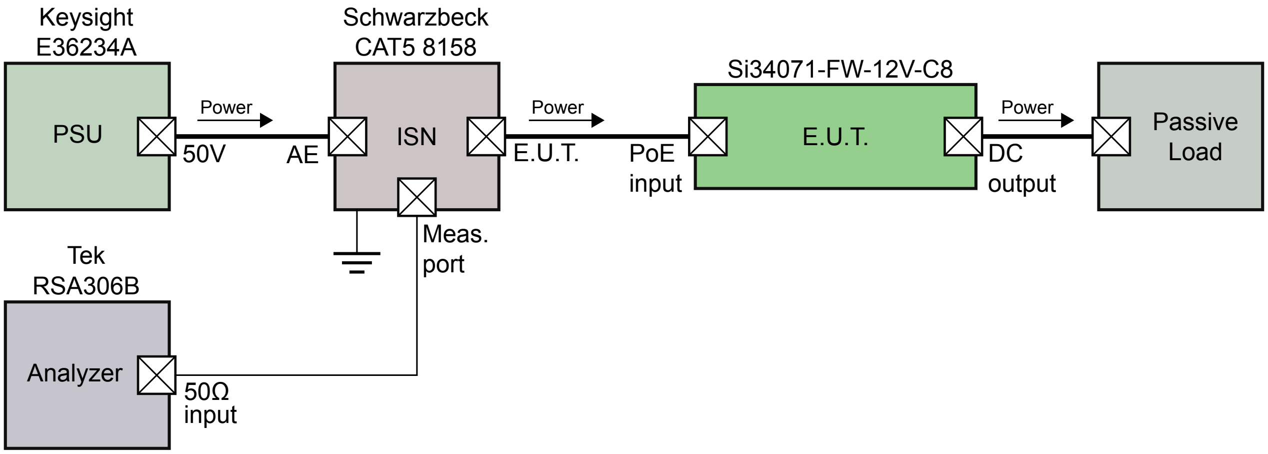


Figure 17.1. Conducted EMI Measurement Setup

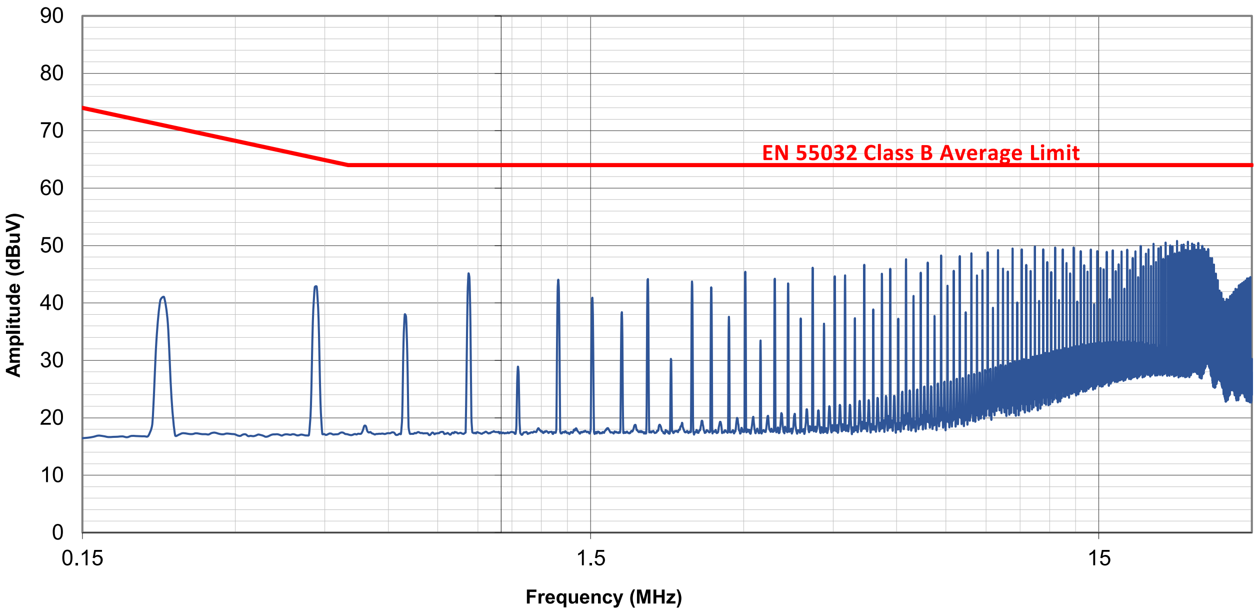


Figure 17.2. Conducted Emissions Measurement on PoE Input, 50 V Input, Full Load, Average Detector

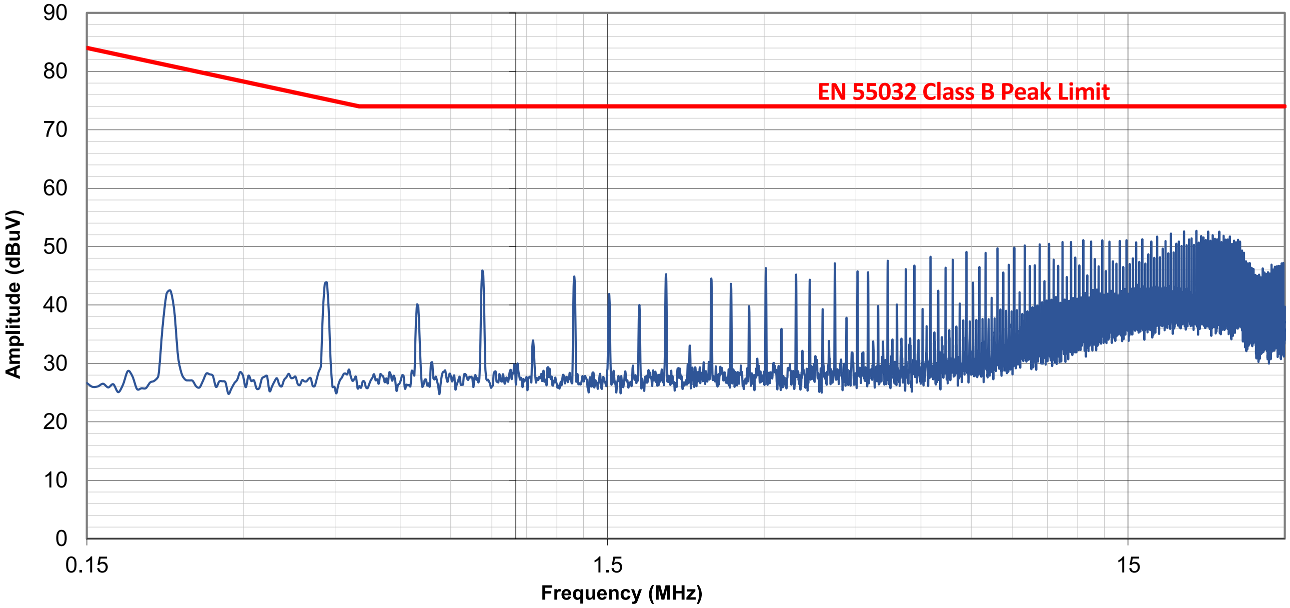


Figure 17.3. Conducted Emissions Measurement on PoE Input, 50 V Input, Full Load, Peak Detector

18. Thermal Measurements

The Si34071-FW-12V-C8 board’s top and bottom side thermal images at 71.3W input power are shown in the following figures.

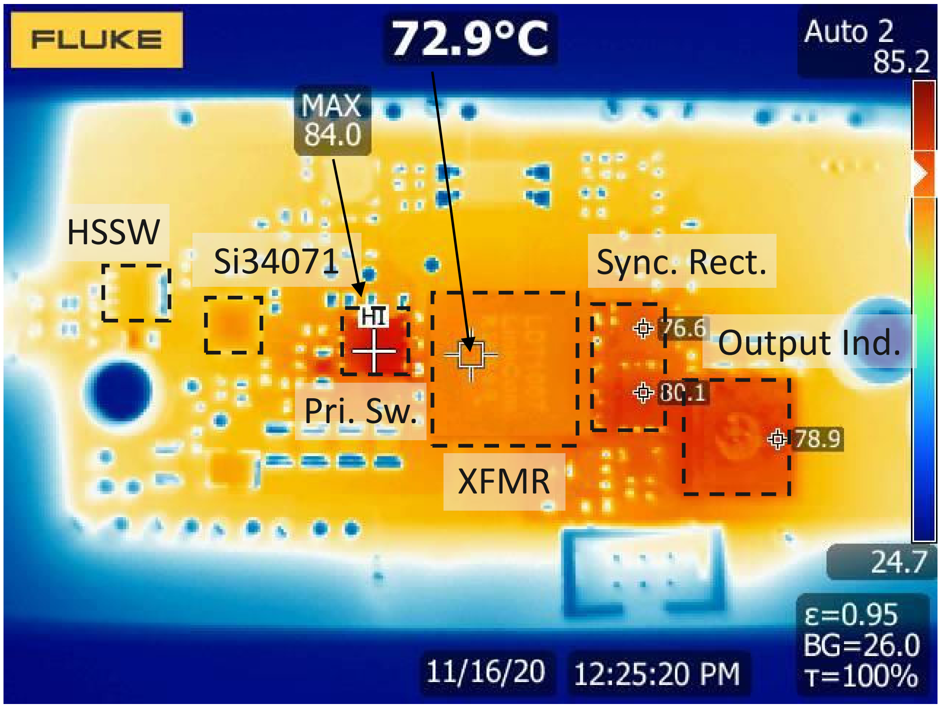


Figure 18.1. Thermal Image of the Top Side, 50 V Input Voltage with 71.3 W Input Power

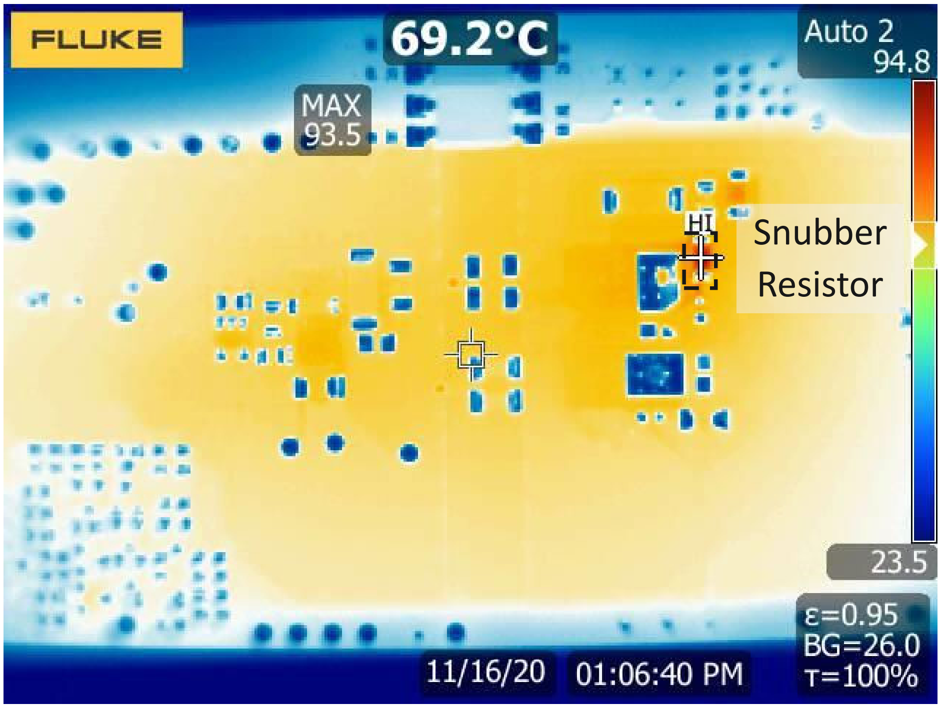


Figure 18.2. Thermal Image of the Bottom Side, 50 V Input Voltage with 71.3 W Input Power

Note: Ambient temperature was 26 °C.

19. Layout

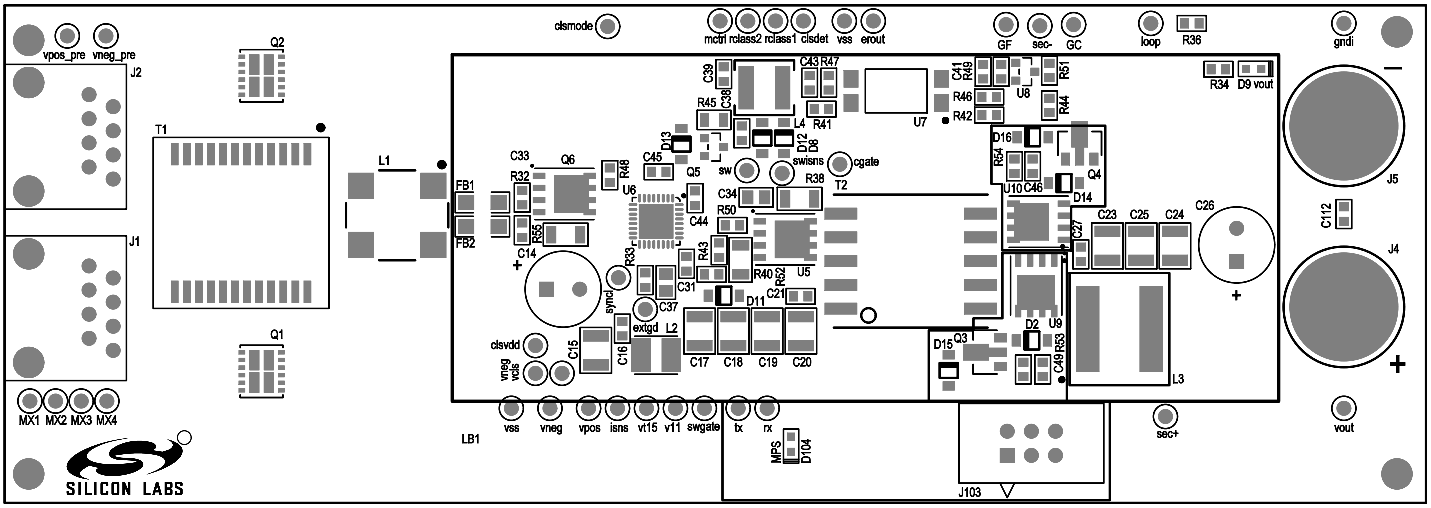


Figure 19.1. Primary Silkscreen

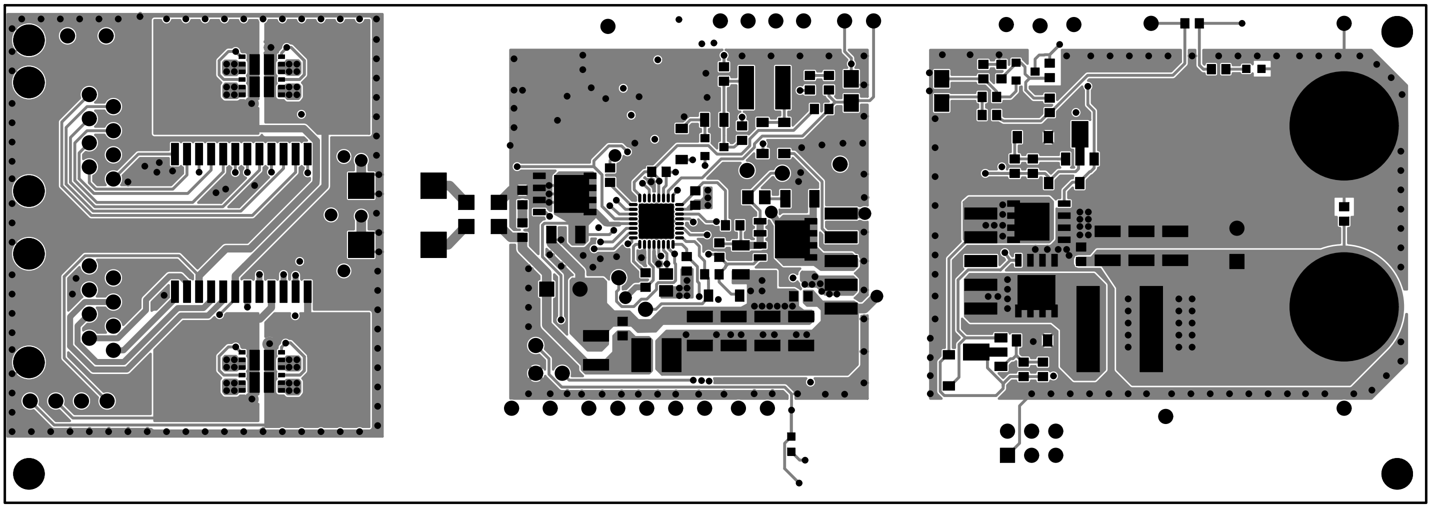


Figure 19.2. Top Layer

Figure 19.3. Internal 1 Layer

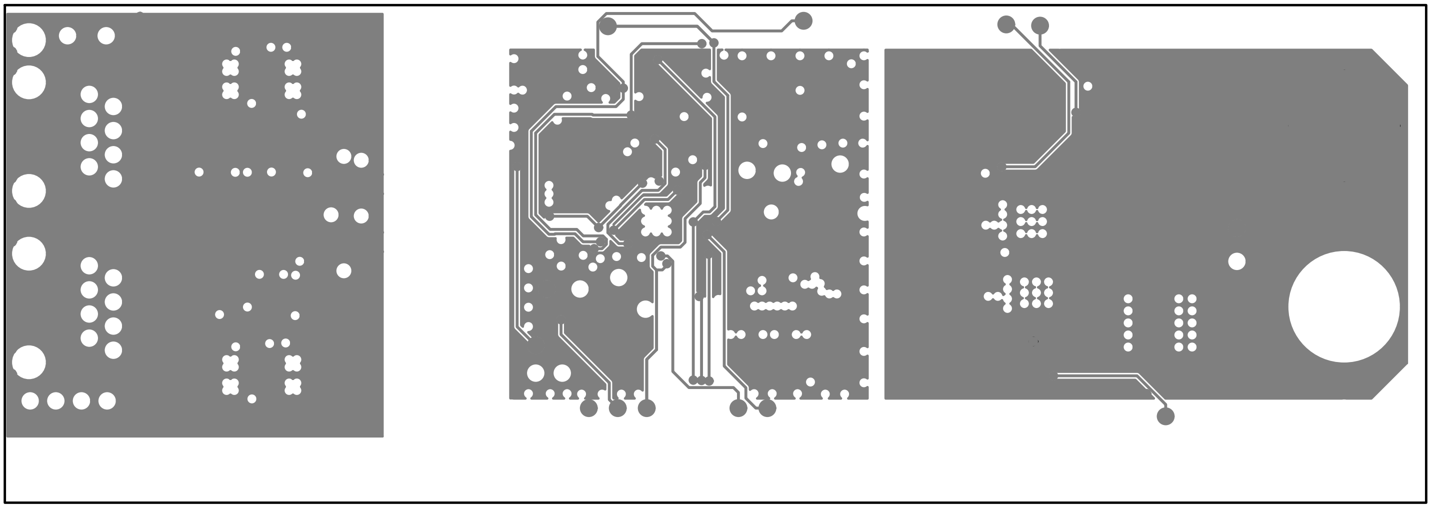


Figure 19.4. Internal 2 Layer

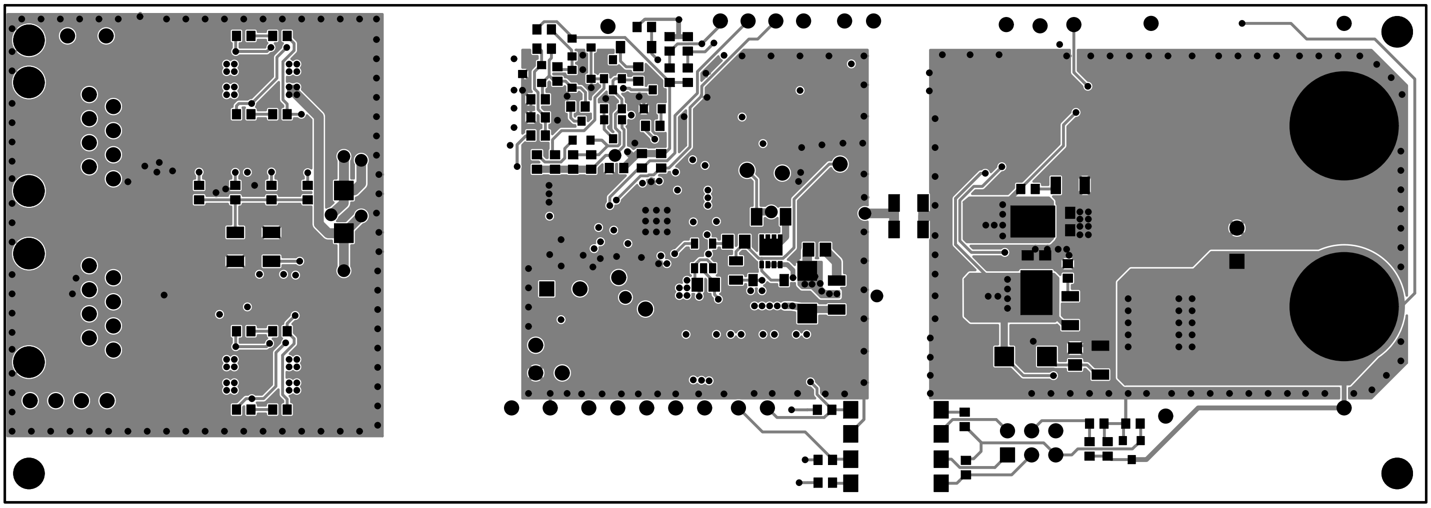


Figure 19.5. Bottom Layer

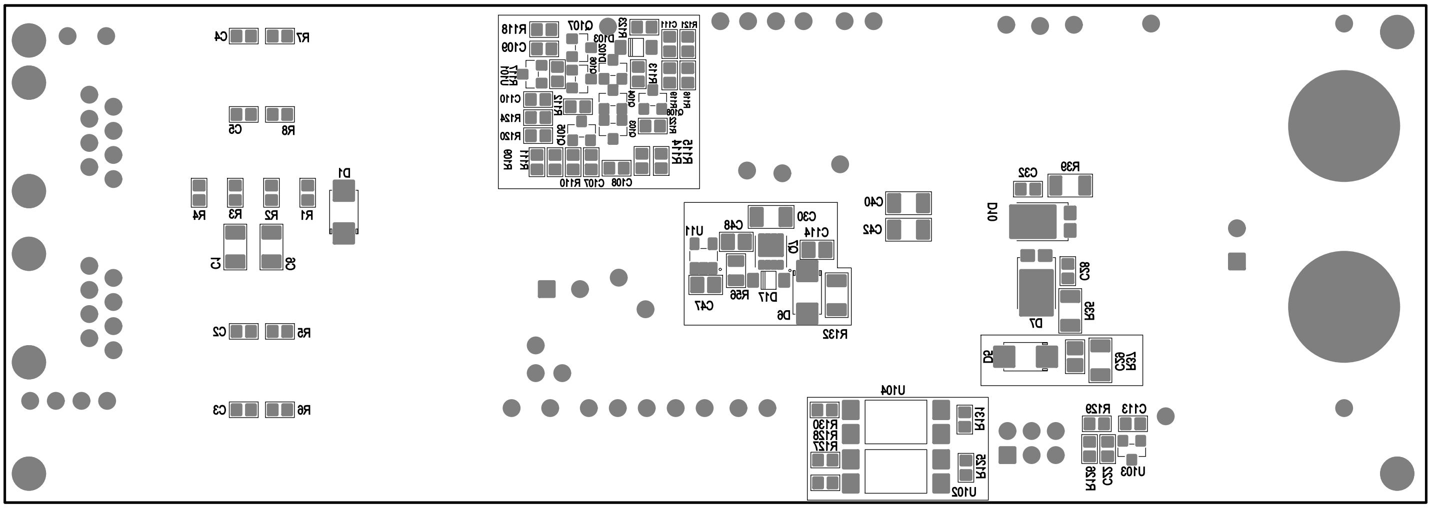


Figure 19.6. Bottom Silkscreen

20. Bill of Materials

Reference Designator	Quantity	Description	Manufacturer	Manufacturer PN
C1, C6, C40, C42	4	1 nF, 2000 V, ±5%, X7R	Kemet	C1206C102JGRACTU
C108	1	0.1 µF, 25 V, ±10%, X7R	Venkel	C0603X7R250-104K
C109	1	1 nF, 100 V, ±10%, X7R	Venkel	C0603X7R101-102K
C111	1	47 pF, 100 V, ±10%, X7R	Venkel	C0603X7R101-470K
C112, C113	2	1 µF, 6.3 V, ±10%, X5R	Venkel	C0603X5R6R3-105K
C14	1	47 µF, 100 V, ±20%, Alu. Electrolytic	Panasonic	ECA2AM470
C15, C17, C18, C19, C20	5	4.7 µF, 100 V, ±10%, X7R	Venkel	C1210X7R101-475KNE
C16, C21, C33	3	0.1 µF, 100 V, ±10%, X7R	Venkel	C0603X7R101-104K
C2, C3, C4, C5, C107, C110	6	0.01 µF, 100 V, ±10%, X7R	Venkel	C0603X7R101-103K
C22	1	1 µF, 16 V, ±10%, X5R	Venkel	C0603X5R160-105K
C23, C24, C25	3	47 µF, 16 V, ±20%, X5R	Venkel	C1210X5R160-476MNE
C26	1	470 µF, 16 V, ±20%, Alu. Electrolytic	Panasonic	ECA1CM471
C27	1	0.022 µF, 50 V, ±20%, X7R	TDK Corporation	C1608X7R1H223M
C28, C44	2	1 nF, 50 V, ±5%, C0G	Venkel	C0603C0G500-102J
C29	1	0.1 µF, 100 V, ±10%, X7R	Venkel	C0805X7R101-104K
C30	1	0.047 µF, 250V, ±10%, X7R	Venkel	C1206X7R251-473K
C31	1	220 nF, 16V, ±5%, X7R	Kemet	C0603C224J4RACTU
C32	1	1.5 nF, 50 V, ±10%, X7R	Venkel	C0603X7R500-152KNE
C37, C47	2	1uF, 50 V, ±10%, X7R	Samsung	CL21B105KBFNNNE
C38	1	2.2 µF, 10V, ±10%, X7R	Venkel	C0603X7R100-225K
C39	1	0.01 µF, 25 V, ±10%, X8R	Kemet	C0603C103K3HACAUTO
C41	1	3.3 nF, 16V, ±10%, X7R	Venkel	C0603X7R160-332K
C43	1	22 nF, 16 V, ±20%, X7R	Venkel	C0603X7R160-223M
C45	1	0.1 µF, 10 V, ±10%, X7R	Venkel	C0603X7R100-104K
C46	1	22 pF, 50 V, ±5%, C0G	Venkel	C0603C0G500-220J
C48	1	0.1 µF, 50 V, ±10%, X7R	Venkel	C0805X7R500-104K
C49	1	47 pF, 50 V, ±5%, C0G	Kemet	C0603C470J5GAC
D102	1	BAV99, 100 V, Dual, Switch	Diodes Inc.	BAV99-7-F
D104	1	LED Yellow	Vishay	TLMY1000-GS08
D13	1	16 V, 16 V, 5%, Zener	On Semi	MMSZ4703T1G
D2, D16, D103	3	10 V, 10 V, 5%, Zener	On Semi	MMSZ4697T1G
D5	1	ES1B, 100 V, Fast	Diodes Inc.	ES1B
D6	1	ES1C, 150 V, Fast	Diodes Inc.	ES1C

Reference Designator	Quantity	Description	Manufacturer	Manufacturer PN
D8, D11, D12, D14, D15, D17	6	1N4148W, 100 V	Diodes Inc.	1N4148W-7-F
D9	1	LED, GREEN	Lumex Inc.	SML-LXFP0603SUGCTR
FB1, FB2	2	Ferrite Bead, 600 Ω,	Würth	742792118
J1, J2	2	RJ-45, Receptacle	Molex	95001-2881
J103	1	3X2 Shrouded Header	3M	30306-6002HB
J4, J5	2	Binding Post	Abbatron HH Smith	101
L1	1	250 µH, 80VDC	Würth	744272251
L2	1	2.2 µH, ±20%, Unshielded	Murata	84222C
L3	1	15 µH, ±20%, Shielded	Coilcraft	XAL1010-153ME
L4	1	1 mH, ±20%, Shielded	Würth	74404054102
Q1, Q2	2	FDMQ8205A, 100V, Bridge Rectifier	OnSemi	FDMQ8205A
Q103, Q104, Q105	3	MMBTA56L, -80V, PNP	On Semi	MMBTA56L
Q106, Q107, Q108	3	MMBTA06LT1, 80V, NPN	On Semi	MMBTA06LT1
Q3, Q4	2	FCX491TA, 60V, NPN	Diodes Inc.	FCX491TA
Q5	1	MMBT3904, 40V, NPN	Fairchild	MMBT3904
Q6	1	SQJ476EP-T1, 100V, N-CH	Vishay	SQJ476EP-T1_GE3
Q7	1	FDMC2523P, -150V, P-CH	Fairchild	FDMC2523P
R1, R2, R3, R4, R5, R6, R7, R8	8	75R, ±0.5%, ThinFilm	Susumu	RR0816Q-750-D
R109	1	3.65 kΩ, ±1%, ThickFilm	Venkel	CR0603-16W-3651FT
R110, R113, R119, R126	4	100 kΩ, ±1%, ThickFilm	Venkel	CR0603-10W-1003F
R111, R112	2	20.0 kΩ, ±1%, ThickFilm	Venkel	CR0603-16W-2002F
R114	1	127R, ±1%, ThickFilm	Venkel	CR0603-10W-1270F
R115	1	255R, ±1%, ThickFilm	Venkel	CR0603-10W-2550F
R116, R122	2	10 kΩ, ±1%, ThickFilm	Venkel	CR0603-16W-1002F
R117, R118	2	49.9 kΩ, ±1%, ThickFilm	Venkel	CR0603-10W-4992F
R120	1	41.2 kΩ, ±1%, ThickFilm	Venkel	CR0603-10W-4122F
R121	1	200 kΩ, ±5%, ThickFilm	Bourns	CR0603-JW-204ELF
R123	1	1.20 kΩ, ±1%, ThickFilm	Venkel	CR0603-10W-1201F
R127	1	330R, ±1%, ThickFilm	Venkel	CR0603-16W-3300F
R128	1	560R, ±1%, ThickFilm	Venkel	CR0603-10W-5600F
R129	1	120 kΩ, ±1%, ThickFilm	Venkel	CR0603-10W-1203F
R32	1	3.0R, ±5%, ThickFilm	Venkel	CR0603-10W-3R0JT
R33	1	95.3 kΩ, ±1%, ThickFilm	Venkel	CR0603-16W-9532F
R34, R125, R130, R131	4	1 kΩ, ±1%, ThickFilm	Venkel	CR0603-10W-1001F

Reference Designator	Quantity	Description	Manufacturer	Manufacturer PN
R35	1	10R, ±1%, ThickFilm	Venkel	CR1206-4W-10R0F
R36, R40	2	10.0R, ±1%, ThickFilm	Venkel	CR0603-16W-10R0F
R37	1	10 kΩ, ±5%, ThickFilm	Venkel	CR1206-4W-103J
R39	1	7.5R, ±5%, ThickFilm	Venkel	CR1206-8W-7R5JT
R41	1	3.24 kΩ, ±1%, ThickFilm	Venkel	CR0603-10W-3241F
R42	1	2.15 kΩ, ±1%, ThickFilm	Venkel	CR0603-10W-2151F
R43	1	24 kΩ, ±1%, ThickFilm	Panasonic	ERJ-3EKF2402V
R44	1	36.5 kΩ, ±1%, ThickFilm	Venkel	CR0603-16W-3652F
R45	1	3.3 kΩ, ±1%, ThickFilm	Venkel	CR0805-10W-3301F
R47, R49	2	0R	Venkel	CR0603-16W-000
R48, R124	2	24.9 kΩ, ±1%, ThickFilm	Venkel	CR0603-10W-2492F
R50	1	100R, ±1%, ThickFilm	Venkel	CR0603-10W-1000F
R51	1	4.12 kΩ, ±1%, ThickFilm	Venkel	CR0603-10W-4121F
R52	1	0.039R, ±1%, ThickFilm	Panasonic	ERJ-8CWFR039V
R53, R54	2	4.7 kΩ, ±5%, ThickFilm	Venkel	CR0603-10W-472J
R55	1	0.1R, ±1%, ThickFilm	Venkel	LCR1206-R100F
R56	1	10 kΩ, ±1%, ThickFilm	Venkel	CR0805-8W-1002F
T1	1	LAN Transformer	Würth	7490220122
T2	1	LDT1057-50, 12 V/6 A, FORWARD	LinkCom	LDT1057-50
U103	1	AP2210N-3.3, 3.3V, LDO	Diodes Inc.	AP2210N-3.3TRG1
U11	1	FAN3100CSX, Gate Driver	ON Semiconductor	FAN3100CSX
U5	1	FDMS86200, 150V, N-CH	ON Semiconductor	FDMS86200
U6	1	Si34071, PD Controller	Silicon Labs	Si34071-A01-GM
U7, U102, U104	3	Optocoupler	Vishay	FOD817C3SD
U8, U101	2	Shunt Regulator	TI	TLV431BCDBZR
U9, U10	2	NVMFS5C680NLT1G, 60V, N-CH	ON Semi	NVMFS5C680NLT1G
Not Installed Components				
C34, C114	2	820 pF, 200 V, ±10%, C0G	Venkel	C0805C0G201-821KNE
D1	1	TVS, 400 W, 58 V	Littelfuse	SMAJ58A
D7, D10	2	Schottky, 10 A, 40 V	Diodes Inc.	PDS1040-13
R132	1	10R, 1/4 W, ±1%, ThickFilm	Venkel	CR1206-4W-10R0F
R38	1	6.8R, 1/8 W, ±5%, ThickFilm	Venkel	CR1206-8W-6R8J
R46	1	1 kΩ, 1/10 W, ±1%, ThickFilm	Venkel	CR0603-10W-1001F

21. Si34071-FW-12V-C8 Design and Layout Checklist

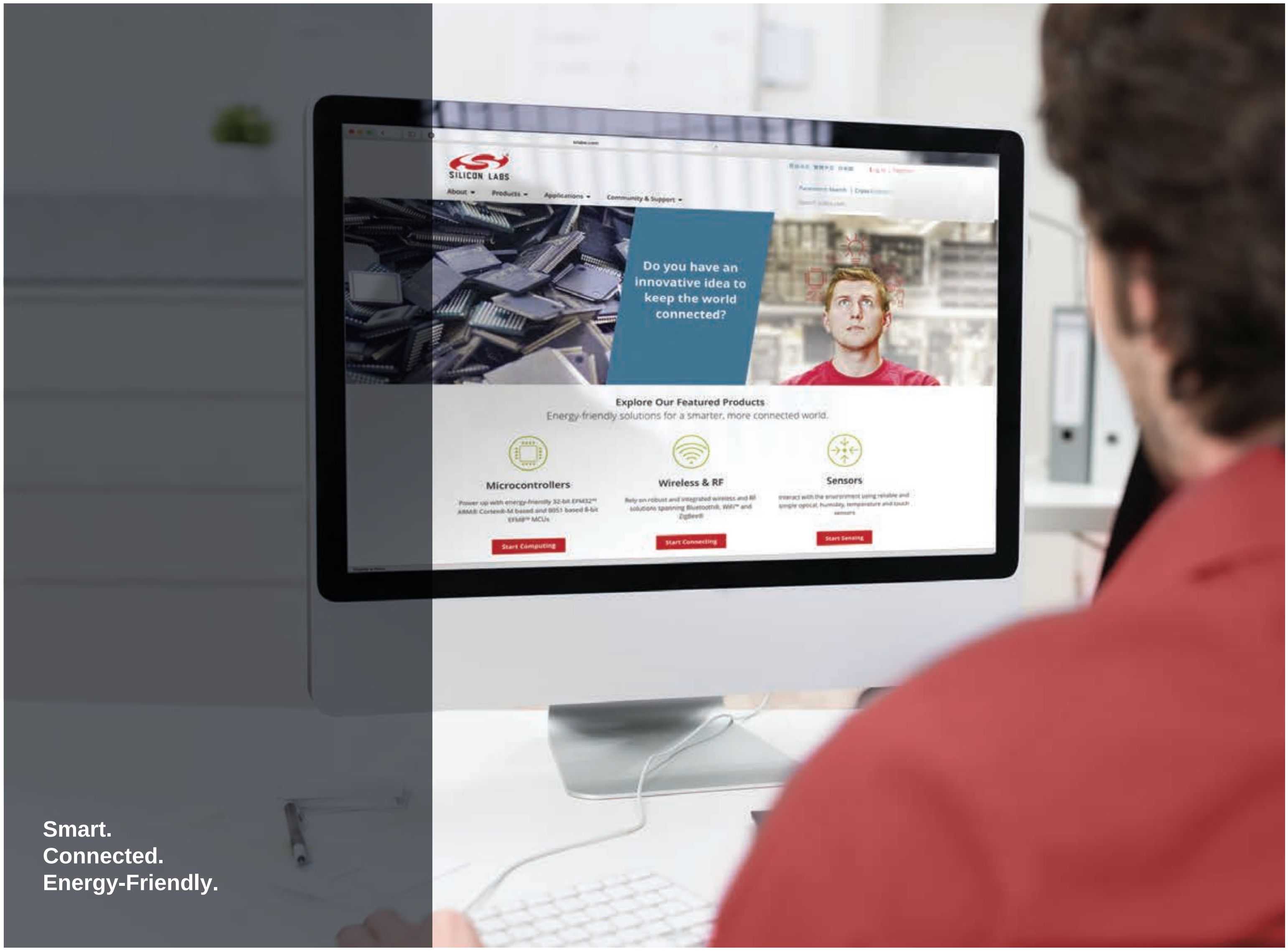
The complete EVB design databases are located at www.silabs.com/PoE link. Silicon Labs strongly recommends using these EVB schematics and layout files as a starting point to ensure robust performance and avoid common mistakes in the schematic capture and PCB layout processes.

Below is a recommended design checklist that can assist in trouble-free development of robust PD designs.

Refer also to the Si34071 data sheet and AN1130: Si3404/06x PoE-PD ControllerDesign Guide when using the following checklist.

1. Design Planning checklist:
    a. Determine if your design requires an isolated or non-isolated topology. For more information, see AN1130.
    b. Silicon Labs strongly recommends using the EVB schematics and layout files as a starting point as you begin integrating the Si34071 into your system design process.
    c. Determine your load’s power requirements (i.e., VOUT and IOUT consumed by the PD, including the typical expected transient surge conditions).
    d. Based on your required PD power level, select the appropriate class resistors (R114, R115) value by referring to AN1179.
2. General Design Checklist:
    a. Non-standard PoE injectors turns on the PD without detection and classification phases. In most cases, dV/dt is not controlled and could violate IEEE requirements. To ensure robustness with those injectors, please include a 3Ω resistors in place of R32.
    b. If industrial temperature range (−40..+85°C) of operation is required then some components need to be replaced. For stable operation at low temperatures up to −40°C, change the following parts in your design: C26 aluminum electrolytic capacitor with an aluminum polymer capacitor (for example: Würth Elektronik 870025374007), do not populate C43 and R47 and if the input rectifiers are FET bridges install low-leakage Schottky diodes (for example BAT46ZFILM) in parallel with the FETs body diode as noted in AN1179. At the high temperature range, up to +85°C, detection resistance R48 change may be needed, for more information, see "AN1179: Si34071 802.3bt PD PoE Interface".
3. Layout Guidelines:
    a. Make sure VNEG pin of the Si34071 is connected to the backside of the QFN package with an adequate thermal plane.
    b. Use solid primary side VSS plane under switching circuits to make a low impedance return path. A solid VSS plane can greatly reduce the radiated emission of the board.
    c. Keep the trace length from the switching FET to VSS as short as possible. Make all of the power (high current) traces as short, direct, and thick as possible. It is a good practice on a standard PCB board to make the traces an absolute minimum of 15 mils (0.381 mm) per ampere.
    d. Usually, one standard via handles 200 mA of current. If the trace needs to conduct a significant amount of current from one plane to the other, use multiple vias.
    e. Keep the high di/dt circular area of the loop from the primary forward FET to the transformer and returning from the input filter capacitors (C17..C21) to VSS as small a diameter as possible. Also, minimize the high di/dt circular area of the loop from the output of the transformer to the self-driven synchronous rectifier FETs (U9 and U10) as small as possible. If possible, keep the direction of current flow in these two loops the opposite.
    f. Keep the high-power traces as short as possible.
    g. Keep the feedback and loop stability components as far from the transformer and noisy power traces as possible.
    h. If the outputs have a ground plane or positive output plane, do not connect the high current carrying components and the filter capacitors through the plane. Connect them together, and then connect to the plane at a single point.

To help ensure first-pass success, contact our customer support by submitting a help ticket and uploading your schematics and layout files for review.



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