Si3473/72 Data Sheet

Octal or Quad 2-pair 802.3bt Ethernet Port PoE PSE Controller

The Si3473 and Si3472 are fully programmable, 50 V to 57 V power sourcing equipment (PSE) controllers for IEEE 802.3bt 2-pair, Type 3 applications. As 2-pair, Type 3 PSE controllers, Si3473/72 are compatible with IEEE 802.3af and IEEE 802.3at powered device (PD) loads. Designed for use in PSE endspans (switches) and midspans (injectors), the Si3473/72 integrates eight (Si3473) or four (Si3472) independent ports, each with the IEEE-required detection and classification functionality.

In addition, the Si3473/72 features include powered device (PD) disconnect using dc-sense algorithms, a robust multipoint detection algorithm, software configurable per-port current and voltage monitoring, and programmable current limits to support the IEEE 802.3af, 802.3at, and 2-pair 802.3bt standards. Intelligent power protection circuitry includes input undervoltage detection, output power limit, and short-circuit protection. The Si3473/72 operates autonomously or by host processor control through a two wire, I^2C-compatible serial interface. An interrupt pin is used to alert a host processor of various status and fault events.

Applications

- IEEE 802.3af, 802.3at, and 2-pair 802.3bt Power Sourcing Equipment (PSE)
- Power over Ethernet Switches
- IP Phone Systems
- Smartgrid Switches
- Ruggedized and Industrial Switches
- Multiport PoE Injectors
- Applications powering IEEE Type 1 & 2 PDs through Class 4 up to 30 W
- Applications powering legacy 2-pair Class 5 PDs to 45 W

KEY FEATURES

- Octal or Quad Port Power Sourcing Equipment (PSE) controller
- IEEE 802.3bt 2-pair, Type 3 compliant
- IEEE 802.3af and IEEE 802.3at compatible
- Autonomous or I^2C host interface
- Emergency Shutdown support with port priority control
- Adds enhanced features for maximum design flexibility:
  - Per-port current and voltage monitoring
  - Multi-point detection
  - Programmable power MOSFET gate drive control
  - Configurable watchdog timer enables failsafe operation
- Maskable interrupt pin
- Comprehensive fault protection circuitry includes:
  - Power undervoltage lockout
  - Output current limit and short-circuit protection
  - Thermal overload detection
- Extended operating temp range: –40 to +85 °C
- 38-pin 5 x 7 mm QFN package (Si3472)
- 56-pin, 8 x 8 mm QFN package (Si3473)

1. Ordering Guide

Table 1.1. Si3473/72 Ordering Guide

Ordering Part Number[1]	Product Revision	Current Sense Resistor[2]	Package	Temperature Range (Ambient)
Si3473A-A01-IM	A01	255 mΩ	56-pin, 8 x 8 mm QFN RoHS-compliant	–40 to 85 °C
Si3473B-A01-IM	A01	200 mΩ	56-pin, 8 x 8 mm QFN RoHS-compliant	–40 to 85 °C
Si3472A-A01-IM	A01	255 mΩ	38-pin, 5 x 7 mm QFN RoHS-compliant	–40 to 85 °C
Si3472B-A01-IM	A01	200 mΩ	38-pin, 5 x 7 mm QFN RoHS-compliant	–40 to 85 °C

Note:

1. Add an “R” to the end of the part number for tape and reel option (e.g., Si3473/72A or Si3473/72A-A01-IMR).
2. Options include industry-standard 255 mΩ or more thermally efficient 200 mΩ sense resistor.

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2. Functional Description

2.1 Overview

The Si3473/2 integrates a high-performance microcontroller with high-resolution A/D and D/A capabilities, and independent, high-voltage PSE port interfaces. External power FETs and sense resistors are used to power the PoE ports, communicate to a PD, and sense the current and voltage levels on the ports. The Si3473/72 enables an extremely flexible solution for virtually any PoE switch application. The Si3473/72 contains all PSE controller functions needed for an octal (Si3473) or quad (Si3472) port PoE design.

The Si3473/72 includes many additional features that can be individually enabled or disabled by programming the extended register set appropriately:

- Per-port current / voltage monitoring and measurement
- Multipoint detection algorithms
- Programmable gate drive for external MOSFETs
- Watchdog timer (WDT)

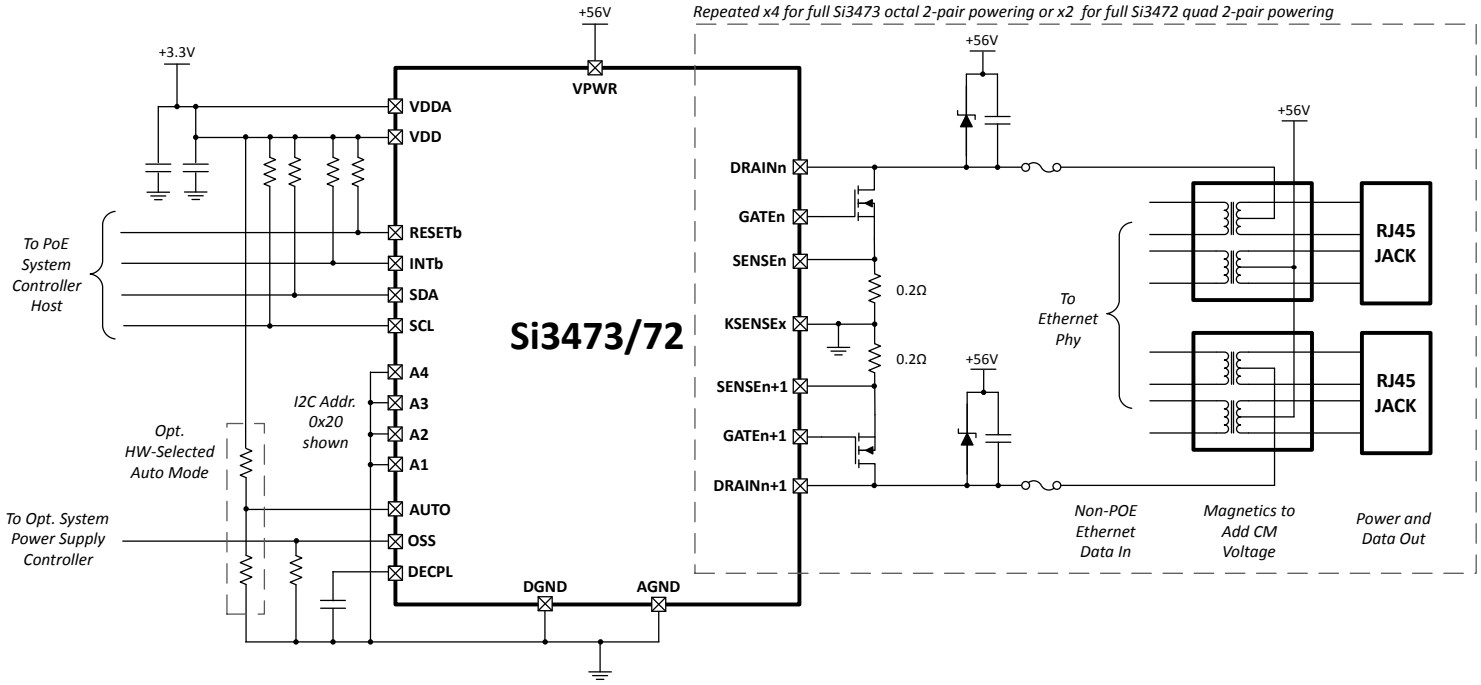


Figure 2.1. Si3473/72 Typical Application Circuit

2.2 Functional Block Diagram

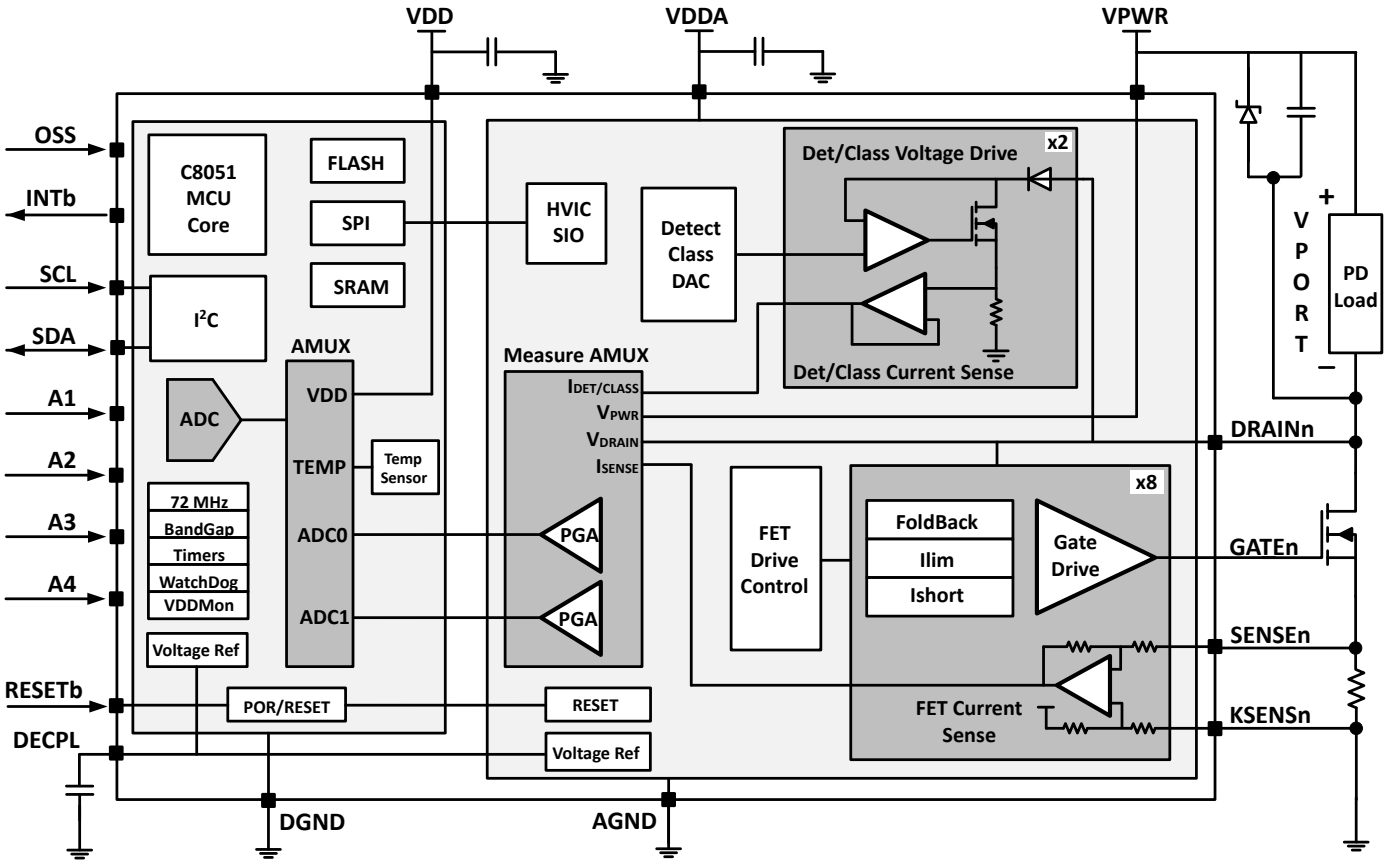


Figure 2.2. Si3473/72 Functional Block Diagram

2.3 Operational Modes

The Si3473/72 has three different operating modes: Autonomous, Semi-Autonomous, and Manual, plus one non-operating mode, Shutdown. The operating mode can be selected based on system requirements, such as whether the PSE system is power-constrained, whether the PSE system has a power manager host, or whether the PSE system must identify and power up non-compliant PD loads.

2.3.1 Autonomous Mode

Autonomous Mode should only be used in PSE systems where there is enough power to power all ports simultaneously to their total allocated power. Autonomous Mode can only be used in non-power constrained PSE systems. In Autonomous Mode, the Si3473/72 will automatically detect, classify and power on ports that present a valid PD signature without any external host interaction.

There are two methods to place the Si3473/72 into Autonomous Mode. One method is to power cycle the Si3473/72 while applying a voltage (other than VDD) on the AUTO pin. When using this method, the power allocation set by the AUTO pin applies to each port. The system must have sufficient VPWR current to handle the worst case where all ports are each supplying maximum PD current load. A requirement for AUTO pin Autonomous Mode is that each port must have the same Power Allocation setting.

The second method is to configure and start the Autonomous Mode through the I²C registers. Use this method to configure and invoke the Autonomous Mode for systems that have ports with different power allocation settings or dynamic power allocation settings. Whether Autonomous Mode is invoked by the AUTO pin or by the I²C interface, the I²C register interface remains active so an external host processor can poll the event registers, for example, to control indicator LEDs.

For more details on autonomous operation, refer to 2.10.1 AUTO Pin Autonomous Mode and 2.10.2 I²C Autonomous Mode.

2.3.2 Semi-Autonomous Mode

In PSE systems with high port counts, it is common to have more ports than the system power supply can power simultaneously. In Semi-Autonomous Mode, the Si3473/Si3472 I2C register interface allows a host processor to power or deny PD power requests as new PD loads are attached. In these systems, the Si3473/72 controller performs low level PoE protocols with PD power loads and provides real-time fault monitoring and power consumption measurements required by an external host processor to perform power management.

2.3.3 Manual Mode

Manual Mode allows an external host processor to force a condition on the port(s) that bypasses the PoE protocol. For example, a host can use Manual Mode to force a port to power on a PD load immediately without exercising Detection and Classification protocol. Because of this behavior, Manual Mode should be used for diagnostic or debug purposes only.

2.4 Host Interface

The Si3473/72 communicates with a host through an I^2C interface using:

- Registers
- Events
- Pushbuttons

In this data sheet, register names, fields, and bits are listed in all capitals. Some have prefixes such as PORTn_ or PORTnm_. The PORTn_ describes attributes that are associated with 2-pair (2P) ports. The Si3473 only supports 2-pair port configurations. The Si3474 can be configured for 4-pair port configurations. Some registers are associated with one set of four 2-pair ports (quad). The Si3473 has two quads and the second set of four 2-pair ports are accessed in the same register but through the alternate I^2C address. The Si3472 has one quad. Refer to 3. Register Map for a complete listing of registers.

During operation, the Si3473/72 monitors global conditions such as temperature and supply voltage, and some conditions that are associated with the individual PoE ports. When an event occurs, the Si3473/72 will drive the INTb pin low. A host will then read the INTERRUPT register and decode what event has occurred. The Si3473/72 drives the INTb low until the appropriate Clear-on-Read (CoR) register is read by a host.

Some events cause the Si3473/72 to take immediate action without instructions from a host. Other events notify a host that a change has occurred and allow a host to determine how to handle the event. Once a host receives notification of an event, it is expected to act upon that event. The details and mechanics of event handling are described in 2.9 Event Handling.

A host can instruct the Si3473/72 to take certain actions through a Pushbutton (PB) command. All write-only registers are Pushbutton registers. A register designated as Pushbutton will always return zero when read.

Each Si3473/72 port can be in one of four operational Modes, controlled by the PORT_MODE register. PORTn_PORT_MODE can be set to:

- SHUTDOWN
- MANUAL
- SEMI_AUTO
- AUTO

The AUTO Mode is most applicable to a non-hosted PSE system. The MANUAL Mode is used primarily for diagnostic and debug purposes. For hosted PSE systems, SHUTDOWN and SEMI_AUTO port Modes are the most important. When PORTn_PORT_MODE is set to SHUTDOWN, that port is in an idle state, ready to be configured by a host.

A port enters SHUTDOWN by:

- A hard reset (power on reset or by deasserting the RESETb pin)
- Setting RESET_QUAD in the PB_RESET register to set all ports in that quad to SHUTDOWN
- Setting individual PORTn_RESET_PORT bits in PB_RESET register. Each port has a dedicated bit
- Any SUPPLY_EVENT
- An I^2C WATCHDOG event (equivalent to a RESET_QUAD)

A port in SEMI_AUTO Mode, when combined with PORTn_DETECT_ENABLE and PORTn_CLASS_ENABLE, instructs the Si3473/72 to actively look for connected PDs on a port. In a power-managed, hosted PSE system, the figure below describes the key interactions and events between a host and the PoE port conditions in the Si3473/72. The following sections describe the control flow of a Semi-Auto PSE.

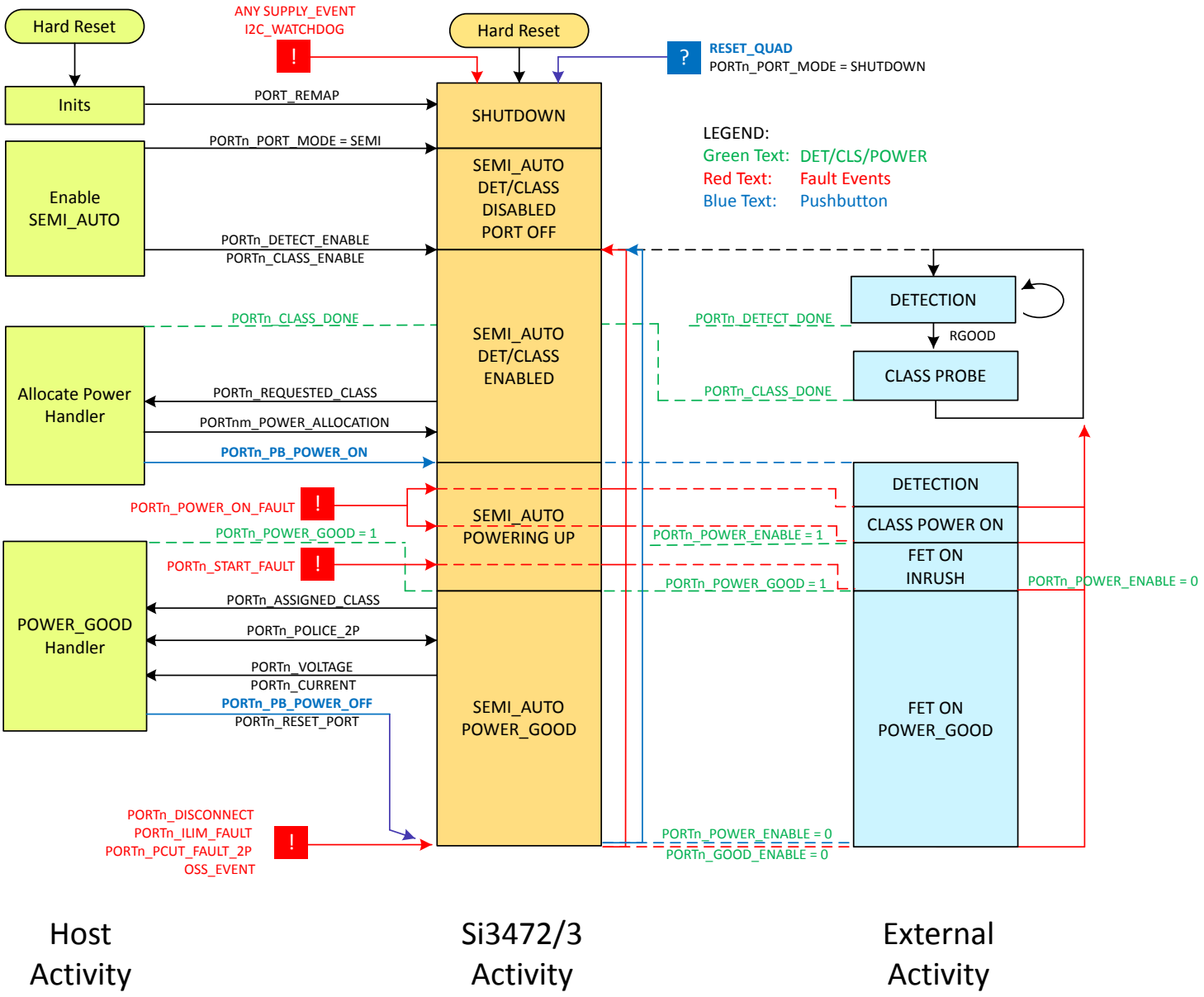


Figure 2.3. Semi-Auto System State Diagram

2.5 Reset and Initialization

Hard resets are invoked by either cycling power (Power on Reset or PoR) and/or deasserting the RESETb input. After a hard reset, all registers are set to default values. A PoR will always set all registers to default values. Invoking a hard reset by deasserting the RESETb input will set all registers to default values except the upper nibble of SUPPLY_EVENT. The upper nibble is sticky until the condition that is causing the global event is cleared. For specific information, refer to 3.7 SUPPLY_EVENT and SUPPLY_EVENT CoR (0x0A, 0x0B).

Immediately after a hard reset, a host must initialize the PORT_REMAP register. For specifics, refer to 3.23 PORT_REMAP (0x26). Once written to, this register is locked until a hard reset of the Si3473/72 unlocks it again.

During initialization, a host sets other global registers as needed.

Note that there is an important difference between the Si3472 and Si3473 pertaining to how RESETb affects powered ports. A powered port on the Si3473 powers down within 20 us after the FALLING edge of RESETb. On the other hand, a powered port on the Si3472 powers down within 300 us after the RISING edge of RESETb.

2.6 Semi-Auto Detection and Class Probe

A host instructs the Si3473/72 to start detecting attached PDs by setting:

- PORTn_PORT_MODE = SEMI_AUTO
- PORTn_DETECT_ENABLE and PORTn_CLASS_ENABLE in DETECT_CLASS_ENABLE

Prior to driving the Detection waveform, the Si3473/72 checks that the port's external FET is properly off and is not damaged. The first test is a current measurement across the external sense resistor and the second test is a voltage measurement at the DRAINx pin. If excessive current or an unexpected drain voltage is detected, PORTn_DETECTION_STATUS will indicate a MOSFET_FAULT and Detection is aborted.

The Si3473/72 detects a PD by making a differential resistance measurement. To do this, the Si3473/72 drives 4 V (V_{det1}) to 8 V (V_{det1}) and back to 4 V on each enabled port through the DRAINx pin, while measuring current at each step. The results are used to calculate the Detection resistance, also known as the PD Signature Resistance, which is nominally 25 kΩ. The Si3473/72 reports the Detection results in the PORTn_DETECTION_STATUS field of the PORTn_DETECT_CLASS_STATUS registers.

During Detection, the Si3473/72 monitors the voltage driven for evidence of contention with another PSE driving the same line. If the measured voltage deviates significantly from the driven voltage, PORTn_DETECTION_STATUS will report a PSE to PSE fault. The Si3473/72 also uses the voltage/current measurements taken during the Detection waveform to determine if the PD Signature Resistance is too capacitive and reports this in the PORTn_DETECTION_STATUS.

A DETECT_DONE event will be reported to a host after the Detection sequence. If the Detection result is RGOOD, the Si3473/72 begins a Class Probe to determine the PD's Class Signature. A Class Probe will always consist of three class "fingers" to determine the PD requested power followed by a Class Reset. Three fingers are used to support Class 5 legacy PDs. The following figure shows the expected waveform with the aforementioned three fingers for a 2-pair powered PD.

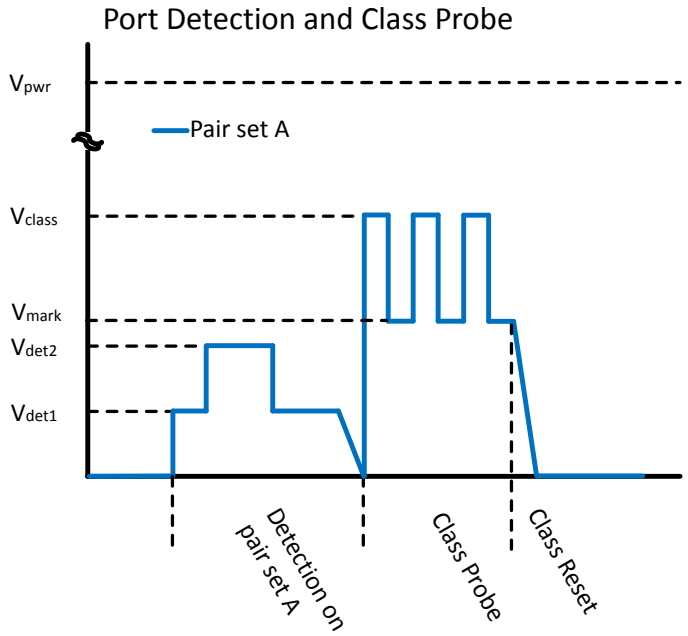


Figure 2.4. Port Voltage During Semi-Auto DET/CLASS 2-Pair Waveform

2.7 Powering Up

A port is ready to be powered on after PORTn_CLASS_DONE event is reported. A host can examine the results of PORTn_CLASS_STATUS to discover the PD's requested class. A host can then set or adjust PORTnm_POWER_ALLOCATION as needed, followed by setting the PORTn_PB_POWER_ON for the port. The Si3473/72 goes through this sequence of events as described in the following subsections.

2.7.1 Power Demotion

Before powering on a port, a host can determine how much power the PD has requested by reading the PD's requested class. If a host determines that it has the requested power available, it will typically set PORTnm_POWER_ALLOCATION so that the PD receives the power it has requested. If a host knows it does not have the full power available, it can choose to set the PORTnm_POWER_ALLOCATION such that the assigned class will be less than the requested class; this is known as Power Demotion.

A power-demoted PD can request more power at any time through the Ethernet Link Layer Discovery Protocol (LLDP). Through LLDP, if the PD requests additional power (and if the PSE has more power to spare at that time), it can then grant the additional power. A host communicates the allowable additional power to the Si3473/72 by updating the PORTn_POLICE_2P registers and need not put the port into SHUTDOWN or perform another PORTn_PB_POWER_ON sequence.

When a Class 4 PD is only provided Class 3 power, the PSE will only send one Classification finger to the PD. In this case, the Si3473/72 will supply Class 3 power and report "Class 4 Type 1 Limited" in PORTn_CLASS_STATUS. PORTn_ASSIGNED_CLASS will show Class 3, and PORTn_REQUESTED_CLASS will show the result of the Class Probe, which will be Class 4.

It is important to note that Power Demotion can only occur from Class 4 to Class 3. There is no demotion strategy to lower classes.

2.7.2 Final Detection and Class Probe

When a PORTn_PB_POWER_ON command is received by the Si3473/72, it is likely to be performing a DET/CLASS PD discovery sequence that is unrelated to the port receiving the PB_POWER_ON pushbutton. The Si3473/72 allows those started sequences to complete before executing the Pushbutton command for the specified port. PB_POWER_ON performs a final set of Detection and "Class Power On" operations for the ports that a host wants to power on. The Class Power On sequence is described in the next section.

The PB_POWER_ON Detection sequence is similar to that performed by Semi-Auto Detection and Class Probe, with some slight differences. If the Detection results are anything other than RGOOD for the ports being powered up, the PORTn_POWER_ON_FAULT event is set to INVALID. The Si3473/72 then performs another Class Probe to reconfirm the PD's requested class followed by a Class Reset.

2.7.3 Class Power On

Unlike Class Probe, Class Power On sequence intends to power on the PD. With Class Power On, the number of Classification fingers is used to communicate to the PD how much power it was allocated by the PSE. For example, a Class 4 PD learns it has been power demoted and has been allocated only 15.5 W of power if the PSE presents a single Classification finger during Class Power On. If the PSE presents a Class 4 PD with two fingers during Class Power On, the PD learns it may draw the full 30 W.

If, during Class Power On, an overcurrent or an invalid Classification occurs, the PORTn_POWER_ON_FAULT event is set to *Classification Error*.

Class Power On results are stored in PORTn_ASSIGNED_CLASS. However, PORTn_CLASS_STATUS can contain additional information. In the case of a Power Demotion where a Class 4 PD is demoted to Class 3, PORTn_CLASS_STATUS will report *Class 4 Type 1 Limited*, whereas PORTn_ASSIGNED_CLASS will report Class 3. Refer to Table 3.3 Classification Event Timing on page 64 in 3.34 CLASS_RESULTS (0x4C – 0x4F) for a comprehensive list of class codes and when they are updated.

The Si3473/72 sends out a long class pulse on the first finger during Class Power On for two purposes. First, a long first Classification finger communicates to the PD that the Si3473/72 supports Short Maintain Power Signature (MPS) to save even more power when in standby. Second, with the initial long class pulse, it is possible to detect if the PD supports Autoclass. Refer to 2.8.5 Autoclass for details.

After Class Power On has completed, the FET controlling power to the port is turned on, and the Inrush period begins. The following figure shows the expected waveform for a PORTn_PB_POWER_ON sequence powering a 2-pair PD.

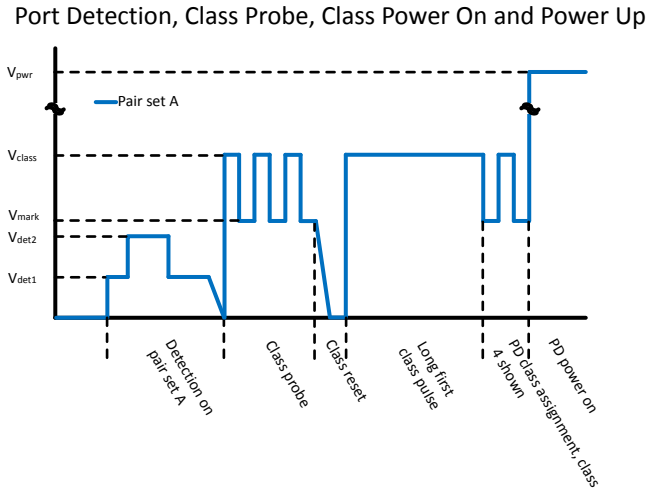


Figure 2.5. 2P Port Detection Waveform

2.8 Powered States

There are two states for which the FET is ON:

1. Inrush Period
2. Power Good State

2.8.1 FET On Status

Each pair set has the PORTn_POWER_ENABLE and PORTn_POWER_GOOD status information suitable for tracking the general state of the Si3473/72 after a PORTn_PB_POWER_ON event, as shown in the following table.

Table 2.1.

PORTn_POWER_ENABLE	PORTn_POWER_GOOD	FET State	After PORTn_PB_POWER_ON
0	0	OFF	Final Detection Class Probe Class Power
1	0	ON	Inrush Period
1	1	ON	Power Good
0	1	—	Invalid

The PORTn_POWER_ENABLE_CHANGE and PORTn_POWER_GOOD_CHANGE bits in the POWER_EVENT register reflect the changes in the POWER_ENABLE and the POWER_GOOD fields of the POWER_STATUS register. These events can be used by a host as a signal to check the POWER_STATUS register and get the most up-to-date port status.

Once set, the PORTn_POWER_GOOD_CHANGE and PORTn_POWER_ENABLE_CHANGE bits are typically cleared by reading the POWER_CHANGE CoR register. In addition, PORTn_POWER_GOOD_CHANGE and PORTn_POWER_ENABLE_CHANGE bits are cleared when PORTn_RESET_PORT is set, PORTn_PB_POWER_OFF is set, or when a port is turned off as a result of an OSS Event.

2.8.2 Inrush Period

Immediately after the external FET is turned on, the Si3473/72 enters the Inrush Period. The Inrush Period is a fixed time period defined by t_{INRUSH}, During the Inrush Period, the Si3473/72 performs a voltage-foldback function for currents higher than 425 mA in order to limit the current drawn from the VPWR rail (see). The Si3473/72 also has a proprietary short-circuit FET protection circuit intended to protect the FET from damage.

The terms “start” and “inrush” are used interchangeably in this document. The Inrush Period is the initial part of a power-on in which the PSE is expected to supply current to the PD’s bulk capacitors. During the Inrush Period, a port implements a 425 mA current limit, with a 30 V Foldback, during a t_{START} or t_{INRUSH} time period.

After t_{INRUSH}, the port should no longer be in a current-limited state. If the port is still in a current-limited state, the port is powered off, and the PORTn_START_FAULT event is raised. Otherwise, the port reaches a POWER_GOOD state, and the Si3473/72 begins monitoring the port.

See 2.8.4 Current Limit and Voltage Foldback for an illustration of how current limiting and voltage foldback work.

2.8.3 Power Good State

When a port is in a POWER_GOOD state, three things are monitored:

1. Disconnection
2. ILIM / Current Limit
3. PCUT / Power Overload Cutoff Point

Disconnection monitoring checks to see if the PD is drawing too little current.

For the next two items, the Si3473/72 is monitoring for “too much current”. The difference between these two over-current monitors is the speed of the action taken.

ILIM events are considered to be fast, high current events. As such, the Si3473/72 aims to limit the current by reducing port voltage. Under extremely fast and high current conditions, the Si3473/72 implements a hardware control loop that aims to control the maximum port current by dynamically lowering the port voltage.

On the other hand, a PCUT does not involve FETs operating in a current-limited state. But rather, the Si3473/72 is monitoring the port voltage and port current, then comparing them against the POLICE register limits.

2.8.3.1 Disconnection

While in the POWER_GOOD state, the Si3473/72 checks whether or not the PD is still connected to the port. A connected PD is obligated to draw a minimum amount of current. To keep the PSE from declaring a disconnection, the PD must meet a defined “Maintain Power Signature” (MPS) for the time duration of t_{MPDO}. If the PD does not meet these MPS requirements, the PSE may choose to power down the port and set the PORTn_DISCONNECTION bit.

2.8.3.2 ILIM / Current Limit

Depending on the assigned PD Class, the Si3473/72 chooses a current-limit template designed to allow normal PD currents to flow, while also setting a peak current threshold to begin a voltage foldback. The Si3473/72 implements a number of current limit templates. A current limit template is a 2-dimensional function that defines a current limit based on a FET's drain voltage. At low drain voltages, the current limit is set at its maximum.

Whenever the measured port current exceeds these current limits, a feedback circuit then adjusts the gate voltage of the FET to fold-back the voltage. The speed at which the gate voltage is adjusted is a function of the difference between the current limit threshold at the drain voltage against the sensed port current.

As a simple example, if the Si3472/73 continuously detects overcurrent in excess of t_{LIM}, it will be considered an ILIM fault and remove power from the port. Section 2.8.4 Current Limit and Voltage Foldback illustrates how this current limiting and voltage foldback works.

The foldback mechanism is done automatically, while the drain voltage is monitored to check for evidence of a current-limited state. The Si3473/72 implements a counter that counts up by 1 whenever the FET is in an over-current state. For every subsequent non-overcurrent event, the counter is decreased by 1/16. This allows current limited events to self-clear if only transient, and prevents nuisance disconnections while also allowing the disconnection of a port based on the severity of the event.

In addition to the programmable current-limit foldback voltage templates, the Si3473/72 also implements a separate short circuit monitor so that if the measured current exceeds two times the pre-set current limit threshold, the FET is turned off. This feature protects the FET in the case of an unexpected short-circuit.

Current Limit faults are reported through the PORTn_ILIM_FAULT bits in the ILIM_START_FAULT register.

2.8.3.3 PCUT Faults

After Class Power On, the PSE is obligated to supply a certain amount of power to the PD based on the assigned class plus expected wire loss. If PSE senses that too much power is being drawn, the PSE disconnects the PD and issues a PCUT event to a host. Once the Port has reached a POWER_GOOD state, the Si3473/72 enforces this mutual power agreement through the PORTn_POLICE_2P register.

Power values in the PORTn_POLICE_2P registers represent the minimum levels the PSE is obligated to supply and the maximum power the PD is allowed to draw before the PSE will disconnect. The majority of the PSE power budget is spent by the PD as useful power, but some of the PSE power budget is dissipated due to wire transmission losses.

The internal PCUT threshold is set at 15% above the power levels shown in PORTn_POLICE_2P. This 15% threshold was chosen to maximize the probability of powering up legacy PDs and to accommodate higher wire loss use cases.

It is important to note that a host always has the option of re-adjusting PORTn_POLICE_2P once the port has reached Power Good state to a lower PCUT level.

The expected PCUT behavior needs to take measurement error into consideration.

For Class 0, 1, 2 and 3:

- Measurement Error is 10% max
- Class 1 PORTn_POLICE_2P = 4 W
- Class 2 PORTn_POLICE_2P = 7 W
- Class 0 or Class3 PORTn_POLICE_2P = 15.5 W
- Power is maintained if Measured V * Measured I < 1.05 * PORTn_POLICE_2P
- Power is removed if Measured V * Measured I > 1.25 * PORTn_POLICE_2P
- Power may be maintained or removed if 1.05 * PORTn_POLICE_2P > Measured V * Measured I > * 1.25 PORTn_POLICE_2P

For Class 4

- Measurement Error is 5% max
- Class 4 PORTn_POLICE_2P = 30W
- Power is maintained if Measured V * Measured I < 1.10 * PORTn_POLICE_2P
- Power is removed if Measured V * Measured I > 1.20 * PORTn_POLICE_2P
- Power may be maintained or removed if 1.10 * PORTn_POLICE_2P > Measured V * Measured I > 1.20 * PORTn_POLICE_2P

At the completion of Class Power On, the Assigned Class is determined based on the values in PORTnm_POWER_ALLOCATION and PORTn_REQUESTED_CLASS. PORTn_ASSIGNED_CLASS is converted into a minimum power threshold and stored in the applicable PORTn_POLICE_2P register.

After the Si3473/2 sets the police registers based on assigned class, a host can make adjustments to them once it has more accurately determined the actual usage of the PD either through long term checking of the pertinent PORTn_VOLTAGE and PORTn_CURRENT or through LLDP messaging.

PCUT faults are reported in PORTn_PCUT_FAULT_2P.

2.8.4 Current Limit and Voltage Foldback

The figure below illustrates how current limiting works. Consider an initial condition where a FET is ON, with the PD appearing as a 167 Ω load. Suddenly, the load changes from 167 Ω to 62.5 Ω. The initial point condition is below the Green Line, which represents an ILIM Threshold vs VDRAIN template that the Si3473/72 is maintaining. Differences between the actual current and this threshold determine whether current flows into the gate of the FET or out of the gate. The magnitude of the gate current is proportional to the difference between the actual current through the sense resistor, relative to its set point.

When the load initially changes from 167 Ω to 62.5 Ω, the sensed current is higher than the ILIM Threshold at that VDRAIN voltage, and as such, current is removed from the gate, leading to the FET shutting down slightly, and an increase in VDRAIN.

Eventually, VDRAIN will increase enough that it meets the 62.5 Ω load line, where the gate drive becomes zero since the sensed current is at the green line. In this example, when the PD Load decreases from 167 Ω to 62.5 Ω, the port voltage folds back from 50 V to around 22 V.

Note that the example does not show the intermediate steps, only the starting points and end points. This is a feedback circuit and this illustration cannot show that the speed by which VDRAIN increases is in proportion to the magnitude difference between the sensed current and the ILIM curve.

Some things to note include:

1. The FET power in the current limited state is 28 V * 350 mA = 9.8 W. To prevent damage, the Si3473/72 limits the time the FET spends in this condition.
2. The DRAIN Voltage is high. The Si3473/72 can measure this, and by taking the ILIM Template into account, the power level being experienced by the FET can be approximated.

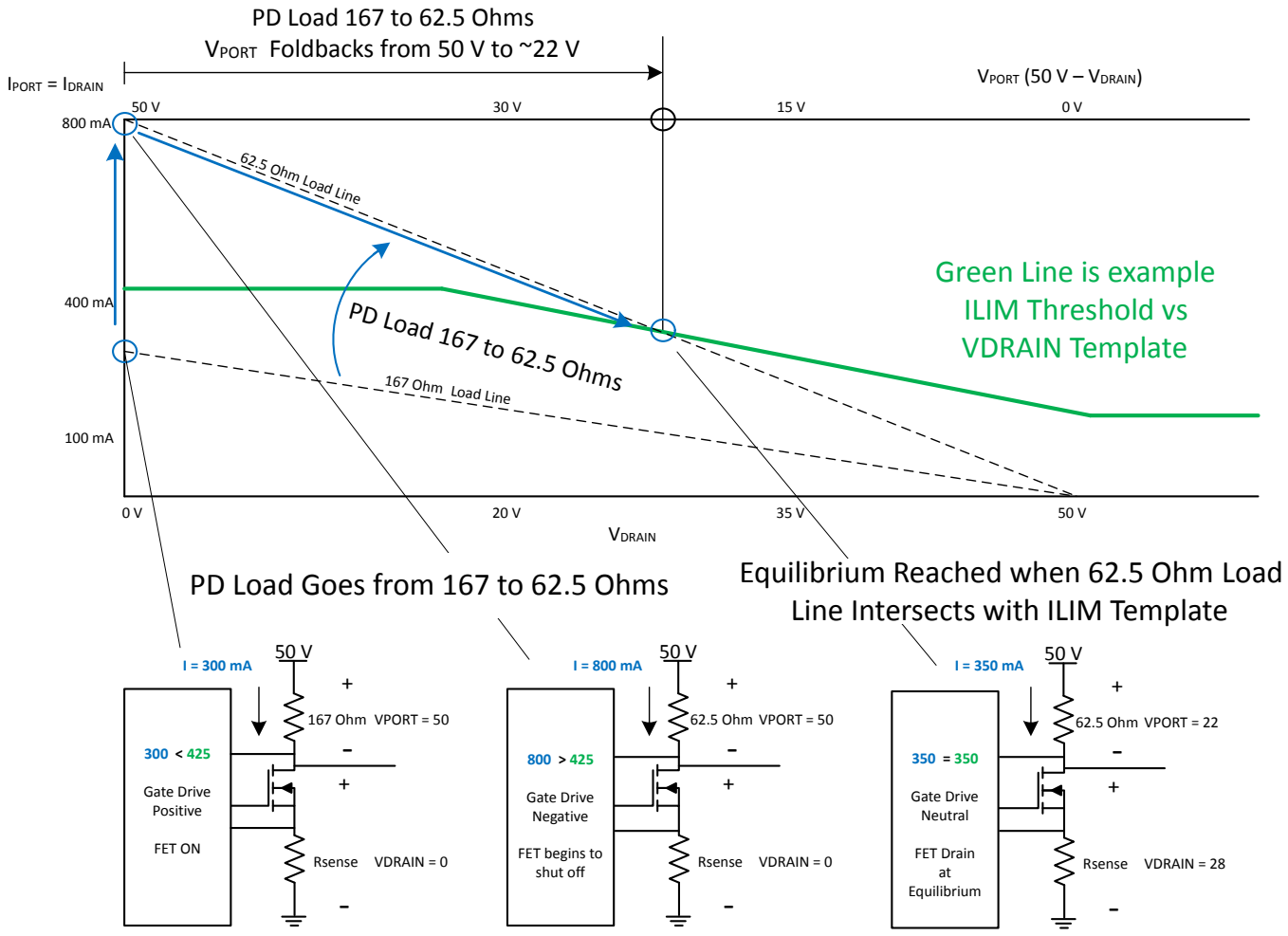


Figure 2.6. Current Limiting and Voltage Feedback

2.8.5 Autoclass

When Automatic Autoclass is enabled, the Si3473/72 monitors the first long class finger of Class Power On to detect if the PD is Autoclass-capable. If the Si3473/72 detects the PD acknowledgement, the PORTn_AUTOCLASS_DETECTED bit is set on that port. The Si3473/72 then takes voltage and current measurements when the pair sets reach the POWER GOOD state. The PORTn_POLICE_2P registers will be initialized based on measured power plus margin. The margin depends on the measured power:

- 0 W to 25.9 W: margin = 1 W
- 26 W to 36.9 W: margin = 2 W
- 37 W to 44.9 W: margin = 3 W
- 45 W to 51.9 W: margin = 4 W

If PORTn_AUTO_AUTOCLASS is set, the corresponding PORTn_POLICE_2P register is updated using the information in PORTn_AUTOCLASS_POWER, plus some power margin. A host may also initiate a Manual Autoclass by setting PORTn_MANUAL_AUTOCLASS in the AUTOCLASS_CONTROL register. The manual Autoclass feature is typically used in conjunction with the LLDP-initiated Autoclass procedure.

A host is expected to initiate a Manual Autoclass when the PD is drawing its maximum power. The Si3473/72 stores the computed Autoclass power results in PORTn_AUTOCLASS_POWER. Once the results are written into PORTn_AUTOCLASS_POWER fields, the Si3473/72 clears the PORTn_MANUAL_AUTOCLASS bits. When both PORTn_MANUAL_AUTOCLASS bits are cleared, a host can use this as an indication that information is ready. A host may then overwrite the results of the police register based on the power information supplied by the PORTn_AUTOCLASS_POWER field.

2.9 Event Handling

As an I2C primary controller, a host can initiate communication with the Si3473/72 at any time. As events associated with PSE operations can happen at any time, the Si3473/72 signals a host by asserting the INTb pin and then waits for a host to respond.

A host may be busy when an event occurs and unable to service the interrupt until after the conditions that caused the event have passed. The Si3473/72 interface uses clear-on-read (COR) registers that retain event information until a host can read it.

When the Si3473/72 wants attention from a host, it does so by setting an event in the event register map. The event bits map into a corresponding bit in the INTERRUPT register. If the corresponding INTERRUPT_MASK bit is also set, then the INTb pin will be asserted.

In a high port count system that has multiple Si3473 PSE controllers, all of the controllers' INTb open drain output pins must be tied together. Even with a single Si3473 PSE controller, there is just one INTb output for two quads that have separate I2C addresses. Therefore, when the INTb pin is asserted, a host must read the INTERRUPT register from every I2C address in the PSE system.

For speedy servicing of interrupts in a high port count system controlled by a single host, the INTERRUPT register is read first by a host. Each bit in the INTERRUPT register is mapped to another register where the details of the event are available to read. See Table 3.1 Si3473/72 Registers on page 27. The only way to clear the INTERRUPT register bit and associated INTb output is to have a host read these COR registers. For example, a host reads INTERRUPT and observes that the DISCONNECT bit is set. The color coding in the table below indicates that a host must read the DISCONNECT_PCUT_FAULT register to clear the DISCONNECT bit in the INTERRUPT register. In this case, a host would know to read DISCONNECT_PCUT_FAULT register as this is where the DISCONNECTION field is located.

When a host reads the appropriate COR register, the INTb pin is not guaranteed to negate since a new event may have occurred after the COR register was read to clear the event.

When a PORTn_START_FAULT event is reported, the corresponding PORTn_POWER_ON_FAULT is updated with supplemental information about the fault. However, only the ILIM_START_FAULT register must be read to clear the START_EVENT INTERRUPT bit.

In addition to reading a CoR register, PORTn_CLASS_DONE, PORTn_DETECT_DONE, PORTn_DISCONNECTION, PORTn_PCUT_FAULT_2P, PORTn_ILIM_FAULT, and PORTn_START_FAULT registers can also be cleared by:

1. Setting PORTn_PORT_MODE to SHUTDOWN
2. Setting PORTn_PB_POWER_OFF in PB_POWER_ENABLE
3. Setting PORTn_RESET_PORT in PB_RESET
4. An OSS_EVENT in SUPPLY_EVENT as a result of an emergency shutdown
5. Setting RESET_QUAD
6. Setting CLEAR_ALL_INTS

Table 2.2. Event Register Bits Associated with Interrupt Register

Address	Name	Access	b7	b6	b5	b4	b3	b2	b2	b0
INTERRUPT REGISTERS										
0x00	INTERRUPT	RO	SUPPLY_EVENT	START_EVENT	P_I_FAULT	CLASS_DONE	DETECT_DONE	DISCONNECT	POWER_GOOD_CHANGE	POWER_ENABLE_CHANGE
0x01	INTERRUPT_MASK	R/W								
EVENT REGISTER BITS ASSOCIATED WITH INTERRUPT REGISTER										
0x02	POWER_EVENT	RO	POWER_GOOD_CHANGE				POWER_ENABLE_CHANGE			
0x03		CoR								
0x04	CLASS_DETECT_EVENT	RO	CLASS_DONE				DETECT_DONE			
0x05		CoR								
0x06	DISCONNECT_PCUT_FAULT	RO	DISCONNECTION				PCUT_FAULT			
0x07		CoR								
0x08	ILIM_START_FAULT	RO	ILIM_FAULT				START_FAULT			
0x09		CoR								
0x0A	SUPPLY_EVENT	RO	OVER_TEMP	VDD_UVLO_FAIL	VDD_UVLO_WARN	VPWR_UVLO	--	--	OSS_EVENT	--
0x0B		CoR								
0x24	POWER_ON_FAULT	RO	PORT4_POWER_ON_FAULT		PORT3_POWER_ON_FAULT		PORT2_POWER_ON_FAULT		PORT1_POWER_ON_FAULT	
0x25		CoR								

2.10 Autonomous Operation

If the total allocated PD load can be supplied by the system VPWR, one of the two Autonomous Modes may be used.

In auto mode, the Si3473/72 attempts to power on the port after every successful Detection/Classification. If a fault occurs at any time, the Si3473/72 will return to continuous Detection/Classification.

2.10.1 AUTO Pin Autonomous Mode

To configure AUTO Pin Autonomous Mode, a voltage (other than VDD) must be applied to the AUTO pin input at time of Si3473/72 power up. The common way to achieve this is to use two resistors to create a voltage divider as shown inside the dashed box labeled "Opt. HW-Selected Auto Mode" in Figure 2.1 Si3473/72 Typical Application Circuit on page 6.

With a 15 kΩ resistor to VDD, the following resistors to GND can be used to configure the AUTO pin Autonomous Mode.

Table 2.3. AUTO Pin Autonomous Mode Configuration

Lower Resistor	Maximum Allowable PD Class	Available Power to Each Port	PSE Location	Equivalent Register Setting	
				POWER_ALLOCATION	MIDSPAN Bit in MISC (Register 0x17 Bit 0)
None	Hosted I²C Operation				
124 kΩ	Class 3	4 W	Midspan	0x11	1
61.9 kΩ	Class 4	7 W	Midspan	0x22	1
35.7 kΩ	Class 3	15 W	Midspan	0x00	1
22.6 kΩ	Class 4	30 W	Midspan	0x33	1
15.8 kΩ	Class 1	4 W	Endspan	0x11	0
11 kΩ	Class 2	7 W	Endspan	0x22	0
7.68 kΩ	Class 3	15 W	Endspan	0x00	0
5.1 kΩ	Class 4	30 W	Endspan	0x33	0

The operation of AUTO Pin Autonomous Mode is identical to setting the following (in both Quads or the Si3473):

1. PORT_REMAP = 0xE4 (no remapping)
2. POWER_ALLOCATION is described in the POWER_ALLOCATION column of the above table.
3. INTERRUPT_MASK = 0xE4 (faults enabled)
4. PORT_MODE = 0xFF (all ports in AUTO Mode)
5. PORT_DETECT_CLASS_ENABLE = 0xFF (all ports DETECT_ENABLE = 1 and CLASS_ENABLE = 1)
6. MIDSPAN is described in the MIDSPAN Bit column of the above table.

2.10.2 I²C Autonomous Mode

A host can place a port in I²C Autonomous Mode at any time through the register interface by setting PORTn_DETECT_ENABLE, PORTn_CLASS_ENABLE, and PORTn_MODE to AUTO.

Placing the Si3473/72 in I²C Autonomous Mode requires the following register settings to both Quads (only one quad for Si3472):

1. PORT_REMAP = 0xE4 (no remapping)
2. POWER_ALLOCATION = system-dependent
3. INTERRUPT_MASK = 0xE4 (faults enabled)
4. PORT_MODE = 0xFF (all ports in AUTO Mode)
5. PORT_DETECT_CLASS_ENABLE = 0xFF (all ports DETECT_ENABLE = 1 and CLASS_ENABLE = 1)

POWER_ALLOCATION refers to setting the PORTnm_POWER_ALLOCATION registers. Refer to 3.25 POWER_ALLOCATION (0x29) for more details.

2.11 OSS Operation

2.11.1 Emergency Shutdown Feature

The Si3473/72 supports two kinds of Emergency Shutdown procedures, both of which are controlled by a host via the OSS pin. If MULTIBIT_PRIORITY_ENABLE = 0 (in MISC register), then 2.11.1.1 1-Bit Shutdown Priority describes the Emergency Shutdown behavior. Otherwise, if MULTIBIT_PRIORITY_ENABLE = 1 (in MISC register), then 2.11.1.2 Multi-Bit Shutdown Priority describes the Emergency Shutdown behavior.

The Emergency Shutdown Feature is useful in systems having multiple power supplies. When one of the power supplies fails, a host can use the Emergency Shutdown Feature to quickly turn off ports using the OSS pin. A host is expected to configure the priority level of each port so that the Si3473/72 knows which ports to power down in case of an emergency.

2.11.1.1 1-Bit Shutdown Priority

If MULTIBIT_PRIORITY_ENABLE = 0, then the PORTn_PORT_POWER_PRIORITY bit in each port defines the port Shutdown priority. PORTn_PORT_POWER_PRIORITY bits are found in the POWER_PRIORITY_PCUT_DISABLE register. If PORTn_PORT_POWER_PRIORITY is set, then the associated port is tagged as a "Low Priority" port. "High Priority" ports are unaffected by an OSS event.

A positive-going edge on the OSS pin will shut down powered lower priority ports. All powered lower priority ports will be shut down within 50 µs. Refer to the PORTn_PB_POWER_OFF description for all event and register bits that are cleared. When a low priority port is shut down, the POWER_GOOD_CHANGE and POWER_ENABLE_CHANGE registers reflect the events and the POWER_GOOD_CHANGE bit and POWER_ENABLE_CHANGE bit in the INTERRUPT register are set. The OSS_EVENT bit in the SUPPLY_EVENT register is also set.

2.11.1.2 Multi-Bit Shutdown Priority

If MULTIBIT_PRIORITY_ENABLE is set, then PORTn_MULTIBIT_PRIORITY defines the port priority and OSS action.

The figure below shows the operation and timing diagram of the OSS pin in multi-bit mode. Note that:

- The priority of each port is defined by a 3-bit value in PORTn_MULTIBIT_PRIORITY for each port.
- A port whose priority setting is "000" has the highest priority; priority setting of "111" has the lowest priority.
- When a host system wants certain priority ports to be shut down, it will transmit the “Shutdown code” over the OSS pin.
- Ports whose port priority settings are greater than or equal to the received Shutdown code will be turned off. For example, a received OSS Shutdown code of "101" will shut down ports whose port priority settings are "101", "110" or "111".

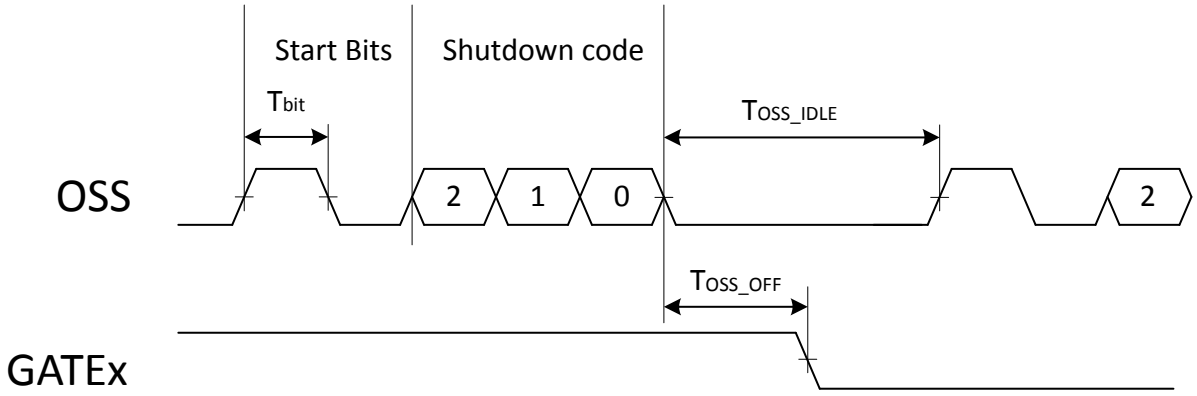


Figure 2.7. OSS Pin in Multi-Bit Mode

The following table describes the timing parameters associated with the OSS pin in multi-priority bit mode.

Table 2.4. Description of Timing Parameters Associated with the OSS Pin In Multi-Bit Mode

Parameter	Description	Min	Typ	Max	Units
T_{bit}	Bit Period	24	25	26	µs
T_{OSS_OFF}	Maximum time between receiving Shut-down code and shutting down of the ports	—	—	50	µs
T_{OSS_IDLE}	Idle time between consecutive Shutdown code transmission in multi-bit mode	125	—	—	µs

2.12 I²C Interface

2.12.1 I²C Protocol

Communicating with the Si3473/72 is accomplished through a 2-wire I²C compatible serial interface. An I²C transaction begins with a START condition and concludes with a STOP condition. The Si3473/72 registers are described in Table 3.1 Si3473/72 Registers on page 27. Note that the Register Map describes the operation of a quad (four ports). Each Si3473 has two quads. As such the Si3473 responds to two I²C addresses, one for each quad. The Si3472 has only one quad and therefore responds only to the main I²C address.

2.12.1.1 Slave Address

The I²C Slave Addresses that the Si3473/72 responds to are dependent on the following:

- A1, A2, A3 and A4 pin strapping (the Si3472 does not have an A4 pin and is therefore limited to 3 bits of addresses.)
- Quad

As mentioned previously, each Si3473 responds to two I²C Addresses since there are two quads in each Si3473.

The 7-bit Slave Address is effectively constructed as this bit pattern:

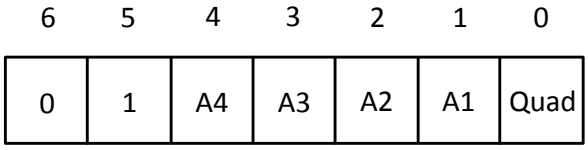


Figure 2.8. 7-bit I²C Address Bit Pattern

The following table outlines the I²C Addresses that the Si3473/72 will respond to, based on the A1, A2, A3 and A4 pin strapping as well as which quad a host intends to access:

Table 2.5. Si3473/72 I²C Slave Address

A4[1]	A3	A2	A1	Quad 0 I²C Address	Quad 1 I²C Address (Si3473 only)
0	0	0	0	0x20	0x21
0	0	0	1	0x22	0x23
0	0	1	0	0x24	0x25
0	0	1	1	0x26	0x27
0	1	0	0	0x28	0x29
0	1	0	1	0x2A	0x2B
0	1	1	0	0x2C	0x2D
0	1	1	1	0x2E	0x2F
1	0	0	0	0x30	0x31
1	0	0	1	0x32	0x33
1	0	1	0	0x34	0x35
1	0	1	1	0x36	0x37
1	1	0	0	0x38	0x39
1	1	0	1	0x3A	0x3B
1	1	1	0	0x3C	0x3D
1	1	1	1	0x3E	0x3F

Note:

1. A4 is effectively tied low on the Si3472.

2.12.1.2 Available I²C Transfer Types

All Si3473/72 registers are accessible using 8-bit Writes and 8-bit Reads.

In addition, 16-bit Port Parametric Measurement Registers must be read using a 16-bit Read address in order to guarantee that the MSB and LSB of the Voltage or Current measurement belong to each other. The 16-bit Read Register Address should be pointing to the least significant byte so that the burst-read will end with the MSB. The following figures illustrate the bits of the possible read and write operations.

Legend

S	Start Bit
Sr	Repeated Start Bit
P	Stop Bit
A1…A4	Si3473/72 A1, A2, A3, A4 pin strapping
Q	Si3473/72 Quad Selection (virtual ‘A0’)
R0…R7	Si3473/72 Register Address
D0…D7	Si3473/72 Register Data LSB
D8…D15	Si3473/72 Register Data MSB
Wr	Write Bit
Rd	Read Bit
A	ACK bit
N	No ACK bit

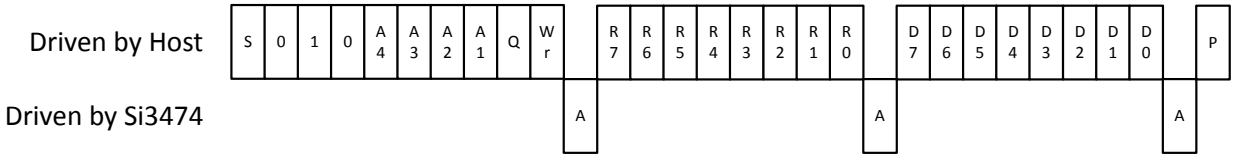


Figure 2.9. 8-Bit Write

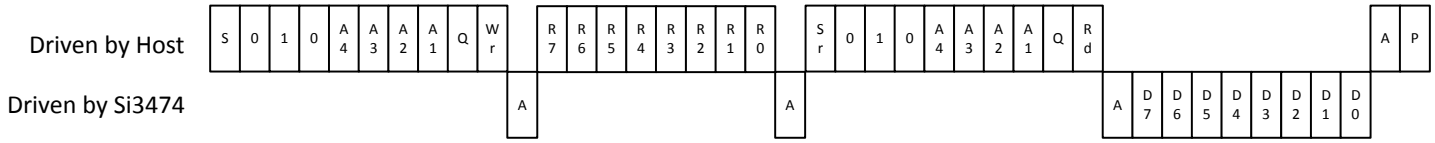


Figure 2.10. 8-Bit Read

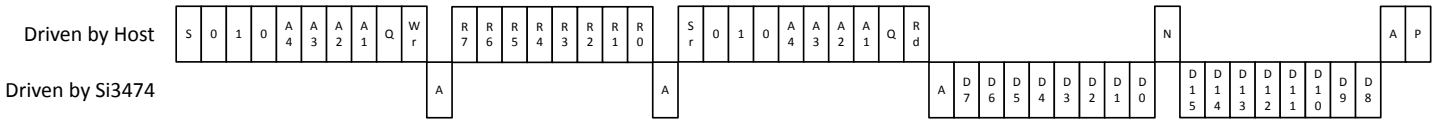


Figure 2.11. 16-Bit Read

2.13 Updating the Si3473/72 FLASH Using the Bootloader

The Si3473/72 firmware can be updated through the I2C interface. The Si3473/72 FLASH memory is separated into the "Application" space and the "Bootloader" space. To ensure that the flash loading process never results in a non-communicating device, only the "Application" part of the firmware is capable of being updated; the Bootloader cannot update itself.

The registers FLASH_CONTROL, FLASH_ERASE_KEY_FLASH_ADDRESS_LSB, FLASH_ADDRESS_MSB, and FLASH_DATA work together to implement the flash update process. The figure below illustrates the flash loading sequence.

A good practice for a host is to check the FIRMWARE_REVISION to see if the FLASH update is necessary.

Once it has been determined that the device needs to be updated, start the flash update procedure with a device reset. The following figure explains the steps to flash the Si3473 and Si3472 devices.

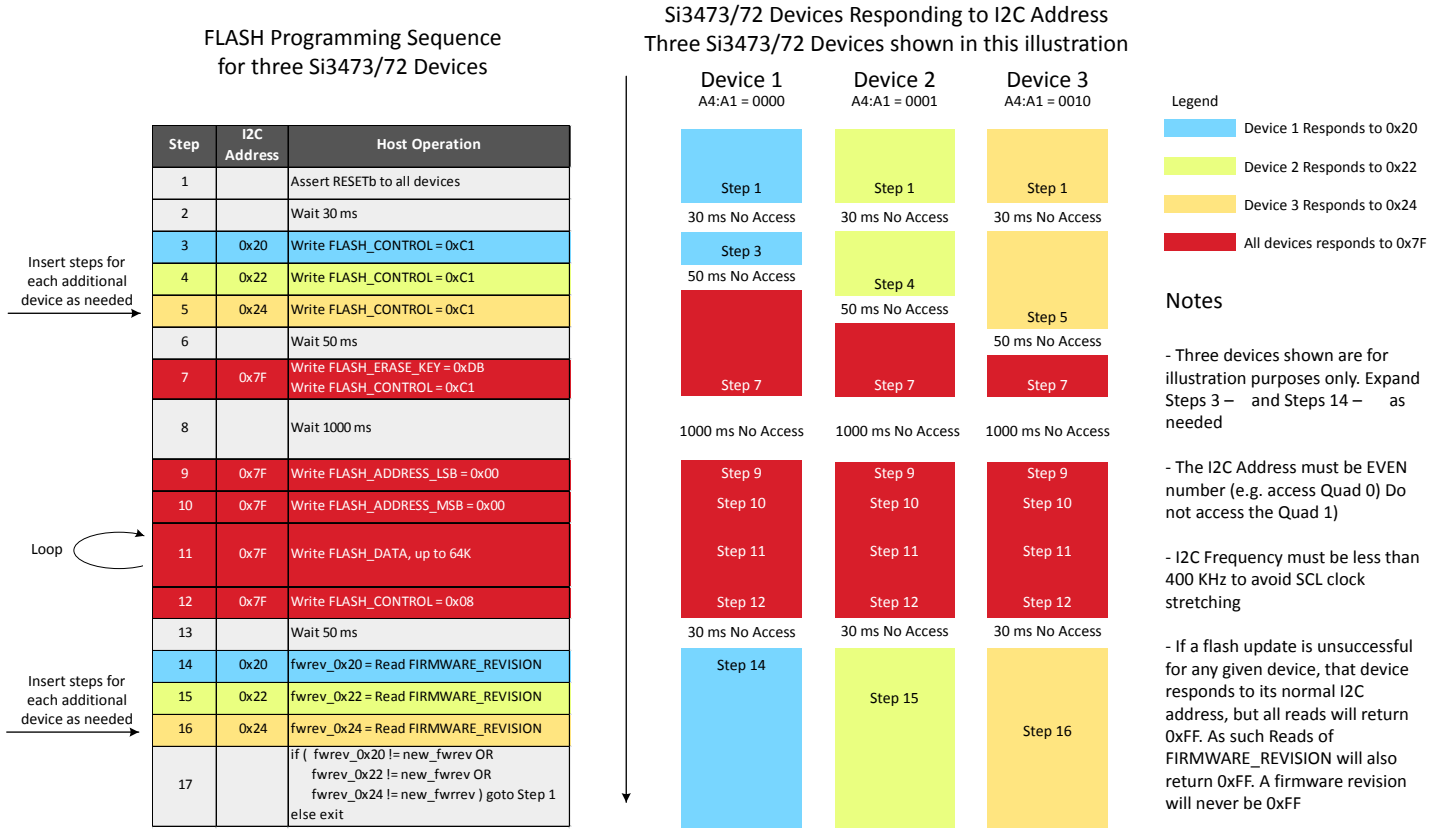


Figure 2.12. Si3473/72 Flash Updating Sequence

The chip reset is illustrated in Step 1. After a RESET, wait 30 ms before starting communication because the device is booting. After the 30 ms wait period, the devices should be able to communicate through I2C, via the standard I2C Address based on the A1-A4 pin strapping.

In Step 3, Step 4 and Step 5, a host should individually command each device to enter its bootload state (FLASH_CONTROL=0xC1). Note that a host must access each device individually through its normal I2C address. It is also important to note that a host must access only the Quad 0. Quad 0 of each device has an even I2C Address. After each device receives its FLASH_CONTROL=0xC1 command, each device will reset into a special state where the device responds to the Global Address 0x7F.

Once a host has sent FLASH_CONTROL=0xC1 through each individual I2C Address, it should delay an additional 50 ms to allow the last device to be ready. This 50 ms delay is illustrated in Step 6. After this final delay, a host can proceed to Step 7, where a host sends another FLASH_CONTROL=0xC1 command. However, this time, a host will use the Global Address 0x7F. In addition, FLASH_ERASE_KEY=0xDB is sent prior to the FLASH_CONTROL=0xC1. This is illustrated in Step 7.

Upon receiving the FLASH_ERASE_KEY=0xDB and FLASH_CONTROL=0xC1 in Step 7, each device will begin to erase the Application FLASH area. This process takes 1000 ms, and a host should not initiate communication during this time. This is illustrated in Step 8.

After the 1000 ms delay, a host should then write 0x00 to both the FLASH_ADDRESS_LSB and FLASH_ADDRESS_MSB registers to indicate the starting address. This is illustrated in Steps 9 and 10.

A host then sends the contents of the new firmware by writing to the FLASH_DATA continuously. For accessing FLASH_DATA, in addition to the standard I2C Register Byte Write method, the Si3473/72 also supports burst writes in order to increase the throughput of the flash update. The burst write is illustrated in the figure below:

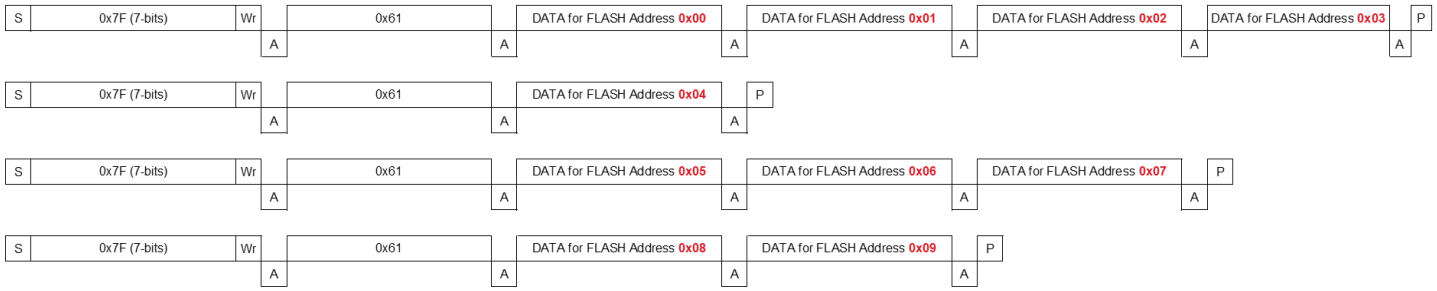


Figure 2.13. Burst Write

To complete the flash update, a host then writes FLASH_CONTROL=0x08 using the Global Address 0x7F. This is illustrated in Step 12. When each Si3473/72 device receives the FLASH_CONTROL=0x08 command, it completes the flash update process and computes the Flash CRC. The Si3473/72 will then reboot and the FIRMWARE_REVISION register can be checked using the normal, non-global addresses to make sure the firmware revision has been updated.

The bootloader firmware is separate from the application firmware and unaware of the expected FIRMWARE_REVISION value. A host should manually check the proper firmware revision in the FIRMWARE_REVISION register using the normal, non-global, I2C address.

In the event something goes wrong with the flash update, a host will receive 0xFF in response to a FIRMWARE_REVISION read. A host will receive 0xFF for all registers if the firmware update procedure fails. If this happens, a host should simply restart the entire process from the very beginning.

3. Register Map

Table 3.1. Si3473/72 Registers

Addr	Name	Access	Reset State	7	6	5	4	3	2
Interrupt Registers									
0x00	INTERRUPT	RO	1000 0000	SUPPLY_ EVENT	START_ EVENT	P_I_ FAULT	CLASS_ DONE	DETECT_ DONE	DISCO NEC
0x01	INTERRUPT_MASK	R/W	1000 0000						
Event Registers									
0x02	POWER_EVENT	RO	0000 0000	POWER_GOOD_CHANGE				POWER_E	
0x03		CoR							
0x04	CLASS_DETECT_EVENT	RO	0000 0000	CLASS_DONE				DET	
0x05		CoR							
0x06	DISCONNECT_PCUT_FAULT	RO	0000 0000	DISCONNECTION				PCU	
0x07		CoR							
0x08	ILIM_START_FAULT	RO	0000 0000	ILIM_FAULT				STA	
0x09		CoR							
0x0A	SUPPLY_EVENT	RO	0xxx[1] 0000	OVER_ TEMP	VDD_ UVLO_ FAIL	VDD_ UVLO_ WARN	VPWR_ UVLO	—	
0x0B		CoR							
0x24	POWER_ON_FAULT	RO	0000 0000	PORT4_POWER_ ON_FAULT		PORT3_POWER_ ON_FAULT		PORT2_POWER_ ON_FAULT	
0x25		CoR	0000 0000						
Main Status Registers									
0x0C	PORT1_CLASS_ DETECT_STATUS	RO	0000 0000	PORT1_CLASS_STATUS				PORT1_DE	
0x0D	PORT2_CLASS_ DETECT_STATUS	RO	0000 0000	PORT2_CLASS_STATUS				PORT2_DE	
0x0E	PORT3_CLASS_ DETECT_STATUS	RO	0000 0000	PORT3_CLASS_STATUS				PORT3_DE	
0x0F	PORT4_CLASS_ DETECT_STATUS	RO	0000 0000	PORT4_CLASS_STATUS				PORT4_DE	

Addr	Name	Access	Reset State	7	6	5	4	3	2
0x10	POWER_STATUS	RO	0000 0000	POWER_GOOD					POW
0x11	PIN_STATUS	RO	0aaa aq00	—	PIN_A4	PIN_A3	PIN_A2	PIN_A1	QUAD
Main Configuration Registers									
0x12	PORT_MODE	R/W	0000 0000	PORT4_PORT_MODE		PORT3_PORT_MODE		PORT2_PORT_MO	
0x13	DISCONNECT_ENABLE	R/W	0000 1111	—				DISCON	
0x14	DETECT_CLASS_ ENABLE	R/W	0000 0000	CLASS_ENABLE				DETE	
0x15	POWER_PRIORITY_ PCUT_DISABLE	R/W	0000 0000	PORT_POWER_PRIORITY				DISA	
0x16	TIMING_CONFIG	R/W	0000 0000	TLIM		TSTART		TOVLD	
0x17	MISC	R/W	1000 0000	INT_PIN_ ENABLE	—	—	MULTI-BIT_ PRIORI-TY_ ENA-BLE	CLASS_ CHANGE	DETEC CHANG
Pushbuttons									
0x18	PB_DETECT_CLASS	WO	0000 0000	RESTART_CLASS				RESTA	
0x19	PB_POWER_ENABLE	WO	0000 0000	PB_POWER_OFF				PB_	
0x1A	PB_RESET	WO	0000 0000	CLEAR_ ALL_INTS	CLEAR_ INT_PIN	—	RESET_ QUAD	RES	

Addr	Name	Access	Reset State	7	6	5	4	3	2
Miscellaneous									
0x1B	VENDOR_ID	RO	0100 0101	MANUFACTURER_ID					
0x1C	AUTOCLASS	RO	0000 0000	AUTOCLASS_DETECTED					
0x1D	Reserved	R/W	0000 0000	—					
0x1E	PORT1_POLICE_2P	R/W	1111 1111	PORT1_POLICE_2P					
0x1F	PORT2_POLICE_2P	R/W	1111 1111	PORT2_POLICE_2P					
0x20	PORT3_POLICE_2P	R/W	1111 1111	PORT3_POLICE_2P					
0x21	PORT4_POLICE_2P	R/W	1111 1111	PORT4_POLICE_2P					
0x22-0x23	Reserved	R/W	0000 0000	—					
0x26	PORT_REMAP	R/W	1110 0100	PORT4_REMAP		PORT3_REMAP		PORT2_REMAP	
0x27	PORT1_PORT2_MULTIBIT_PRIORITY	R/W	0000 0000	—	PORT2_MULTIBIT_PRIORITY			—	POR
0x28	PORT3_PORT_4_MULTIBIT_PRIORITY	R/W	0000 0000	—	PORT4_MULTIBIT_PRIORITY			—	POR
0x29	POWER_ALLOCATION	R/W	0000 0000	—	PORT34_POWER_ALLOCATION			—	PORT
0x2C	TEMPERATURE	RO	xxxx[1] xxxx	TEMPERATURE					
0x2D	Reserved	R/W	0000 0000	—					

Addr	Name	Access	Reset State	7	6	5	4	3	2
Must Use 16-BIT SMBUS Reads for Parametric Measurements									
0x2E	VPWR	RO	xxxx xxxx[1]	LSB					
—		RO	00xx xxxx[1]	—		MSB			
0x30	PORT1_CURRENT	RO	0000 0000	LSB					
—		RO	0000 0000	—		MSB			
0x32	PORT1_VOLTAGE	RO	0000 0000	LSB					
—		RO	0000 0000	—		MSB			
0x34	PORT2_CURRENT	RO	0000 0000	LSB					
—		RO	0000 0000	—		MSB			
0x36	PORT2_VOLTAGE	RO	0000 0000	LSB					
—		RO	0000 0000	—		MSB			
0x38	PORT3_CURRENT	RO	0000 0000	LSB					
—		RO	0000 0000	—		MSB			
0x3A	PORT3_VOLTAGE	RO	0000 0000	LSB					
—		RO	0000 0000	—		MSB			
0x3C	PORT4_CURRENT	RO	0000 0000	LSB					
—		RO	0000 0000	—		MSB			
0x3E	PORT4_VOLTAGE	RO	0000 0000	LSB					
—		RO	0000 0000	—		MSB			

Addr	Name	Access	Reset State	7	6	5	4	3	2
Firmware Revision And Chip Revision									
0x40	MAX_ILIM_MANUAL_ POLICE	RW	0000 0000	MAX_ILIM					MANU
0x41	FIRMWARE_REVISION	RO	Firmware Depend-ent	MAJOR_REVISION					MINO
0x42	I2C_WATCHDOG	RW	0001 0110	0	0	0	WATCHDOG_DISAE		
0x43	CHIP_REVISION	RO	Firmware Depend-ent	Device ID				Silicon Revision	
Detection Resistance Results									
0x44	PORT1_DETECT_ RESISTANCE	RO	0000 0000	PORT1_DETECT_RESISTANCE					
0x45	PORT2_DETECT_ RESISTANCE	RO	0000 0000	PORT2_DETECT_RESISTANCE					
0x46	PORT3_DETECT_ RESISTANCE	RO	0000 0000	PORT3_DETECT_RESISTANCE					
0x47	PORT4_DETECT_ RESISTANCE	RO	0000 0000	PORT4_DETECT_RESISTANCE					
0x48	PORT1_DETECT_ CAPACITANCE	RO	0000 0000	PORT1_DETECT_CAPACITANCE					
0x49	PORT2_DETECT_ CAPACITANCE	RO	0000 0000	PORT2_DETECT_CAPACITANCE					
0x4A	PORT3_DETECT_ CAPACITANCE	RO	0000 0000	PORT3_DETECT_CAPACITANCE					
0x4B	PORT4_DETECT_ CAPACITANCE	RO	0000 0000	PORT4_DETECT_CAPACITANCE					

Addr	Name	Access	Reset State	7	6	5	4	3	2
Assigned Class and Requested Class									
0x4C	PORT1_CLASS_RESULTS	RO	0000 0000	PORT1_ASSIGNED_CLASS				PORT1_RE	
0x4D	PORT2_CLASS_RESULTS	RO	0000 0000	PORT2_ASSIGNED_CLASS				PORT2_RE	
0x4E	PORT3_CLASS_RESULTS	RO	0000 0000	PORT3_ASSIGNED_CLASS				PORT3_RE	
0x4F	PORT4_CLASS_RESULTS	RO	0000 0000	PORT4_ASSIGNED_CLASS				PORT4_RE	
Autoclass Configuration and Results									
0x50	AUTOCLASS_CONTROL	R/W	0000 0000	MANUAL_AUTOCLASS				AUTO_	
0x51	PORT1_AUTOCLASS_ RESULTS	R/W	0000 0000	0	PORT1_AUTOCLASS_POWE				
0x52	PORT2_AUTOCLASS_ RESULTS	R/W	0000 0000	0	PORT2_AUTOCLASS_POWE				
0x53	PORT3_AUTOCLASS_ RESULTS	R/W	0000 0000	0	PORT3_AUTOCLASS_POWE				
0x54	PORT4_AUTOCLASS_ RESULTS	R/W	0000 0000	0	PORT4_AUTOCLASS_POWE				
Miscellaneous									
0x55	ALTERNATIVE_FOLDBACK	R/W	0000 0000	PGOOD_FOLDBACK				INRU	
0x56 - 0x5E	Reserved	R/W	0000 0000	—					

Addr	Name	Access	Reset State	7	6	5	4	3	2
Flash Control									
0x5F	FLASH_ERASE_KEY	R/W	0000 0000	FLASH_ERASE_KEY					
0x60	FLASH_CONTROL	R/W	0000 0000	START_ FLASH-ING	RESET_ CPU	0	0	END_ FLASH-ING	0
0x61	FLASH_DATA	R/W	0000 0000	FLASH_DATA					
0x62	FLASH_ADDRESS_LSB	R/W	0000 0000	FLASH_ADDRESS_LSB					
0x63	FLASH_ADDRESS_MSB	R/W	0000 0000	FLASH_ADDRESS_MSB					
0x64-0xFF	Reserved	R/W	0000 0000	—					

Note:

1. x = undefined after reset.

3.1 INTERRUPT Register (Address 0x00)

INTERRUPT	Register Address: 0x00 Access Type: Read Only Reset: 1000 0000

7	6	5	4	3	2	1	0
SUP-PLY_EVENT	START_EVEN T	P_I_FAULT	CLASS_DONE	DE-TECT_DONE	DISCONNECT	POW-ER_GOOD_C HANGE	POWER_ENA-BLE_CHANGE

Bit	Name	Description
7	SUPPLY_EVENT	VDD, VPWR or Temperature failed 0 = No Events 1 = At least one event in OVER_TEMP, VDD_UVLO_FAIL, VDD_UVLO_WARN, VPWR_UVLO in SUPPLY_EVENT
6	START_EVENT	Fault occurred after PORTn_PB_POWER_ON but before achieving PORTn_POW-ER_GOOD 0 = No Events 1 = At least one event bit in START_FAULT in ILIM_START_FAULT
5	P_I_FAULT	A port previously reached POWER_GOOD state is now unpowered due to a PCUT or ILIM event 0 = No Events 1 = At least one event bit in ILIM_FAULT in ILIM_START_FAULT, PCUT_FAULT_2P in DISCONNECT_PCUT_FAULT
4	CLASS_DONE	Class Probe completed successfully 0 = No Events 1 = At least one event in CLASS_DONE in CLASS_DETECT_EVENT
3	DETECT_DONE	Detection completed 0 = No Events 1 = At least one event in DETECT_DONE in CLASS_DETECT_EVENT
2	DISCONNECT	A port previously reached POWER_GOOD state is now unpowered because of PD disconnection or OSS_EVENT 0 = No Events 1 = At least one event bit in DISCONNECTION in DISCONNECT_PCUT_FAULT, OSS_EVENT in SUPPLY_EVENT
1	POWER_GOOD_CHANGE	POWER_GOOD in POWER_STATUS changed 0 = No Events 1 = At least one event in POWER_GOOD_CHANGE in POWER_EVENT
0	POWER_ENABLE_CHANGE	POWER_ENABLE in POWER_STATUS changed 0 = No Events 1 = At least one event in the POWER_ENABLE_CHANGE in POWER_EVENT

3.2 INTERRUPT_MASK Register (Address 0x01)

INTERRUPT_MASK				Register Address: 0x01 Access Type: Read / Write Reset: 1000 0000			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SUP-PLY_EVENT_MASK	START_EVENT_MASK	P_I_FAULT_MASK	CLASS_DONE_MASK	DE-TECT_DONE_MASK	DISCON-NECT_MASK	POW-ER_GOOD_CHANGE_MASK	POWER_ENA-BLE_CHANGE_MASK

Bit	Name	Description
7	SUPPLY_EVENT_MASK	Masks SUPPLY_EVENT in the INTERRUPT register 0 = SUPPLY_EVENT not can assert INTb 1 = SUPPLY_EVENT can assert INTb
6	START_EVENT_MASK	Masks START_EVENT in the INTERRUPT register 0 = START_EVENT cannot assert INTb 1 = START_EVENT can assert INTb
5	P_I_FAULT_MASK	Masks the P_I_FAULT in the INTERRUPT register 0 = P_I_FAULT cannot assert INTb 1 = P_I_FAULT can assert INTb
4	CLASS_DONE_MASK	Masks the CLASS_DONE in the INTERRUPT register 0 = CLASS_DONE cannot assert INTb 1 = CLASS_DONE can assert INTb
3	DETECT_DONE_MASK	Masks the DETECT_DONE in the INTERRUPT register 0 = DETECT_DONE cannot assert INTb 1 = DETECT_DONE can assert INTb
2	DISCONNECT_MASK	Masks DISCONNECT in the INTERRUPT register 0 = DISCONNECT cannot assert INTb 1 = DISCONNECT can assert INTb
1	POW-ER_GOOD_CHANGE_MASK	Masks POWER_GOOD_CHANGE in the INTERRUPT register 0 = POWER_GOOD_CHANGE cannot assert INTb 1 = POWER_GOOD_CHANGE can assert INTb
0	POWER_ENA-BLE_CHANGE_MASK	Masks POWER_ENABLE_CHANGE in the INTERRUPT register 0 = POWER_ENABLE_CHANGE cannot assert INTb 1 = POWER_ENABLE_CHANGE can assert INTb

The INTERRUPT and INTERRUPT_MASK registers work together to influence the INTb pin logic for any given Quad. The Si3473 has two Quads, and either Quad can assert the INTb pin independently.

$Quad\_0\_INT = INTERRUPT_{Q0}$ AND $INTERRUPT\_MASK_{Q0}$

$Quad\_1\_INT = INTERRUPT_{Q1}$ AND $INTERRUPT\_MASK_{Q1}$

INTb = NOT (Quad_0_INT OR Quad_1_INT)

For the Si3472, which has a single quad:

INTb = NOT (Quad_0_INT)

Bits in the in the INTERRUPT register can be cleared by a number of actions:

1. Reading CoR EVENT registers
2. Setting PORTn_PORT_MODE to SHUTDOWN
3. Setting PORTn_PB_POWER_OFF
4. Setting RESET_QUAD
5. Setting PORTn_RESET_PORT
6. Set CLEAR_ALL_INTS
7. OSS Emergency Shutdown

It is also possible to negate the INTb pin directly using the CLEAR_INT_PIN. This method does not clear any event register bits, nor does it clear bits in the INTERRUPT register.

3.3 POWER Event and POWER Event CoR (Address 0x02, 0x03)

POWER_EVENT				Register Address: 0x02 Access Type: Read Only Reset: 0000 0000			Register Address: 0x03 Access Type: Clear on Read Reset: 0000 0000
7	6	5	4	3	2	1	0
POWER_GOOD_CHANGE				POWER_ENABLE_CHANGE			
PORT4	PORT3	PORT2	PORT1	PORT4	PORT3	PORT2	PORT1

Bit	Name	Description
7	PORT4_POWER_GOOD_CHANGE	PORTn_POWER_GOOD_CHANGE PORTn_POWER_GOOD in POWER_STATUS register changed 0 = PORTn_POWER_GOOD did not change 1 = PORTn_POWER_GOOD changed
6	PORT3_POWER_GOOD_CHANGE	
5	PORT2_POWER_GOOD_CHANGE	
4	PORT1_POWER_GOOD_CHANGE	
3	PORT4_POWER_ENABLE_CHANGE	PORTn_POWER_ENABLE_CHANGE PORTn_POWER_ENABLE in POWER_STATUS register changed 0 = PORTn_POWER_ENABLE did not change 1 = PORTn_POWER_ENABLE changed
2	PORT3_POWER_ENABLE_CHANGE	
1	PORT2_POWER_ENABLE_CHANGE	
0	PORT1_POWER_ENABLE_CHANGE	

For a description of what POWER_GOOD and POWER_ENABLE means, refer to the description in the POWER_STATUS register.

PORTn_POWER_GOOD_CHANGE indicates that PORTn_POWER_GOOD in the POWER_STATUS register has changed. Any set PORTn_POWER_GOOD_CHANGE bit will also set the POWER_GOOD_CHANGE bit in the INTERRUPT register.

PORTn_POWER_ENABLE_CHANGE indicates that PORTn_POWER_ENABLE in the POWER_STATUS register has changed. Any set PORTn_POWER_ENABLE_CHANGE bit will also set the POWER_ENABLE_CHANGE bit in the INTERRUPT register.

3.4 CLASS_DETECT_EVENT and CLASS_DETECT_EVENT CoR (0x04, 0x05)

CLASS_DETECT_EVENT				Register Address: 0x04 Access Type: Read Only Reset: 0000 0000			Register Address: 0x05 Access Type: Clear on Read Reset: 0000 0000
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CLASS_DONE				DETECT_DONE			
PORT4	PORT3	PORT2	PORT1	PORT4	PORT3	PORT2	PORT1

Bit	Name	Description
7	PORT4_CLASS_DONE	PORTn_CLASS_DONE PORTn_CLASS_STATUS in PORTn_CLASS_DETECT_STATUS register was updated or changed (see also CLASS_CHANGE in 3.16 MISC (0x17)). 0 = PORTn_CLASS_STATUS was not updated nor changed. 1 = PORTn_CLASS_STATUS was updated or changed.
6	PORT3_CLASS_DONE	
5	PORT2_CLASS_DONE	
4	PORT1_CLASS_DONE	
3	PORT4_DETECT_DONE	PORTn_DETECT_DONE PORTn_DETECTION_STATUS in PORTn_CLASS_DETECT_STATUS register was updated or changed (see also DETECT_CHANGE in 3.16 MISC (0x17)). 0 = PORTn_DETECTION_STATUS was not updated nor changed. 1 = PORTn_DETECTION_STATUS was updated or changed.
2	PORT3_DETECT_DONE	
1	PORT2_DETECT_DONE	
0	PORT1_DETECT_DONE	

PORTn_DETECT_DONE indicates whether the PORTn_DETECTION_STATUS in PORTn_CLASS_DETECT_STATUS has valid results. Any set bits in the DETECT_DONE field sets the DETECT_DONE bit in the INTERRUPT register.

One common usability issue with enabling the DETECT_DONE bit interrupt is that there tend to be many Detection events. One good way of reducing the number of interrupts is by also setting the DETECT_CHANGE bit in the MISC register. When this bit is set, the PORTn_DETECT_DONE is only updated whenever there is a change in PORTn_DETECTION_STATUS, thereby reducing the number of interrupts to the system.

PORTn_CLASS_DONE indicates whether PORTn_CLASS_STATUS in PORTn_CLASS_DETECT_STATUS register has valid results. The PORTn_CLASS_DETECT_STATUS will always indicate RGOOD as Class Probe does not occur without RGOOD. Any set PORTn_CLASS_DONE bits also set the CLASS_DONE bit in the INTERRUPT register.

3.5 DISCONNECT_PCUT_FAULT and DISCONNECT_PCUT_FAULT CoR (0x06, 0x07)

DISCONNECT_PCUT_FAULT				Register Address: 0x06 Access Type: Read Only Reset: 0000 0000			Register Address: 0x07 Access Type: Clear on Read Reset: 0000 0000
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISCONNECTION				PCUT_FAULT_2P			
PORT4	PORT3	PORT2	PORT1	PORT4	PORT3	PORT2	PORT1

Bit	Name	Description
7	PORT4_DISCONNECTION	PORTn_DISCONNECTION A PORTn in POWER_GOOD, did not detect sufficient current to meet MPS requirements, leading to a disconnection. 0 = PORTn did not disconnect. 1 = PORTn disconnected.
6	PORT3_DISCONNECTION	
5	PORT2_DISCONNECTION	
4	PORT1_DISCONNECTION	
3	PORT4_PCUT_FAULT_2P	PORTn_PCUT_FAULT_2P PORTn in POWER_GOOD state, was powered off because it exceeded the power threshold defined by the pertinent PORTn_POLICE_2P register. 0 = PORTn did not encounter a PCUT fault. 1 = PORTn encountered a PCUT fault.
2	PORT3_PCUT_FAULT_2P	
1	PORT2_PCUT_FAULT_2P	
0	PORT1_PCUT_FAULT_2P	

PORTn_DISCONNECTION indicates a powered port was formerly in a POWER_GOOD state but is now unpowered because the PD drew too much current. Any set PORTn_DISCONNECTION bits also set the DISCONNECT bit in the INTERRUPT register.

PORTn_PCUT_FAULT_2P indicates a powered port, formerly in a POWER_GOOD state, is now unpowered because the PD exceeded the power limits specified by the various POLICE registers. Any set PORTn_PCUT_FAULT_2P bits will set the P_I_FAULT bit in the INTERRUPT register.

3.6 ILIM_START_FAULT and ILIM_START_FAULT CoR (0x08, 0x09)

ILIM_START_FAULT				Register Address: 0x08 Access Type: Read Only Reset: 0000 0000			Register Address: 0x09 Access Type: Clear on Read Reset: 0000 0000
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ILIIM_FAULT				START_FAULT			
PORT4	PORT3	PORT2	PORT1	PORT4	PORT3	PORT2	PORT1

Bit	Name	Description
7	PORT4_ILIM_FAULT	PORTn_ILIM_FAULT PORTn previously in POWER_GOOD state, encountered an overcurrent event, for longer than tLIM, leading to the port being powered down. 0 = PORTn did not encounter an ILIM fault. 1 = PORTn encountered an ILIM fault.
6	PORT3_ILIM_FAULT	
5	PORT2_ILIM_FAULT	
4	PORT1_ILIM_FAULT	
3	PORT4_START_FAULT	PORTn_START_FAULT PORTn was still powering up encountered an overcurrent condition, for longer than the t_{INRUSH}. PORTn never achieved a POWER_GOOD status and is not powered. 0 = PORTn did not encounter a start fault. 1 = PORTn encountered a start fault.
2	PORT3_START_FAULT	
1	PORT2_START_FAULT	
0	PORT1_START_FAULT	

PORTn_ILIM_FAULT indicates that a powered port in POWER_GOOD state is now unpowered because the port was in a current-limited state for longer than the t_{ILIM} time limit. Any set PORTn_ILIM_FAULT bits will set the P_I_FAULT bit in the INTERRUPT register.

PORTn_START_FAULT indicates that a powering port did not reach POWER_GOOD (POWER_ENABLE is set but POWER_GOOD is not set) because PORTn was in a current-limited state for longer than the t_{INRUSH} time limit. Any set PORTn_START_FAULT bits will set the START_FAULT bit in the INTERRUPT register.

3.7 SUPPLY_EVENT and SUPPLY_EVENT CoR (0x0A, 0x0B)

SUPPLY_EVENT				Register Address: 0x0A Access Type: Read Only Reset: 0001 0000		Register Address: 0x0B Access Type: Clear on Read Reset: 0001 0000	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OVER_TEMP	VDD_UV-LO_FAIL	VDD_UV-LO_WARN	VPWR_UVLO	—		OSS_EVENT	—
—	—	—	—	—	—	—	—

Bit	Name	Description
7	OVER_TEMP	Device temperature monitoring indicator 0 = Normal temperature. 1 = Device case temperature exceeded 125 °C.
6	VDD_UVLO_FAIL	VDD UVLO Failure Status 0 = VDD is greater than 2.25 V. 1 = VDD was measured to be under 2.25 V. Upon entering this condition, VDD needs to be higher than 2.6 V to exit this condition.
5	VDD_UVLO_WARN	VDD UVLO Warning Status 0 = VDD is greater than 2.8 V. 1 = VDD was measured under 2.8 V. Upon entering this condition, VDD needs to be higher than 3.1 V to exit this condition.
4	VPWR_UVLO	VPWR UVLO Status 0 = VPWR is greater than 28 V. 1 = VPWR was measured to be less than 28 V. Upon entering this condition, VPWR needs to be higher than 31 V to exit this condition.
1	OSS_EVENT	Emergency shutdown affected one of the ports in the quad. 0 = No emergency shutdown event. 1 = At least one low priority port was shut down.

When one of the OVER_TEMP, VDD_UVLO_FAIL, VDD_UVLO_WARN, or VPWR_UVLO bits are set, the SUPPLY_EVENT bit in the INTERRUPT register is also set. The ports are powered off and the no Detection, Classification and Power sequence can not occur while these events persist.

3.8 POWER_ON_FAULT and POWER_ON_FAULT CoR (0x24, 0x25)

POWER_ON_FAULT				Register Address: 0x24 Access Type: Read Only Reset: 0000 0000		Register Address: 0x25 Access Type: Clear on Read Reset: 0000 0000	
7	6	5	4	3	2	1	0
POWER_ON_FAULT		POWER_ON_FAULT		POWER_ON_FAULT		POWER_ON_FAULT	
PORT4		PORT3		PORT2		PORT1	

Bit	Name	Description
7-6	PORT4_POWER_ON_FAULT	PORTn_POWER_ON_FAULT While attempting to turn on a port, a fault occurred even before turning on the FET. 00 = No Event. 01 = Invalid Detection. 10 = Classification Error. 11 = Insufficient power allocation.
5-4	PORT3_POWER_ON_FAULT	
3-2	PORT2_POWER_ON_FAULT	
1-0	PORT1_POWER_ON_FAULT	

When PORTn_POWER_ON_FAULT is set, the START_FAULT bit in the INTERRUPT register is also set.

3.9 CLASS_DETECT_STATUS Registers (0x0C–0x0F)

PORTn_CLASS_DETECT_STATUS Register	Register Address: 0x0C/0x0D/0x0E/0x0F; Port 1/2/3/4 respectively Access Type: Read Only Reset: 0000 0000 for each PORTn_CLASS_DETECT_STATUS

7	6	5	4	3	2	1	0
PORTn_CLASS_STATUS				PORTn_DETECTION_STATUS			

Code	PORTn_CLASS_STATUS	Code	PORTn_DETECTION_STATUS
0000	UNKNOWN	0000	UNKNOWN
0001	Class 1	0001	Short circuit
0010	Class 2	0010	Capacitive[1]
0011	Class 3	0011	RLOW
1000	Class 5 4P Single Signature	1000	—
1001	—	1001	—
1010	—	1010	—
1011	—	1011	—
0100	Class 4	0100	RGOOD
0101	—	0101	RHIGH
0110	Class 0	0110	Open circuit
0111	Overcurrent	0111	PSE to PSE[2]
1100	Class 4 Type 1 Limited[1]	1100	—
1101	Class 5 Legacy[2]	1100	—
1110	—	1110	—
1111	Class Mismatch[3]	1111	MOSFET_FAULT

Note:
1. Class 4 Type 1 Limited is not emitted in Semi Auto Class Probe. It may occur during a Class Power On as a result of PB_POWER_ON
2. This status will only be reported if Class 5 Legacy power allocation is selected.
3. The Si3473/72 automatically performs a Class Reset and repeats Classification.

Note:
1. Capacitive status is reported when the load capacitance is larger than 1.5 µF (Cpd > 1.5 µF).
2. The Si3473/72 is capable of detecting whether it is cross-connected to another PSE controller of a different type. In this case, the PSE to PSE Status is reported. Detection of another PSE is based on verifying the voltage level on the output (DRAINn pin) during Detection.

In SEMI_AUTO mode, the Classification process is not initiated unless RGOOD is reported. When reading PORTn_CLASS_STATUS outside of an event handler servicing the PORTn_CLASS_DONE, the Classification status can be unknown, or it can be the last Classification status after the last RGOOD.

It is generally recommended to read PORTn_CLASS_STATUS only when PORTn_CLASS_DONE indicates that there is useful information available.

3.10 PORT_POWER_STATUS Register (0x10)

PORT_POWER_STATUS				Register Address: 0x10 Access Type: Read Only Reset: 0000 0000			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
POWER_GOOD				POWER_ENABLE			
PORT4	PORT3	PORT2	PORT1	PORT4	PORT3	PORT2	PORT1

Bit	Name	Description
7	PORT4_POWER_GOOD	PORTn has passed through the initial inrush period and has successfully powered up the port 0 = OFF 1 = PORTn is in POWER_GOOD state PORTn is in POWER_GOOD state after the initial t_{INRUSH} and that the PORTn Drain is within 2 V of the Si3473/72 ground reference.
6	PORT3_POWER_GOOD	
5	PORT2_POWER_GOOD	
4	PORT1_POWER_GOOD	
3	PORT4_POWER_ENABLE	PORTn_POWER_ENABLE correlates to PORTn FET ON / OFF Status. 0 = FET is turned OFF. 1 = FET is turned ON. After a PORTn_PB_POWER_ON, the PORTn_POWER_ENABLE is set after the Detection and Class Power On.
2	PORT3_POWER_ENABLE	
1	PORT2_POWER_ENABLE	
0	PORT1_POWER_ENABLE	

The main difference between the POWER_ENABLE and POWER_GOOD concepts is rooted in time delays.

Assume for a moment that both PORTn_POWER_ENABLE and PORTn_POWER_GOOD are both OFF, as an initial condition of this illustration.

When a PORTn_PB_POWER_ON is set, there is typically a delay from this pushbutton setting to when the Si3473/72 starts driving the GATE of the FET to turn it on. However, between PORTn_PB_POWER_ON and the GATE drive, the Si3473/72 may need to complete servicing other ports before starting to service the PORTn_PB_POWER_ON. Even if the Si3473/72 began servicing the PORTn_PB_POWER_ON, the port will still need to go through Detection and Class Power On before turning on the FET.

The PORTn_POWER_ENABLE is declared when the Si3473/72 drives the FET.

At this point, PORTn_POWER_ENABLE is ON, but PORTn_POWER_GOOD is still OFF. This effectively defines an initial start-up period where the port is allowed to current-limit for a short t_{INRUSH} duration in order to charge the PD capacitors. During this time, it is possible that the FET DRAIN would be folded-back to enforce this start-up current limit. Once the t_{INRUSH} period is over, if the DRAIN voltage is less than 2 V, the POWER_GOOD state is declared. Once in the POWER_GOOD state, both PORTn_POWER_ENABLE and PORTn_POWER_GOOD are turned ON.

At this point, monitoring of ILIM, PCUT, and DISCONNECTION events begins. Throughout this document, the POWER_GOOD state is sometimes used to distinguish between the initial t_{INRUSH} period and the long-term port monitoring of these events.

When a port is turned off, PORTn_POWER_ENABLE and PORTn_POWER_GOOD bits both change to OFF simultaneously.

POWER_ENABLE_CHANGE and POWER_GOOD_CHANGE are used to mark the transition time, as these transition times mark the status of the FET and the actions the Si3473/72 is performing to service the port.

3.11 PORT_MODE (0x12)

PORT_MODE				Register Address: 0x12 Access Type: Read / Write Reset: 0000 0000			
7	6	5	4	3	2	1	0
PORT_MODE		PORT_MODE		PORT_MODE		PORT_MODE	
PORT4		PORT3		PORT2		PORT1	

Bit	Name	Description
7-6	PORT4_PORT_MODE	PORTn_PORT_MODE Sets the main port operating mode. SEMI_AUTO is used in managed power use case. AUTO mode is used in unmanaged power use case. MANUAL mode is used generally for debug only. 00 = Set PORTn to SHUTDOWN Mode. 01 = Set PORTn to MANUAL Mode. 10 = Set PORTn to SEMI_AUTO Mode. 11 = Set PORTn to AUTO Mode. See 3.13 DETECT_CLASS_ENABLE (0x14) and 3.18 PB_POWER_ENABLE (0x19).
5-4	PORT3_PORT_MODE	
3-2	PORT2_PORT_MODE	
1-0	PORT1_PORT_MODE	

Setting PORTn_PORT_MODE to SHUTDOWN clears numerous port registers, and possibly the associated INTERRUPT bits. Refer to the description of PORTn_PB_POWER_OFF in PB_POWER_ENABLE for a list.

A host can set PORTn_PORT_MODE, but it also can be set to SHUTDOWN when RESET_QUAD is set.

After setting SEMI_AUTO in PORTn_PORT_MODE, PORTn_CLASS_ENABLE, and PORTn_DETECT_ENABLE, DETECT_ENABLE should also be set to begin continuous Detection and Class Probe. Refer to the DETECT_CLASS_ENABLE register for more details.

3.12 DISCONNECT_ENABLE (0x13)

DISCONNECT_ENABLE				Register Address: 0x13 Access Type: Read / Write Reset: 0000 1111			
7	6	5	4	3	2	1	0
				DISCONNECT_ENABLE			
				PORT4	PORT3	PORT2	PORT1

Bit	Name	Description
3	PORT4_DISCONNECT_ENABLE	PORTn_DISCONNECT_ENABLE Defines operation of a port in POWER GOOD state, whether or not to allow disconnection if the PD does not draw sufficient current and does not meet MPS requirements. Overcurrent and PCUT faults will still result in a disconnection. 0 = Keep port power even if PD current too low. 1 = Normal Disconnection Monitoring.
2	PORT3_DISCONNECT_ENABLE	
1	PORT2_DISCONNECT_ENABLE	
0	PORT1_DISCONNECT_ENABLE	

3.13 DETECT_CLASS_ENABLE (0x14)

DETECT_CLASS_ENABLE				Register Address: 0x14 Access Type: Read / Write Reset: 0000 0000			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CLASS_ENABLE				DETECT_ENABLE			
PORT4	PORT3	PORT2	PORT1	PORT4	PORT3	PORT2	PORT1

Bit	PORTn_CLASS_ENABLE	PORTn_DETECT_ENABLE	Description
7 / 3	PORT4_CLASS_ENABLE	PORT4_DETECT_ENABLE	PORTn_CLASS_ENABLE / PORTn_DETECT_ENABLE It is more useful to describe CLASS_ENABLE and DETECT_ENABLE together. CLASS_ENABLE is shown on the left; DETECT_ENABLE shown on the right. If PORTn_MODE in SEMI_AUTO 00 = No Operation 01 = Continuous Detection 10 = Not supported 11 = Continuous Detection and Class Probe If PORTn_MODE in AUTO 00 = No Operation 01 = Not supported 10 = Not supported 11 = Continuous Detection and Class Probe until a PD is detected. When a PD is detected, a Class Power On is initiated, followed by a turning on the port. In effect, it is as though the Si3473/72 received a PORTn_PB_POWER_ON. If PORTn_MODE in MANUAL Use PB_DETECT_CLASS instead If PORTn_MODE in SHUTDOWN Set up PORTn_PORT_MODE first
6 / 2	PORT3_CLASS_ENABLE	PORT3_DETECT_ENABLE	
5 / 1	PORT2_CLASS_ENABLE	PORT2_DETECT_ENABLE	
4 / 0	PORT1_CLASS_ENABLE	PORT1_DETECT_ENABLE	

PORTn_CLASS_ENABLE and PORTn_DETECT_ENABLE are cleared when the following occur:

1. PORTn_PORT_MODE is set to SHUTDOWN.
2. PORTn_RESET_PORT in PB_RESET is set.
3. RESET_QUAD is set.

The DETECT_CLASS_ENABLE register is intended for use only when PORTn_PORT_MODE is to SEMI_AUTO or AUTO.

If PORTn_PORT_MODE is set to MANUAL, the corresponding bits in PB_DETECT_CLASS are set; refer to PB_DETECT_CLASS for an operational description.

If PORTn_PORT_MODE is set to SHUTDOWN, PORTn_PORT_MODE must be initialized first, as this is an invalid operation.

3.14 POWER_PRIORITY_PCUT_DISABLE (0x15)

PORT_PRIORITY_PCUT_DISABLE				Register Address: 0x15 Access Type: Read / Write Reset: 0000 0000			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PORT_POWER_PRIORITY				DISABLE_PCUT			
PORT4	PORT3	PORT2	PORT1	PORT4	PORT3	PORT2	PORT1

Bit	Name	Description
7	PORT4_POWER_PRIORITY	PORTn_PORT_POWER_PRIORITY Defines the Port Power Priority for use when MULTIBIT_PRIORITY_ENABLE = 0. 0 = OSS event does not shut down PORTn. 1 = OSS event shuts down PORTn PORTn_PORT_POWER_PRIORITY is cleared when RESET_QUAD is set. An OSS event occurs when the OSS pin goes high. Every lower priority port experiences a PORTn_PB_POWER_OFF. Refer to PORTn_PB_POWER_OFF for additional details of what registers are cleared,
6	PORT3_POWER_PRIORITY	
5	PORT2_POWER_PRIORITY	
4	PORT1_POWER_PRIORITY	
3	PORT4_DISABLE_PCUT	PORTn_DISABLE_PCUT Defines operation of a port in the POWER GOOD state, specifying whether or not to power down PORTn if the PD exceeds port power limits defined in PORTn_POLICE_2P. Overcurrent faults and PD Disconnection will still result in a disconnection. 0 = Normal PCUT Monitoring. 1 = Keep port power even if PD exceeds POLICE register limits Although the port power is not removed, PORTn_PCUT_FAULT_2P events are reported, leading to an interrupt. The interrupt may be cleared by increasing the related PORTn_POLICE_2P registers.
2	PORT3_DISABLE_PCUT	
1	PORT2_DISABLE_PCUT	
0	PORT1_DISABLE_PCUT	

3.15 TIMING_CONFIG (0x16)

TLIM	Register Address: 0x16 Access Type: Read / Write Reset: 0000 0000						
7	6	5	4	3	2	1	0
TLIM		TSTART		TOVLD		TMPDO	
PORT1 to PORT4		PORT1 to PORT4		PORT1 to PORT4		PORT1 to PORT4	

Bit	Name	Description
7-6	TLIM	ILIM FAULT Timing Specifies minimum t_{LIM} when PORTn_MAX_ILIM is set. This setting defines the minimum period for which an overcurrent event is tolerated without turning off the port. This setting applies for all ports in the quad. 00 = 60 ms 01 = 15 ms 10 = 10 ms 11 = 6 ms
5-4	TSTART	START FAULT Timing When the port is powering up, if the port is still current limiting after the t_{INRUSH} period, the port is shut off. This setting applies for all ports in the quad 00 = 60 ms 01 = 30 ms 10 = 120 ms 11 = Reserved
3-2	TOVLD	PCUT FAULT Timing A PD drawing power that exceeds the policing power limits for longer than t_{OVLD} will result in the port being shut off. This setting applies for all ports in the quad. 00 = 60 ms 01 = 30 ms 10 = 120 ms 11 = 240 ms
1-0	TMPDO	DISCONNECTION Delay Timing A PD drawing too little current for longer than the t_{MPDO} will result in a disconnection. This setting applies to all ports in the quad. 00 = 360 ms 01 = 90 ms 10 = 180 ms 11 = 720 ms

3.16 MISC (0x17)

MISC				Register Address: 0x17 Access Type: Read / Write Reset: 1000 0000			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
INTER-RUPT_PIN_ENABLE	—	—	MULTI-BIT_PRIORI-TY_ENABLE	CLASS_CHANGE	DE-TECT_CHANGE	MIDSPAN	—

Bit	Name	Description
7	INTERRUPT_PIN_ENABLE	Enables INTb pin output drive. 0 = Enable 1 = Disable
4	MULTIBIT_PRIORITY_ENABLE	Enables Multibit Port Priority. 0 = Single Bit Port Priority. See also PORTn_PORT_POWER_PRIORITY. 1 = Multibit Port Priority. See also PORTn_MULTIBIT_PRIORITY.
3	CLASS_CHANGE	Defines whether CLASS_DONE events in the CLASS_DETECT_STATUS register are set whenever the PORTn_CLASS_STATUS is updated, or only when it changes. 0 = Report CLASS_DONE when CLASS_STATUS is updated. 1 = Report CLASS_DONE when CLASS_STATUS changes.
2	DETECT_CHANGE	Defines whether the DETECT_DONE events in CLASS_DETECT_STATUS register are set whenever the PORTn_DETECTION_STATUS is updated, or only if it changes. 0 = Report DETECT_DONE when DETECTION_STATUS is updated. 1 = Report DETECT_DONE when DETECTION_STATUS changes.
1	MIDSPAN	0 = Endspan (Mode A, typically a PoE enabled Ethernet switch) 1 = Midspan (Mode B, typically a PoE injector)

3.17 PB_DETECT_CLASS (0x18)

PB_DETECT_CLASS				Register Address: 0x18 Access Type: Write Only Reset: 0000 0000			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESTART_CLASS				RESTART_DETECT			
PORT4	PORT3	PORT2	PORT1	PORT4	PORT3	PORT2	PORT1

Bit	PORTn_RESTART_CLASS	PORTn_RESTART_DETECT	Description
7 / 3	PORT4_RESTART_CLASS	PORT4_RESTART_DETECT	PORTn_RESTART_CLASS / PORTn_RESTART_DETECT It is best to view RESTART_CLASS and RESTART_DETECT together. As a shortcut, RESTART_CLASS will be shown below as the 'left bit', while RESTART_DETECT is shown as the 'right' bit. The intended use case of this register is in MANUAL mode. By definition, MANUAL mode is used for debug only. 00 - No operation 01 - Single Detection 10 - Invalid Setting 11 - Single Detection and Classification without powering the port (e.g., Class Probe).
6 / 2	PORT3_RESTART_CLASS	PORT3_RESTART_DETECT	
5 / 1	PORT2_RESTART_CLASS	PORT2_RESTART_DETECT	
4 / 0	PORT1_RESTART_CLASS	PORT1_RESTART_DETECT	

PB_DETECT_CLASS is intended for use when PORTn_PORT_MODE is MANUAL and is not intended for use in SEMI_AUTO or AUTO modes.

However, if PB_DETECT_CLASS is used while the PORTn_PORT_MODE is set to SEMI_AUTO or AUTO, the respective bits are transferred over to the DETECT_CLASS_ENABLE register.

3.18 PB_POWER_ENABLE (0x19)

PB_POWER_ENABLE				Register Address: 0x19 Access Type: Write Only Reset: 0000 0000			
7	6	5	4	3	2	1	0
PB_POWER_OFF				PB_POWER_ON			
PORT4	PORT3	PORT2	PORT1	PORT4	PORT3	PORT2	PORT1

Bit	Name	Description
7	PORT4_PB_POWER_OFF	PORTn_PB_POWER_OFF Initiates Pushbutton OFF. 0 = Do Nothing 1 = Power OFF PORT n
6	PORT3_PB_POWER_OFF	
5	PORT2_PB_POWER_OFF	
4	PORT1_PB_POWER_OFF	
3	PORT4_PB_POWER_ON	PORTn_PB_POWER_ON Initiates Pushbutton ON. 0 = Do Nothing 1 = Power ON PORT n
2	PORT3_PB_POWER_ON	
1	PORT2_PB_POWER_ON	
0	PORT1_PB_POWER_ON	

When a PORTn_PB_POWER_OFF bit is set, all bits associated with the PORTn being Powered OFF are set to their default reset values, which are mostly cleared, with a few exceptions. This also applies to OSS_EVENT, PORTn_RESET_PORT and when PORTn_PORT_MODE is set to SHUTDOWN.

- PORTn_POWER_ENABLE
- PORTn_POWER_GOOD
- PORTn_CLASS_DONE
- PORTn_DETECT_DONE
- PORTn_DISCONNECTION
- PORTn_PCUT_FAULT_2P
- PORTn_ILIM_FAULT
- PORTn_START_FAULT
- PORTn_CLASS_STATUS
- PORTn_DETECTION_STATUS
- PORTn_POWER_ON_FAULT
- PORTn_CURRENT
- PORTn_VOLTAGE
- PORTn_PGOOD_FOLDBACK
- PORTn_INRUSH_FOLDBACK
- PORTn_DETECT_RESISTANCE
- PORTn_DETECT_CAPACITANCE
- PORTn_ASSIGNED_CLASS
- PORTn_REQUESTED_CLASS
- PORTn_AUTOCLASS_POWER
- PORTn_POLICE_2P

If a host sets a PORTn_PB_POWER_ON and PORTn_PORT_MODE is in SEMI_AUTO, it is expected that PORTnm_PORT_ALLOCATION, PORTn_CLASS_ENABLE, and PORTn_DETECT_ENABLE are already initialized.

Detection and Class Probes that have already started are allowed to complete first. A new Detection and Classification are performed before the FET is finally turned on. If any faults occur prior to FET turn on, they are reported as PORTn_POWER_ON_FAULT events.

Once the FET is turned on, PORTn_POWER_ENABLE is set. There is a short Inrush Period to allow the PD to charge its capacitors. After the Inrush Period, if the PORTn DRAIN voltage does not settle to under 2 V, the port is disconnected and a PORTn_START_FAULT is issued.

On the other hand, if the DRAIN voltage is under 2V, PORTn_POWER_GOOD is issued and the port reaches the POWER_GOOD state.

PORTn_POLICE_2P is initialized automatically based on PORTn_ASSIGNED_CLASS. These registers are used later to check if the PD is exceeding its power budget. If the PD exceeds the negotiated power thresholds, PORTn_PCUT_FAULT_2P events will occur.

If PORTn_AUTO_AUTOCLASS is set and if the PD is Autoclass-capable, PORTn_POLICE_2P is updated based on PORTn_AUTOCLASS_POWER. At any time after the Si3473/72 updates the PORTn_POLICE_2P registers, a host can choose to manage power by overwriting these police registers. A host can compute actual PD power by monitoring PORTn_CURRENT and PORTn_VOLTAGE and may choose to increase or decrease port power as part of its power management scheme.

If a host chooses to decrease police registers, it may choose to also set the PORTn_DISABLE_PCUT so that it can be informed if a PD exceeds the police register thresholds without turning off power to the PD.

In addition, the Si3473/72 also monitors for disconnections (PORTn_DISCONNECTION) and current limit events (PORTn_ILIM_FAULT).

Typically, it is expected that PORTn_PB_POWER_ON is set in conjunction with PORTn_CLASS_ENABLE and PORTn_DETECT_ENABLE. However, there is a special use case in MANUAL mode that would allow Detection and Classification to be skipped. If a host sets PORTn_PB_POWER_ON with PORTn_PORT_MODE in MANUAL mode, and if PORTn_CLASS_ENABLE = 0 and PORTn_DETECT_ENABLE = 0, then Detection and Classification are all skipped and the port is powered on immediately. Then PORTn_POLICE_2P and are initialized based on PORTnm_POWER_ALLOCATION instead of PORTn_ASSIGNED_CLASS.

3.19 PB_RESET (0x1A)

PB_RESET				Register Address: 0x1A Access Type: Write Only Reset: 0000 0000			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CLEAR_ALL_INTS	CLEAR_INT_PIN		RESET_QUAD	RESET_PORT			
EIGHT PORTS	NONE		PORT1 to PORT4	PORT4	PORT3	PORT2	PORT1

Bit	Name	Description
7	CLEAR_ALL_INTS	Clears the INTb pin by clearing all events on all Quads. 0 = Do Nothing 1 = Clear all events in all ports (all Quads) and negate INTb
6	CLEAR_INT_PIN	Clears the INTb pin directly in hardware without affecting any event bits. 0 = Do Nothing 1 = Clear INTb pin
4	RESET_QUAD	Registers in the current quad are initialized to Reset defaults. Registers in other quad are unaffected. 0 = Do Nothing 1 = Reset registers in the Quad to reset defaults
3	PORT4_RESET_PORT	PORTn_RESET_PORT Initiates Port Reset 0 = Do Nothing 1 = Associated PORTn Registers are set to Reset default values Refer to PORTn_PB_POWER_OFF for a list of register Reset default values. If the port is powered, it will be shut off.
2	PORT3_RESET_PORT	
1	PORT2_RESET_PORT	
0	PORT1_RESET_PORT	

PORTn_RESET_PORT clears event registers similar to that of PORTn_PB_POWER_OFF. If PORTn is powered, the port will be shut off. Refer to PORTn_PB_POWER_OFF for the list of registers set to Reset default values. The main difference between PORTn_RESET_PORT and PORTn_PB_POWER_OFF is that PORTn_RESET_PORT may be used regardless of the PORTn_PORT_MODE setting.

3.20 VENDOR_ID (0x1B), FIRMWARE_REVISION (0x41), CHIP_REVISION (0x43)

VENDOR_ID				Register Address: 0x1B Access Type: Read Only			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MANUFACTURER_ID					IC_ID		
0	1	0	0	0	1	0	1

FIRMWARE_REVISION				Register Address: 0x41 Access Type: Read Only			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MAJOR_REVISION				MINOR_REVISION			
?	?	?	?	?	?	?	?

CHIP_REVISION				Register Address: 0x43 Access Type: Read Only			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CHIP_REVISION							
DEVICE_ID				SILICON_REVISION		SENSE_RESISTOR	

Bit	Name	Description
7-4	DEVICE_ID	0011 = Si3472 0100 = Si3473
3-2	SILICON_REVISION	00, Incremented if revisions are needed
1-0	SENSE_RESISTOR	00 = 200 Ω 01 = 255 Ω 10 = 150 Ω 11 = 100 Ω

The purpose of MANUFACTURER_ID in the VENDOR_ID register is to allow a host to determine the manufacturer of the device in the presence of a multi-source design. This allows a host to make adjustments to its software based on chip behavior across different vendors. The DEVICE_ID defines the product as an Si347x-Class device. Together, the MANUFACTURER_ID and the DEVICE_ID is an overall identifier of a class of chips that may be similar to competitive offerings.

The VENDOR_ID is therefore static and does not change across revisions in either hardware or firmware.

The CHIP_REVISION tracks Si3473/72 hardware revisions.

The FIRMWARE_REVISION tracks firmware revisions. The upper nibble is a "major" revision, while the lower nibble is a "minor" revision.

Table 3.2.

Ordering Part Number	Chip Revision	DEVICE_ID	SENSE_RESISTOR
Si3472A-A01-IM	0x31	0011	01
Si3472B-A01-IM	0x30	0011	00
Si3473A-A01-IM	0x41	0100	01

Ordering Part Number	Chip Revision	DEVICE_ID	SENSE_RESISTOR
Si3473B-A01-IM	0x40	0100	00

3.21 AUTOCLASS (0x1C)

AUTOCLASS				Register Address: 0x1C Access Type: Read / Write Reset: 0000 0000			
7	6	5	4	3	2	1	0
AUTOCLASS_DETECTED				Reserved			
PORT4	PORT3	PORT2	PORT1	—			

Bit	Name	Description
7	PORT4_AUTOCLASS_DETECTED	PORTn_AUTOCLASS_DETECTED Indicates that the PD is Autoclass-capable and that the Classification occurred on PORTn 0 = PD not Autoclass-capable 1 = PD is Autoclass-capable
6	PORT3_AUTOCLASS_DETECTED	
5	PORT2_AUTOCLASS_DETECTED	
4	PORT1_AUTOCLASS_DETECTED	
3	Reserved	
2		
1		
0		

3.22 PORT1_POLICE_2P to PORT4_POLICE_2P (0x1E – 0x21)

Name	Address	Access Type	Reset	7	6	5	4	3	2	1	0
PORT1_POLICE_2P	0x1E	R/W	1111 1111	PORTn_POLICE_2P Minimum 2P PCUT Threshold (Watts) = PORTn_POLICE_2P * 0.5 W							
PORT2_POLICE_2P	0x1F	R/W	1111 1111								
PORT3_POLICE_2P	0x20	R/W	1111 1111								
PORT4_POLICE_2P	0x21	R/W	1111 1111								

PORTn_POLICE_2P registers are initialized by the Si3473/72 as part of PORTn_PB_POWER_ON. PORTnm_POWER_ALLOCATION, in conjunction with the PD Requested Class, will negotiate to an ASSIGNED_CLASS. The PCUT thresholds are then set by the Si3473/72.

Any of these police registers can be adjusted based on the actual power used by the port. Once the port has achieved a POWER_GOOD state, the police registers can be written and the Si3473/72 will then evaluate power thresholds as set by these police registers.

It is important to note that the power values represented in the police register interfaces are the MINIMUM threshold. The actual internal thresholds are increased by 5%.

PORTn_POLICE_2P are set to Reset default values when:

1. Setting PORTn_PORT_MODE = SHUTDOWN
2. Setting PORTn_PB_POWER_OFF
3. Setting PORTn_RESET_PORT
4. Setting RESET_QUAD
5. OSS Event

3.23 PORT_REMAP (0x26)

PORT_REMAP				Register Address: 0x26 Access Type: Read / Write Reset: 11 10 01 00			
7	6	5	4	3	2	1	0
REMAP		REMAP		REMAP		REMAP	
PORT4		PORT3		PORT2		PORT1	

Bit	Name	Description
7-6	PORT4_REMAP	PORTn_REMAP PORTn_REMAP defines the physical pins used when referencing the logical concept called "PORTn" 00 = Use physical pins GATE1, DRAIN1, SENSE1 01 = Use physical pins GATE2, DRAIN2, SENSE2 10 = Use physical pins GATE3, DRAIN3, SENSE3 11 = Use physical pins GATE4, DRAIN4, SENSE4 PORTn_REMAP must use a single write to PORT_REMAP, immediately after reset. For example, the concept called "PORT4", by default, uses DRAIN4. The PORT4_REMAP field is therefore ‘11’.
5-4	PORT3_REMAP	
3-2	PORT2_REMAP	
1-0	PORT1_REMAP	

The port remapping feature allows a host to rearrange the sequencing of the Si3473/72 ports so that it better aligns to the end product’s port alignment. Be aware that a Physical Port must appear, and may only appear, in one Logical Port.

Figure 3.1 RJ45 Example Layouts on page 57 shows a graphic illustration of how to create a logical-to-physical mapping by first starting with a sketch of how the DRAIN pins might line up to the RJ45 jacks. If the same physical pin code is assigned to more than one PORTn_REMAP field, the Si3473/72 rejects the setting. It is best to confirm if the Si3473/72 accepted the remap setting by reading back the PORT_REMAP register.

The PORT_REMAP register is one of two registers that must be written once immediately after reset. Even if the intention is to use the default PORT_REMAP, PORT_REMAP must be written with 0xE4. Without this, the Si3473/72 will not function. Once PORT_REMAP is written, ONLY a hardware reset can be used to allow PORT_REMAP to be written again.

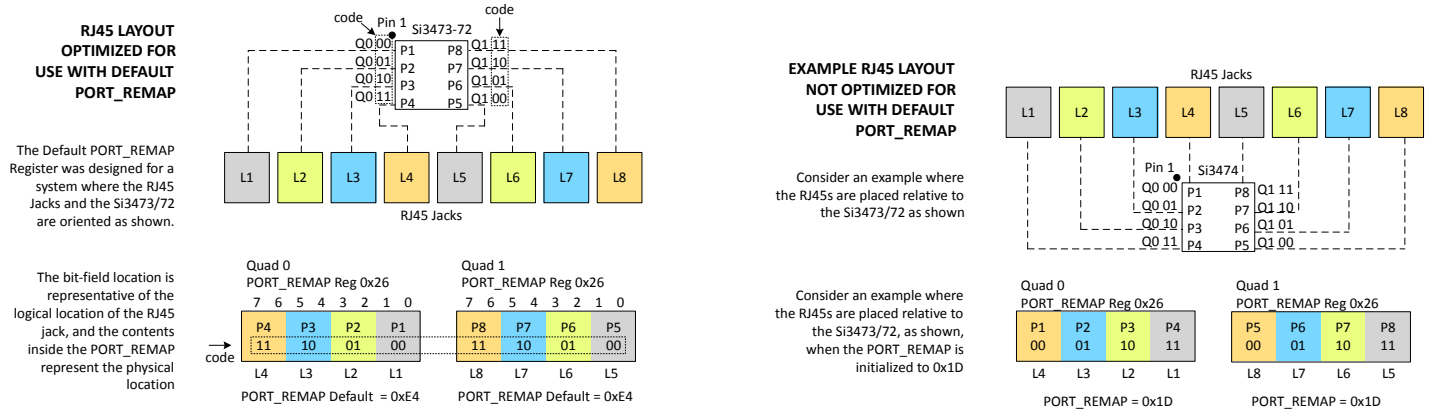


Figure 3.1. RJ45 Example Layouts

3.24 PORTn_MULTIBIT_PRIORITY (0x27, 0x28)

Name	Address	Access Type	Reset	7	6	5	4	3	2	1	0
PORT1_PORT2_MULTIBIT_PRIORITY	0x27	R/W	0000 0000	PORT2_MULTIBIT_PRIORITY				PORT1_MULTIBIT_PRIORITY			
PORT3_PORT4_MULTIBIT_PRIORITY	0x28	R/W	0000 0000	PORT4_MULTIBIT_PRIORITY				PORT3_MULTIBIT_PRIORITY			

Address	Bit	Name	Description
0x27	6-4	PORT2_MULTIBIT_PRIORITY	PORTn_MULTIBIT_PRIORITY MULTIBIT_PRIORITY_ENABLE in MISC register must be set for PORTn_MULTIBIT_PRIORITY to take effect. PORTn_MULTIBIT_PRIORITY defines the OSS Code needed to turn PORTn off. 111 = Receiving OSS Code 111 or lower shuts down PORTn (lowest priority). 110 = Receiving OSS Code 110 or lower shuts down PORTn. 101 = Receiving OSS Code 101 or lower shuts down PORTn. 100 = Receiving OSS Code 100 or lower shuts down PORTn. 011 = Receiving OSS Code 011 or lower shuts down PORTn. 010 = Receiving OSS Code 010 or lower shuts down PORTn. 001 = Receiving OSS Code 001 or lower shuts down PORTn. 000 = Receiving OSS Code 000 shuts down the port (highest priority). Note that the higher the PORTn_MULTIBIT_PRIORITY setting, the more OSS Codes that can shut it down. As such, the lower the PORTn_MULTIBIT_PRIORITY is, the higher the priority of the port.
0x27	2-0	PORT1_MULTIBIT_PRIORITY	
0x28	6-4	PORT4_MULTIBIT_PRIORITY	
0x28	2-0	PORT3_MULTIBIT_PRIORITY	

If MULTIBIT_PRIORITY_ENABLE = 1, then PORT1_PORT2_MULTIBIT_PRIORITY and PORT3_PORT4_MULTIBIT_PRIORITY defines port power priority and governs OSS action. See 2.7.3 Class Power On for figures showing the operation and timing diagram of the OSS pin in multi-bit mode. The most significant bit is sent first. The priority for PORTn is defined with the three bits specified by PORTn_MULTIBIT_PRIORITY. A port whose priority setting is ‘000’ has the highest priority; a priority setting of ‘111’ has the lowest priority. When a host system wants certain priority ports shut down, it will transmit the “shutdown code” over the OSS pin. Ports whose port priority settings are greater than or equal to the received shutdown code will be turned off. For example, a received OSS shutdown code of ‘101’ will shut down ports whose port priority settings are ‘101’, ‘110’ or ‘111’.

3.25 POWER_ALLOCATION (0x29)

POWER _ALLOCATION				Register Address: 0x29 Access Type: Read / Write Reset: 0000 0000			
7	6	5	4	3	2	1	0
—	POWER_ALLOCATION			—	POWER_ALLOCATION		
PORT34				PORT12			

Bit	Name	Description
6-4	PORT34_POWER_ALLOCATION	PORTnm_POWER_ALLOCATION
2-0	PORT12_POWER_ALLOCATION	

PORTnm_POWER_ALLOCATION			2PP Port
Bit 2	Bit 1	Bit 0	
0	0	0	15 W Class 3
0	0	1	4 W Class 1
0	1	0	7 W Class 2
0	1	1	30 W Class 4
1	0	0	RESERVED
1	0	1	45W Class 5 Legacy[1]
1	1	X	RESERVED

Note:

1. The Class 5 Legacy setting allows the PSE to provide Class 5 power to a PD that presents a Classification current between 51 mA and 60 mA. This behavior is not defined in the IEEE 802.3bt specification.

3.26 TEMPERATURE (0x2C)

TEMPERATURE				Register Address: 0x2C Access Type: Read Only Reset: xxxx xxxx[1]			
7	6	5	4	3	2	1	0
TEMPERATURE Approximate Chip Temperature in Centigrade according to this formula: (TEMPERATURE * 0.652) – 20							

Note:

1. x = undefined after reset.

3.27 Parametric Measurement Registers (0x2E – 0x3F)

VPWR, PORTn_VOLTAGE and PORTn_CURRENT are each 14-bit registers straddled across two bytes.

A host must use an SMBus Burst Read of 16-bits, so with proper LSB / MSB pairing. Improper LSB / MSB pairing will result in a 256 code error if the measurement happens to be near a multiple of 256.

All of the 16-bit registers begin on even bytes. The SMBus Burst Read should therefore have an even Register Address. The first byte returned from the SMBus Read is the LSB, followed by the MSB.

VPWR can be read at any time.

PORTn_VOLTAGE and PORTn_CURRENT can be read as long as the port is in a POWER_GOOD state. PORTn_VOLTAGE and PORTn_CURRENT are cleared when any of the following occur:

1. PORTn_PORT_MODE = SHUTDOWN
2. PORTn_PB_POWER_OFF = 1
3. PORTn_RESET_PORT = 1
4. An OSS_EVENT
5. RESET_QUAD = 1

3.28 VPWR, PORT1_VOLTAGE, PORT2_VOLTAGE, PORT3_VOLTAGE, PORT4_VOLTAGE (0x2E/0x2F, 0x32/0x33, 0x36/0x37, 0x3A/0x3B, 0x3E/0x3F)

Name	Address	Access Type	Reset	7	6	5	4	3	2	1	0
VPWR_LSB	0x2E	RO	xxxx xxxx[1]	VPWR Voltage (in volts) = 60 * ((VPWR_MSB << 8) + VPWR_LSB) / 16384							
VPWR_MSB	0x2F	RO	00xx xxxx[1]								
PORT1_VOLTAGE_LSB	0x32	RO	0000 0000	PORTn Voltage (in volts) = 60 * ((PORTn_VOLTAGE_MSB << 8) + PORTn_VOLTAGE_LSB) / 16384							
PORT1_VOLTAGE_MSB	0x33	RO	0000 0000								
PORT2_VOLTAGE_LSB	0x36	RO	0000 0000								
PORT2_VOLTAGE_MSB	0x37	RO	0000 0000								
PORT3_VOLTAGE_LSB	0x3A	RO	0000 0000								
PORT3_VOLTAGE_MSB	0x3B	RO	0000 0000								
PORT4_VOLTAGE_LSB	0x3E	RO	0000 0000								
PORT4_VOLTAGE_MSB	0x3F	RO	0000 0000								

Note:

1. x = undefined after reset.

3.29 PORT1_CURRENT, PORT2_CURRENT, PORT3_CURRENT, PORT4_CURRENT (0x30/0x31, 0x34/0x35, 0x38/0x39, 0x3C/0x3D)

Name	Address	Access Type	Reset	7	6	5	4	3	2	1	0
PORT1_CURRENT_LSB	0x30	RO	0000 0000	PORTn Current (in mA) = 1000 * ((PORTn_CURRENT_MSB << 8) + PORTn_CURRENT_LSB) / 16384							
PORT1_ CURRENT _MSB	0x31	RO	0000 0000								
PORT2_ CURRENT _LSB	0x34	RO	0000 0000								
PORT2_ CURRENT _MSB	0x35	RO	0000 0000								
PORT3_ CURRENT _LSB	0x38	RO	0000 0000								
PORT3_ CURRENT _MSB	0x39	RO	0000 0000								
PORT4_ CURRENT _LSB	0x3C	RO	0000 0000								
PORT4_ CURRENT _MSB	0x3D	RO	0000 0000								

3.30 MAX_ILIM_MANUAL_POLICE (0x40)

MAX_ILIM_MANUAL_POLICE				Register Address: 0x40 Access Type: Read / Write Reset: 0000 0000			
7	6	5	4	3	2	1	0
MAX_ILIM				MANUAL_POLICE			
PORT4	PORT3	PORT2	PORT1	PORT4	PORT3	PORT2	PORT1

Bit	Name	Description
7	PORT4_MAX_ILIM	PORTn_MAX_ILIM Sets the port's current limit to the maximum possible setting allowed by the Si3473/72 0 = Port Current Limit not yet maximized 1 = Max Port Current Limit When the port is in a POWER_GOOD state, the PORTn_MAX_ILIM is set by the device if the highest (1275 mA) current limit setting is used. For the ports whose PORTn_MAX_ILIM is zero, a host can set it to 1 to maximize the current limit to 1275 mA. When set, the PORTn_TLIM setting is enforced. The PORTn_PGOOD_FOLDBACK register is also used.
6	PORT3_MAX_ILIM	
5	PORT2_MAX_ILIM	
4	PORT1_MAX_ILIM	
3	PORT4_MANUAL_POLICE	PORTn_MANUAL_POLICE Defines ports for which the police register settings are manually set 0 = The police registers are updated automatically based on a PD's assigned class 1 = The police registers are initialized by a host before PORTn_PB_POWER_ON. A host is responsible for maintaining the police registers.
2	PORT3_MANUAL_POLICE	
1	PORT2_MANUAL_POLICE	
0	PORT1_MANUAL_POLICE	

3.31 I2C_WATCHDOG (0x42)

I2C_WATCHDOG							Register Address: 0x42 Access Type: Read / Write Reset: 000 1011 0
7	6	5	4	3	2	1	0
0	0	0	WATCHDOG_DISABLE				WATCHDOG_STATUS

Bit	Name	Description
4-1	WATCHDOG_DISABLE	WATCHDOG_DISABLE Enables the I²C Watchdog 1011 = Disable the I²C Watchdog NOT 1011 = Enable the I²C Watchdog
0	WATCHDOG_STATUS	0 = I²C Watchdog did not occur 1 = I²C Watchdog occurred

The Si3473/72 implements an I²C transaction watchdog. The I²C transaction watchdog is disabled by default and can be enabled by setting WATCHDOG_DISABLE to any bit pattern except 0xB. When WATCHDOG_DISABLE is set, the transaction watchdog will begin a 50 ms timer whenever an I²C Start Bit is detected. If an I²C Stop Bit is not detected within the 50 ms time period, the Si3473/72 restarts the I²C subsystem and performs an action equivalent to RESET_QUAD. This results in all ports being shut off.

Once the WATCHDOG_STATUS bit is set, it remains set until a host sets it to 0.

The main benefit of enabling the I²C WATCHDOG feature is to allow recovery if an I²C miscommunication results in the Si3473/72 entering a "stuck" state where it continuously asserts the SDA pin.

Consider this condition as an example of how the Si3473/72 could end up asserting the SDA continuously:

Although an I²C fault leads to the powering down of all ports, it places the Si3473/72 in a known state, ready for a host to reinitialize and start anew.

3.32 DETECT_RESISTANCE (0x44 – 0x47)

Name	Address	Access Type	Reset	7	6	5	4	3	2	1	0
PORT1_DETECT_RESISTANCE	0x44	RO	0000 0000	PORTn PD RESISTANCE (in kΩ) = (50/256) * PORTn_DETECT_RESISTANCE							
PORT2_DETECT_RESISTANCE	0x45	RO	0000 0000								
PORT3_DETECT_RESISTANCE	0x46	RO	0000 0000								
PORT4_DETECT_RESISTANCE	0x47	RO	0000 0000								

3.33 DETECT_CAPACITANCE (0x48 – 0x4B)

Name	Address	Access Type	Reset	7	6	5	4	3	2	1	0
PORT1_DETECT_CAPACITANCE	0x48	RO	0000 0000	PORTn PD Capacitance (in uF) = PORTn_DETECT_CAPACITANCE * 0.05							
PORT2_DETEC_CAPACITANCE	0x49	RO	0000 0000								
PORT3_DETECT_CAPACITANCE	0x4A	RO	0000 0000								
PORT4_DETECT_CAPACITANCE	0x4B	RO	0000 0000								

3.34 CLASS_RESULTS (0x4C – 0x4F)

Name	Address	Access Type	Reset	7	6	5	4	3	2	1	0
PORT1_CLASS_RESULTS	0x4C	RO	0000 0000	ASSIGNED_CLASS				REQUESTED_CLASS			
PORT2_CLASS_RESULTS	0x4D	RO	0000 0000	ASSIGNED_CLASS				REQUESTED_CLASS			
PORT3_CLASS_RESULTS	0x4E	RO	0000 0000	ASSIGNED_CLASS				REQUESTED_CLASS			
PORT4_CLASS_RESULTS	0x4F	RO	0000 0000	ASSIGNED_CLASS				REQUESTED_CLASS			

Address	Bit	Name	Description
0x4C	7 - 4	PORT1_ASSIGNED_CLASS	PORTn_ASSIGNED_CLASS The assigned class represents the result of Class Power On initiated by a PORTn_PB_POWER_ON
0x4D	7 – 4	PORT2_ASSIGNED_CLASS	
0x4E	7 – 4	PORT3_ASSIGNED_CLASS	
0x4F	7 – 4	PORT4_ASSIGNED_CLASS	
0x4C	3 - 0	PORT1_REQUESTED_CLASS	PORTn_REQUESTED_CLASS When a PORTn_PB_POWER_ON event is issued, the most recent Class Probe results are stored here. The Class Probe results are effectively the requested class.
0x4D	3 - 0	PORT2_REQUESTED_CLASS	
0x4E	3 - 0	PORT3_REQUESTED_CLASS	
0x4F	3 - 0	PORT4_REQUESTED_CLASS	

The following table aims to provide a summary of when values can be expected in the various fields that may contain Classification information.

Table 3.3. Classification Event Timing

Classification Code	PORTn_CLASS_STATUS	PORTn_REQUESTED_CLASS	PORTn_ASSIGNED_CLASS	Comments
0000	UNKNOWN	UNKNOWN	UNKNOWN	
0001	Class 1	Class 1	Class 1	
0010	Class 2	Class 2	Class 2	
0011	Class 3	Class 3	Class 3	
0100	Class 4	Class 4	Class 4	
0101				
0110	Class 0	Class 0		If Class 0 is requested, it is converted to Class 3
0111	Overcurrent (greater than 60 mA)			
1001	—	—	—	
1010	—	—	—	
1011	—	—	—	
1100	Class 4+ Type 1 limited			Requested Class ≥ CLASS_4, demoted to CLASS_3
1101	Overcurrent (between 51 mA and 60 mA)	Legacy Class 5	Legacy Class 5	PB_POWER_ON with Class 5 POWER_ALLOCATION treats currents between 51 mA and 60 mA as a Class 5 PD
1110	—	—	—	
1111	Class mismatch			This is a temporary status setting as Classification is repeated

Note:

1. Red Text: Possible if Class Power On is unsuccessful (PORTn_POWER_ON_FAULT in POWER_ON_FAULT register).
2. Green Text: Updated during Class Probe (PORTn_CLASS_DONE in CLASS_DETECT_STATUS).
3. Blue Text: Updated during Class Power On (PORTn_POWER_GOOD in POWER_STATUS register).
4. All Initialized to UNKNOWN after:
   - PORTn_PORT_MODE = SHUTDOWN
   - PORTn_PB_POWER_OFF = 1
   - PORTn_RESET_PORT = 1
   - An OSS_EVENT
   - RESET_QUAD = 1

3.35 AUTOCLASS_CONTROL (0x50)

AUTOCLASS_CONTROL				Register Address: 0x50 Access Type: Read / Write Reset: 0000 0000			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MANUAL_AUTOCLASS				AUTO_AUTOCLASS			
PORT4	PORT3	PORT2	PORT1	PORT4	PORT3	PORT2	PORT1

Bit	Name	Description
7	PORT4_MANUAL_AUTO-CLASS	PORTn_MANUAL_AUTOCLASS Initiates an Autoclass measurement. 0 = No Action 1 = Manually initiate an Autoclass power measurement. After being set, PORTn_MANUAL_AUTOCLASS will clear itself when the result in PORTn_AUTOCLASS_POWER is ready. It is recommended that a host make use of this auto-clearing behavior to determine that PORTn_AUTOCLASS_POWER is ready to be read. Once PORTn_AUTOCLASS_POWER is updated, a host may add some margin, then update the related PORTn_POLICE_2P register.
6	PORT3_MANUAL_AUTO-CLASS	
5	PORT2_MANUAL_AUTO-CLASS	
4	PORT1_MANUAL_AUTO-CLASS	
3	PORT4_AUTO_AUTOCLASS	PORTn_AUTO_AUTOCLASS PORTn_AUTO_AUTOCLASS Enable 0 = Disable AUTO Autoclass 1 = Enables AUTO Autoclass PORTn_AUTO_AUTOCLASS must be initialized before initiating PORTn_PB_POWER_ON. In the presence of an Autoclass-capable PD, the related PORTn_POLICE_2P register is updated based on some margin in addition to the measurement stored in PORTn_AUTOCLASS_POWER.
2	PORT3_AUTO_AUTOCLASS	
1	PORT2_AUTO_AUTOCLASS	
0	PORT1_AUTO_AUTOCLASS	

PORTn_AUTO_AUTOCLASS must be set prior to a PORTn_PB_POWER_ON.

An Autoclass procedure is performed during Class Power On due to a PORTn_PB_POWER_ON. If the Si3473/72 detects an Autoclass request from a PD, PORTn_AUTOCLASS_DETECTED is set.

Once the PORT has reached POWER_GOOD, the PD is expected to draw its maximum power during the first few seconds after powering up. The Si3473/72 automatically measures the PD's power consumption and updates the police registers based on the measured power.

In the 802.3bt standard, it is possible to perform a manual Autoclass procedure between the PSE and PD through Data Link Layer messaging. A host can set the PORTn_MANUAL_AUTOCLASS when the PD is expected to be drawing full power as part of this Data Link Layer Autoclass protocol. Once PORTn_MANUAL_AUTOCLASS is set, the Si3473/72 performs a power measurement. Once the power measurement is ready, PORTn_MANUAL_AUTOCLASS is cleared as an indicator to a host that the PORTn_AUTO-CLASS_POWER is ready.

If a manual autoclass measurement is made, the police registers are not updated, and it is a host's responsibility to set up the various police registers based on the PORTn_AUTOCLASS_POWER results.

3.36 PORT1_AUTOCLASS_RESULTS, PORT2_AUTOCLASS_RESULTS, PORT3_AUTOCLASS_RESULTS, PORT4_AUTOCLASS_RESULTS (0x51 – 0x54)

Name	Addr	Access Type	Reset	7	6	5	4	3	2	1	0
PORT1_AUTOCLASS_RESULTS	0x51	RO	0000 0000	0	AUTOCLASS_POWER						
PORT2_AUTOCLASS_RESULTS	0x52	RO	0000 0000	0	AUTOCLASS_POWER						
PORT3_AUTOCLASS_RESULTS	0x53	RO	0000 0000	0	AUTOCLASS_POWER						
PORT4_AUTOCLASS_RESULTS	0x54	RO	0000 0000	0	AUTOCLASS_POWER						

Addr	Bit	Name	Description
0x51	6 - 0	PORT1_AUTOCLASS_POWER	PORTn_AUTOCLASS_POWER Holds the AUTOCLASS_POWER information Power (in Watts) = PORTn_AUTOCLASS_POWER * 0.5
0x52	6 - 0	PORT2_AUTOCLASS_POWER	
0x53	6 - 0	PORT3_AUTOCLASS_POWER	
0x54	6 - 0	PORT4_AUTOCLASS_POWER	

3.37 ALTERNATIVE_FOLDBACK (0x55)

ALTERNATIVE_FOLDBACK

Register Address: 0x50

Access Type: Read / Write

Reset: 0000 0000

7	6	5	4	3	2	1	0
PGOOD_FOLDBACK				INRUSH_850MA			
PORT4	PORT3	PORT2	PORT1	PORT4	PORT3	PORT2	PORT1

Bit	Name	Description
7	PORT4_PGOOD_FOLDBACK	PORTn_PGOOD_FOLDBACK When PORTn is in the POWER_GOOD state and the PD momentarily increases its current draw, setting this bit decreases the level at which the PORTn fold-backs the port voltage so the current can be supplied at a higher port voltage, thereby increasing the maximum power delivery to the PD. 0 = Normal Voltage Foldback for port in POWER_GOOD state 1 = Decrease level of Port Voltage Foldback
6	PORT3_PGOOD_FOLDBACK	
5	PORT2_PGOOD_FOLDBACK	
4	PORT1_PGOOD_FOLDBACK	
3	INRUSH_850MA	PORTn_INRUSH_850MA Defines the current limit during inrush. Setting this powers legacy high capacitance PDs. 0 = 425 mA Inrush Current Limit 1 = 850 mA Inrush Current Limit
2	INRUSH_850MA	
1	INRUSH_850MA	
0	INRUSH_850MA	

3.38 FLASH REGISTERS (0x5F – 0x63)

Refer to for information on the use of these registers.

4. Electrical Characteristics Si3473/72

Table 4.1. Recommended Operating Conditions[1]

Parameter	Symbol	Test Condition/Note	Min	Typ	Max	Unit
VPWR Input Supply Voltage	V_{PWR}	IEEE Type 3 when port is ON	50	—	57	V
		IEEE Type 4 when port is ON	52	—	57	V
VPWR Slew Rate	$V_{PWRSLEW}$		—	—	1	V/µs
VDD Supply Voltage	V_{DD}		3.0	3.3	3.6	V
Operating Ambient Temperature[2]	T_{AMB}		–40	—	85	°C
Thermal Impedance	θ_{JA}	4-Layer PCB, no airflow	—	24	—	°C/W
Junction Temperature	T_J		–40	—	125	°C

Note:

1. All specification voltages are referenced with respect to DGND. These specifications apply over the recommended operating voltage and temperature ranges of the device unless noted otherwise.
2. The Si3473/72 includes internal thermal shutdown above 125 °C.

Table 4.2. Electrical Specifications

These specifications apply over the recommended operating voltage and temperature ranges of the device specified in Table 4.1 Recommended Operating Conditions[1] on page 67 unless otherwise noted. Typical performance is for T_A = 25 °C, V_{DD} = AGND + 3.3 V, AGND and DGND = 0 V, and VPWR at 54 V. V_{PORTn}, V_{CLASS}, and V_{MARK} voltages are referenced with respect to V_{DRAIN}. All other voltages are referenced with respect to GND.

Parameter	Symbol	Test Condition/Note	Min	Typ	Max	Unit
Power Supply Voltages						
VPWR Under Voltage Lock Out	V_{PWR_UVLO}	Level below which chip is not operational	25	31	34	V
VPWR UVLO Input Voltage (to turn on)	V_{UVLO_ON}		25	28	—	V
VPWR UVLO Input Voltage (to turn off)	V_{UVLO_OFF}		—	31	34	V
VDD UVLO Warning Voltage	$V_{DD\_UVLO\_WARN}$	Digital interface still responds, but VDD_UVLO bit will be set as an indication of an imminent problem.	2.6	2.8	3.0	V
VDD UVLO Failure Voltage	$V_{DD\_UVLO\_FAIL}$	Level below which digital parts of the chip will not respond	2.1	2.25	2.4	V
Hardware Reset Voltage	V_{RESET}	V_{DD} voltage causing reset	—	1.8	—	V
Power Supply Currents[1]						
VPWR Supply Current	I_{VPWR}	During normal operation	—	2	5	mA
		V_{PWR} = 8 V, V_{DD} = 0 V	—	—	100	µA
VDD Supply Current	I_{DD}	During normal operation	—	17	25	mA
MOSFET Fault Specifications						

Parameter	Symbol	Test Condition/Note	Min	Typ	Max	Unit
MOSFET Fault Threshold	V_{PORT}	When FET is driven OFF, if either condition is met, a MOSFET fault is reported.	—	15	—	V
	I_{FET}		—	5.0	—	mA
Detection Specifications						
Detection Short Circuit Current	I_{DET_SC}	Measured when Vdrain is shorted to V_{PWR}	—	3.0	4.9	mA
Detection voltage when RDET = 25.5 kΩ	V_{PORTn}	Primary Detection voltage	2.8	4.0	—	V
		Secondary Detection voltage	—	8.0	10.0	V
Signature Resistance	R_{GOOD}		—	25	—	kΩ
Minimum Signature Resistance @ PD	R_{DET_MIN}		15	17	19	kΩ
Maximum Signature Resistance @ PD	R_{DET_MAX}		26.5	30	33	kΩ
Reject Signature Capacitance	C_{REJECT}		—	—	10	µF
Open Port Threshold	R_{OPEN_PORT}	Threshold between R_HIGH and R_OPEN	100	—	400	kΩ
Shorted Port Threshold	R_{SHORT}		150	—	400	Ω
High Detection Signature Resistance	R_{HIGH}		33	—	100	kΩ
Low Detection Signature Resistance	R_{LOW}		0.4	—	15	kΩ
Classification Specifications						
Class Event Voltage	V_{CLASS}	0 mA < I_{CLASS} < 51 mA	15.5	—	20.5	V
Classification Short Circuit Current	I_{CLASS_SC}	Measured when Vdrain is shorted to V_{PWR}	55	—	95	mA
Classification Current Region	I_{CLASS_REGION}	Class Signature 0	0	—	5	mA
		Threshold between Class Signature 0 or 1	5	—	8	mA
		Class Signature 1	8	—	13	mA
		Threshold between Class Signature 1 or 2	13	—	16	mA
		Class Signature 2	16	—	21	mA
		Threshold between Class Signature 2 or 3	21	—	25	mA
		Class Signature 3	25	—	31	mA
		Threshold between Class Signature 3 or 4	31	—	35	mA
		Class Signature 4	35	—	45	mA
		Threshold between Class Signature 4 or invalid class	45	—	51	mA
		Legacy Class Signature 5	51	—	60	mA
Classification Mark Specifications						
Mark Event Voltage	V_{MARK}	Mark current between 0 and 5 mA	7	—	10	V
Mark Event Current Limitation	I_{MARK_LIM}		5	—	100	mA
Output Voltage						

Parameter	Symbol	Test Condition/Note	Min	Typ	Max	Unit
Threshold Voltage for Power Good Sense	V_{PGOOD}	Measured at V_{DRAINn} to AGND	1	2	3	V
Bias Current of DRAINn Pin	I_{DRAINn}	V_{DRAINn} = 0 V	—	–25	—	µA
Current Limit Detection Threshold	V_{DRAIN_ILIM}	Measured at V_{DRAIN} with respect to AGND	—	—	3.00	V
Resistance from DRAIN to AGND	R_{DRAIN}		—	2.5	—	MΩ
Current Sense[2]						
Power Limit	P_{CUT}	Class 0, 2-pair power, 15.4 W nominal	—	17.8	—	W
		Class 1, 2-pair power, 4 W nominal	—	4.6	—	W
		Class 2, 2-pair power, 7 W nominal	—	8.05	—	W
		Class 3, 2-pair power, 15.4 W nominal	—	17.8	—	W
		Class 4, 2-pair power, 30 W nominal	—	34.5	—	W
		Legacy Class 5, 2-pair power, 45 W nominal	—	47.25	—	W
PCUT Tolerance	P_{CUT}	Policy settings < 15 W	0	5	10	%
		Policy settings ≥ 15 W	0	2.5	5	%
Current Limit	I_{LIM}	Inrush, all assigned PD classes, Vport > 30 V	400	425	450	mA
		Power-on, assigned PD Class 0, 1, 2, 3, 4+ Type 1 limited	—	425	—	mA
		Power-on, assigned PD Class 4, 5	—	1275	—	mA
Disconnect with power provided over two pairs[3]	$I_{PORT\_DIS\_2P}$	Current	—	6.5	—	mA
MOSFET Gate Drive[4]						
Drive Current from GATEn Pin (Active)		GATEn pin active V_{GATEn} = AGND	–70	–50	–20	µA
Drive Current from GATEn Pin (Off)		GATEn pin shut off V_{GATEn} = AGND+ 5 V	—	50	—	mA
Voltage Difference Between any GATEn and AGND Pin		I_{GATEn} = –1 µA	10	11.5	13	V

Note:

1. Positive values indicate currents flowing into the device. Negative currents indicate current flowing out of the device.
2. Current sense resistor, R_{SENSE}, is determined by part number to be either .255 or .200 Ω (see Top Marking section below).
3. An MPS signal is considered present on an alternative when the current on that alternative is above these thresholds.
4. See "AN1228: FET Selection Guide for Si347x PSE Families" for detailed information on FET selection.

Table 4.3. I²C Bus Timing Specifications[1, 2, 3, 4]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Serial Bus Clock Frequency	f_{SCL}	See Figure 4.1 I²C Bus Interface Timing on page 70.	0	—	800	kHz

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCL High Time	t_{SKH}	See Figure 4.1 I²C Bus Interface Timing on page 70.	300	—	—	ns
SCL Low Time	t_{SKL}	See Figure 4.1 I²C Bus Interface Timing on page 70.	650	—	—	ns
Bus Free Time	t_{BUF}	Between STOP and START conditions. See Figure 4.1 I²C Bus Interface Timing on page 70.	650	—	—	ns
Start Hold Time	t_{STH}	Between START and first low SCL. See Figure 4.1 I²C Bus Interface Timing on page 70.	300	—	—	ns
Repeated Start Setup Time	t_{STS}	Between SCL high and START condition. See Figure 4.1 I²C Bus Interface Timing on page 70.	300	—	—	ns
Stop Setup Time	t_{SPS}	Between SCL high and STOP condition. See Figure 4.1 I²C Bus Interface Timing on page 70.	300	—	—	ns
Data Hold Time	t_{DH}	See Figure 4.1 I²C Bus Interface Timing on page 70.	75	—	—	ns
Data Setup Time	t_{DS}	See Figure 4.1 I²C Bus Interface Timing on page 70.	100	—	—	ns
Time from Hardware or Software Reset until Start of I²C Traffic	t_{RESET}	Reset to start condition	5	—	—	ms

Note:

1. All specification voltages are referenced with respect to AGND and DGND at ground.
2. Not production tested (guaranteed by design).
3. All timing references measured at V_{IL} and V_{IH}.
4. SCL and SDA rise and fall times depend on bus pull-up resistance and bus capacitance.

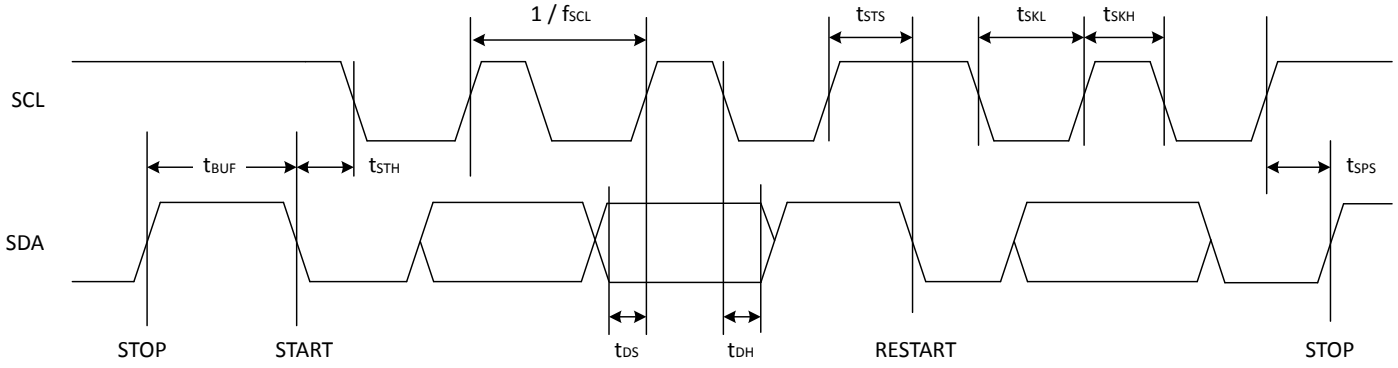


Figure 4.1. I²C Bus Interface Timing

Table 4.4. Digital Pin Recommended Operating Conditions[1]

Parameter	Symbol	Test Condition	Pins	Min	Typ	Max	Unit
Input Low Voltage	V_{IL}		A1-A4, SCL, SDA, RESETb, OSS	—	—	0.3 x VDD	V

Parameter	Symbol	Test Condition	Pins	Min	Typ	Max	Unit
Input High Voltage	V_{IH}		A1-A4, SCL, SDA, RESETb, OSS	0.7 x VDD	—	—	V
Output Low Voltage	V_{OL}	IOL = 13.5 mA, VDD > 3.0 IOL = 3.6 mA, 1.71 < VDD < 2.2 V	SDA, INTb			VDD x 0.2	V
Input Leakage	I_{LK}	VDD < Vpin < VDD + 2.5 V	A1-A4, SCL, SDA, RESETb, OSS	0	5	150	µA
Pullup Current to VDD	I_{PU}		RESET, OSS, INT, SCL, SDA, A1–A4	—	–20	—	µA
Pulse Width of spikes which must be suppressed by input filter	t_{SP}		SCL, SDA	0	—	10	ns

Note:

1. All specification voltages are referenced with respect to DGND. These specifications apply over the recommended operating voltage and temperature ranges of the device unless noted otherwise.
2. SDA and INTb are open drain outputs. Tie each pin to VDD with a 1 kΩ resistor for normal operation
3. Note that VIL and VIH are shown as fractions of VDD. This is intended to allow the I^2C interface to operate with CMOS voltage levels. These values will be higher than the standard TTL interface.

Table 4.5. Absolute Maximum Ratings[1]

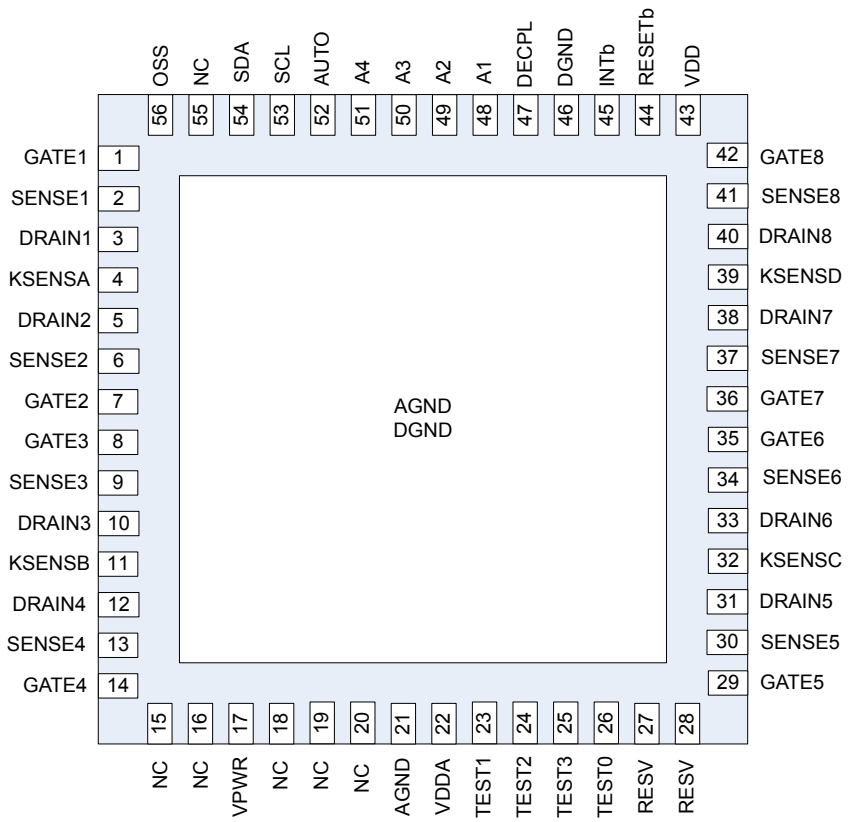
Parameter	Range	Unit
Supply Voltage		
VDD	–0.3 to 4.0	V
VPWR	–0.3 to 80.0	V
DGND with Respect to AGND	0	V
Digital Signals		
All	–0.3 to 3.6	V
Analog Signals		
GATEn with Respect to AGND	–0.3 to 20.0	V
SENSEn with Respect to AGND	–0.3 to 3.0	V
DRAINn with Respect to AGND	–3 to 80	V
Temperature		
Junction	+150	°C
Storage	–55 to +150	°C

Note:

1. Permanent device damage may occur if the maximum ratings are exceeded. Functional operation should be restricted to those conditions specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may adversely affect device reliability.

5. Pin Descriptions

5.1 Si3473 Pin Descriptions

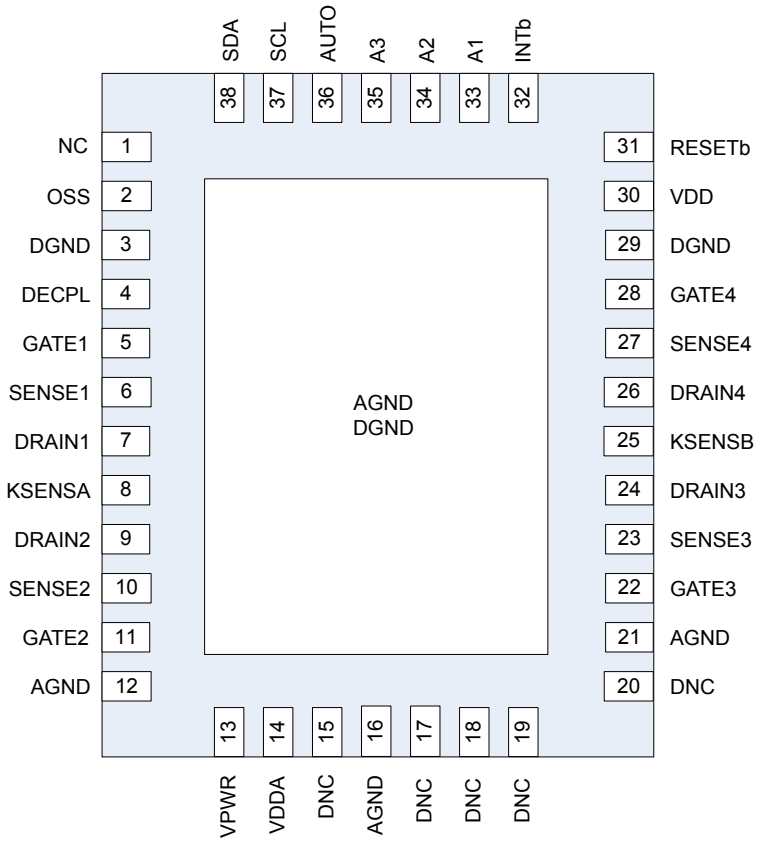


Pin #	Name	Type	Description
44	RESETb	Digital input with 20 µA pull-up to VDD	Active low device reset input. Generally, RESETb is used at initial power up. If RESETb is asserted (pulled to DGND), the MCU is disabled, all internal registers of the device are set to their default (power-up) state, and all output ports are shut off. Valid RESETb timing pulses must be >10 µs. If RESETb is not used, RESETb should either be tied directly to VDD or through a 10 kΩ resistor to VDD.
45	INTb	Digital output (open drain)	Interrupt output. This open drain output pin is asserted low (to DGND) if a fault condition occurs on any of the four ports. The state of INTb is updated for use by a host controller between valid I^2C commands. Refer to the “Interrupts” section of for more information. Tie INTb to VDD through a 10 kΩ resistor for normal operation.
53	SCL	Digital input	Serial clock input. This pin should be tied directly to the SCL (clock) connection on the I^2C bus.
54	SDA	I^2C input/output	Bidirectional I^2C input/output.
51, 50, 49, 48	A4, A3, A2, A1	Digital input with 20 µA pull-up to VDD	I^2C address input. Used to set the base I^2C address for the Si3473/72 in the following (binary) format: 010[A4][A3][A2][A1]b. The three MSB bits of the address are set to 010. Address values are latched after the deassertion of RESETB or when VDD ramps and VPWR exceeds the UVLO threshold voltage. Each address pin should be tied to either VDD or DGND.
46, ePAD	DGND	Digital ground	Ground connection for the 3.3 V digital supply (VDD). DGND and AGND are tied together inside the Si3473/72 package.

Pin #	Name	Type	Description
21, ePAD	AGND	Analog ground	Ground connection for the VPWR supply. DGND and AGND are tied together inside the Si3473/72 package
43	VDD	Digital power	3.3 V digital supply (relative to DGND). Bypass VDD with a 0.1 µF capacitor to DGND as close as possible to the Si3473/72 power supply pins; tied to VDDA.
22	VDDA	Analog power	3.3 V supply to the analog components; tied to VDD at the PCB level.
17	VPWR	Analog power	Positive PoE voltage (+44 to +56 V) relative to AGND.
41	SENSE8	Analog input	Current sense inputs for external MOSFETs. The SENSEn pin measures current through an external sense resistor tied between the AGND supply rail and the SENSEn input. If the I_{CUT} limit (the overcurrent limit) is exceeded, the current limit fault timer is incremented. If the voltage across the sense resistor subsequently triggers (the overcurrent limit), the voltage driven onto the GATEn pin is modulated to provide constant current through the external MOSFET. Tie the SENSEn pin to AGND when the port is not used. To accommodate 802.3at (PoE Plus) classification, both the I_{CUT} and Ilim values can be scaled. See 3.3 POWER Event and POWER Event CoR (Address 0x02, 0x03) for more information.
37	SENSE7		
34	SENSE6		
30	SENSE5		
13	SENSE4		
9	SENSE3		
6	SENSE2		
2	SENSE1		
42	GATE8	Analog output	Gate drive outputs to external MOSFETs. Connect the GATEn outputs to the external MOSFET's gate node. A 50 µA pull-up current source is used to turn on the external MOSFET. When a current limit is detected, the GATEn voltage is reduced to maintain constant current through the external MOSFET. If the fault timer limit is reached, GATEn pulls down, shutting off the external MOSFET. GATEn will clamp to 11.5 V (typical) above AGND. If the port is unused, leave the GATEn pin disconnected or tie to AGND.
36	GATE7		
35	GATE6		
29	GATE5		
14	GATE4		
8	GATE3		
7	GATE2		
1	GATE1		
40	DRAIN8	Analog input with 25 µA pull-up to VPWR	MOSFET drain output voltage sense. The Power Good bit is set on each port when the voltage between DRAINn and AGND drops below 2 V (typical). See 3.3 POWER Event and POWER Event CoR (Address 0x02, 0x03) for further information. DRAINn pins should be left floating if the port is unused.
38	DRAIN7		
33	DRAIN6		
31	DRAIN5		
12	DRAIN4		
10	DRAIN3		
5	DRAIN2		
3	DRAIN1		
56	OSS	Over supply signal	A positive going edge on this pin shuts down ports that have been identified as low priority by setting Register 0x15. This pin has a 20 µA pull-up.
4	KSENSA	Input	Kelvin points for accurate measurement of voltage across the sense resistor for ports 1 and 2.
11	KSENSB	Input	Kelvin points for accurate measurement of voltage across the sense resistor for ports 3 and 4.
32	KSENSC	Input	Kelvin points for accurate measurement of voltage across the sense resistor for ports 5 and 6.
39	KSENSD	Input	Kelvin points for accurate measurement of voltage across the sense resistor for ports 7 and 8.

Pin #	Name	Type	Description
26	TEST4	Input/Output	Test pin for internal use by Skyworks only. Leave floating.
25	TEST3		
24	TEST2		
23	TEST1		
47	DECPL	Decoupling	Place a 0.1 µF capacitor between DECPL and GND.
52	AUTO-MODE	Automode	Enables Automode. Refer to 2.10.1 AUTO Pin Autonomous Mode.
28, 27	RESV	Reserved	Reserved for future use. Leave floating.
19, 18, 16, 15, 55, 20	NC	No Connect	No connections or nets allowed. Leave floating.

5.2 Si3472 Pin Descriptions



Pin #	Name	Type	Description
ePAD	AGND DGND	Analog ground Digital ground	Ground connection for the 3.3 V digital supply (VDD). DGND and AGND are tied together inside the Si3472 package.
21, 16, 12	AGND	Analog ground	DGND and AGND are tied together inside the Si3472 package
27	SENSE4	Analog input	Current sense inputs for external MOSFETs. The SENSEn pin measures current through an external sense resistor tied between the AGND supply rail and the SENSEn input. If the I_{CUT} limit (the overcurrent limit) is exceeded, the current limit fault timer is incremented. If the voltage across the sense resistor subsequently triggers (the overcurrent limit), the voltage driven onto the GATEn pin is modulated to provide constant current through the external MOSFET. Tie the SENSEn pin to AGND when the port is not used. To accommodate 802.3at (PoE Plus) classification, both the I_{CUT} and Ilim values can be scaled. See 3.23 PORT_REMAP (0x26) for more information.
23	SENSE3		
10	SENSE2		
6	SENSE1		
28	GATE4	Analog output	Gate drive outputs to external MOSFETs. Connect the GATEn outputs to the external MOSFET's gate node. A 50 µA pull-up current source is used to turn on the external MOSFET. When a current limit is detected, the GATEn voltage is reduced to maintain constant current through the external MOSFET. If the fault timer limit is reached, GATEn pulls down, shutting off the external MOSFET. GATEn will clamp to 11.5 V (typical) above AGND. If the port is unused, leave the GATEn pin disconnected or tie to AGND.
22	GATE3		
11	GATE2		
5	GATE1		
26	DRAIN4	Analog input with 25 µA pull-up to VPWR	MOSFET drain output voltage sense. The Power Good bit is set on each port when the voltage between DRAINn and AGND drops below 2 V (typical). See 3.3 POWER Event and POWER Event CoR (Address 0x02, 0x03) for further information. DRAINn pins should be left floating if the port is unused.
24	DRAIN3		
9	DRAIN2		
7	DRAIN1		

Pin #	Name	Type	Description
38	SDA	I^2C input/output	Bidirectional I^2C input/output.
37	SCL	Digital input	Serial clock input. This pin should be tied directly to the SCL (clock) connection on the I2C bus.
35, 34, 33	A1, A2, A3	Digital input with 20 µA pull-up to VDD	I2C address input. Used to set the base I2C address for the Si3472 in the following (binary) format: 0100[A3][A2][A1]b. The three MSB bits of the address are set to 010. Address values are latched after the deassertion of RESETB or when VDD ramps and VPWR exceeds the UVLO threshold voltage. Each address pin should be tied to either VDD or DGND.
29,3	DGND	Digital ground	Ground connection for the 3.3 V digital supply (VDD). DGND and AGND are tied together inside the Si3472 package.
13	VPWR	Analog power	Positive PoE voltage (+44 to +56 V) relative to AGND.
14	VDDA	Analog power	3.3 V supply to the analog components; tied to VDD at the PCB level.
30	VDD	Digital Power	3.3 V supply to the digital side; tied to VDDA at the PCB level.
25	KSENSB	Input	Kelvin points for accurate measurement of voltage across the sense resistor for ports 3 and 4.
8	KSENSA	Input	Kelvin points for accurate measurement of voltage across the sense resistor for ports 1 and 2.
2	OSS	Over supply signal	A positive going edge on this pin shuts down ports that have been identified as low priority by setting Register 0x15. This pin has a 20 µA pull-up.
36	AUTO	Automode	Enables Automode.
31	RESETb	Digital input with 20 µA pull-up to VDD	Active low device reset input. Generally, RESETb is used at initial power up. If RESETb is asserted (pulled to DGND), the MCU is disabled, all internal registers of the device are set to their default (power-up) state, and all output ports are shut off. Valid RESETb timing pulses must be >10 µs. If RESETb is not used, RESETb should either be tied directly to VDD or through a 10 kΩ resistor to VDD.
4	DECPL	Decoupling	Place a 0.1 µF capacitor between DECPL and GND.
32	INTb	Digital output (open drain)	Interrupt output. This open drain output pin is asserted low (to DGND) if a fault condition occurs on any of the four ports. The state of INTb is updated for use by a host controller between valid I^2C commands. Refer to the “Interrupts” section of for more information. Tie INTb to VDD through a 10 kΩ resistor for normal operation.
19, 18, 17, 15, 20	DNC	No Connect	No connections or nets allowed. Leave floating.
1	NC	No Connect	No Connection. It is permitted to connect this pin to the neighboring pin SDA.

6. Package Outline

6.1 Package Outline: 56-Pin QFN

The figure below illustrates the package details for the Si3473. The table lists the values for the dimensions shown in the illustration. The Si3473 is packaged in an industry-standard, RoHS-compliant, 56-pin QFN package.

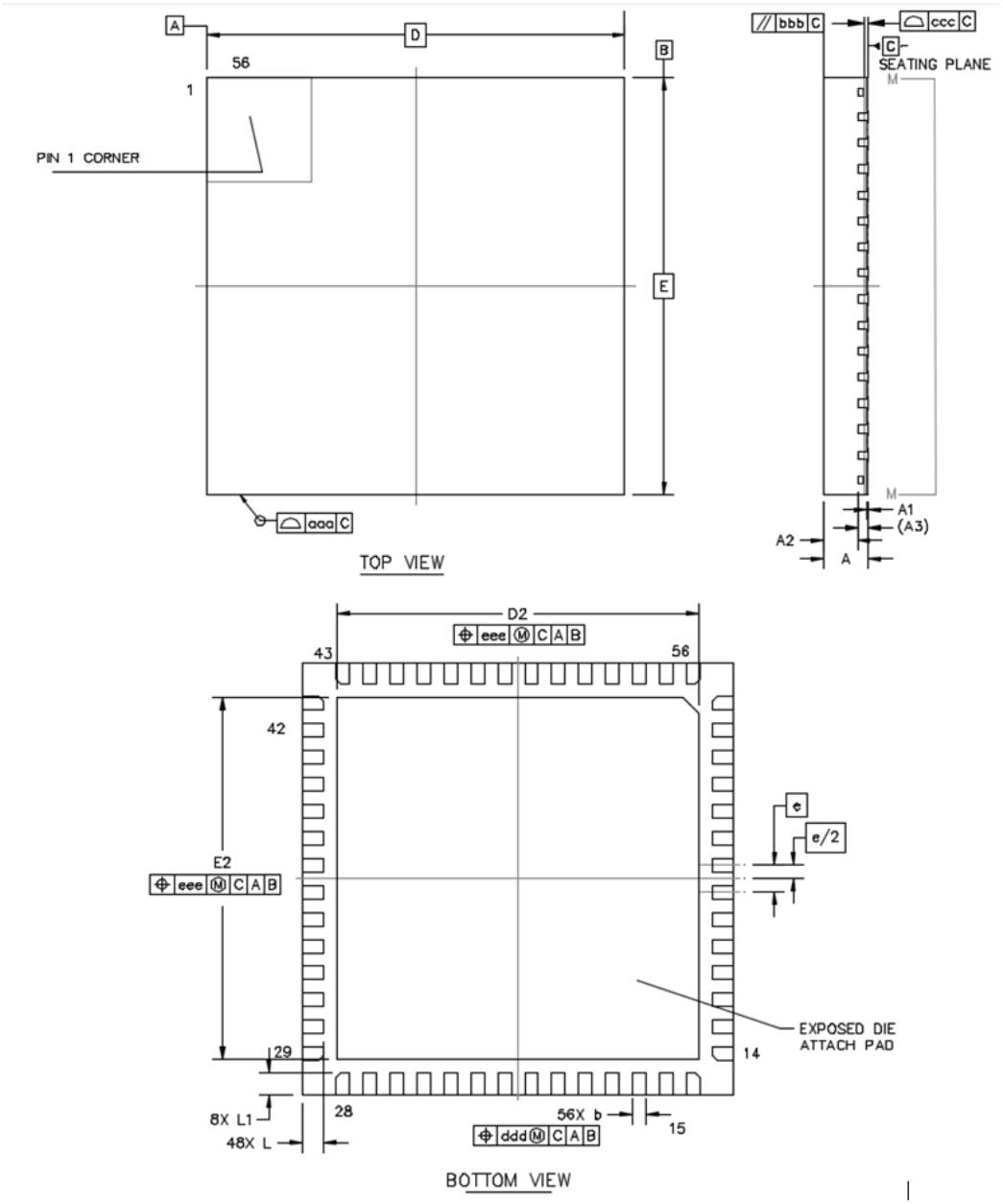


Figure 6.1. 56-Pin QFN Package

Table 6.1. Package Diagram Dimensions

Dimension	Min	Nom	Max
A	0.80	0.85	0.90
A1	0.00	0.035	0.05
A3		0.203 REF	
b	0.20	0.25	0.30
D	7.90	8.00	8.10
E	7.90	8.00	8.10
D2	6.60	6.70	6.80
E2	6.60	6.70	6.80
e		0.50 BSC	
L	0.35	0.40	0.45
L1	0.30	0.40	0.45
aaa		0.10	
bbb		0.10	
ccc		0.08	
ddd		0.10	
eee		0.10	

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220, Variation VLLD-5.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

6.2 Package Outline: 38-Pin QFN

The figure below illustrates the package details for the Si3472. The table lists the values for the dimensions shown in the illustration. The Si3472 is packaged in an industry-standard, RoHS-compliant, 38-pin QFN package. The lead plating material is matte tin.

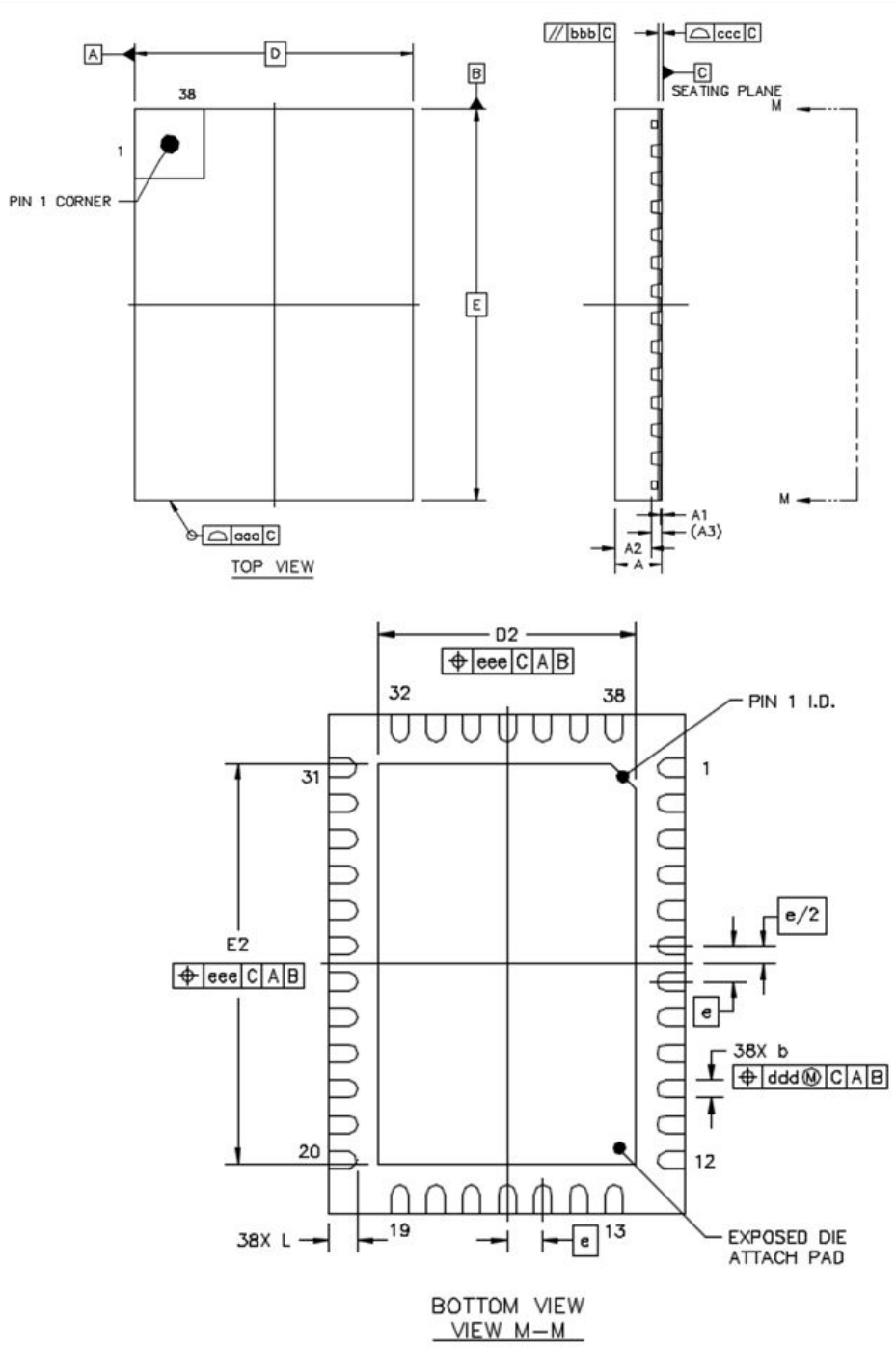


Figure 6.2. 38-Pin QFN Package

Table 6.2. Package Diagram Dimensions

Dimension	Min	Nom	Max
A	0.80	0.85	0.90
A1	0.00	0.035	0.05
A3		0.203 REF	
b	0.20	0.25	0.30
D	4.90	5.00	5.10
E	6.90	7.00	7.10
D2	3.50	3.60	3.70
E2	5.50	5.60	5.70
e		0.50 BSC	
L	0.35	0.40	0.45
aaa		0.10	
bbb		0.10	
ccc		0.08	
ddd		0.10	
eee		0.10	

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220, Variation VLLD-5.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

7. Land Pattern

7.1 Si3473 Land Pattern

The following figure illustrates the land pattern details for the Si3473. The table lists the values for the dimensions shown in the illustration. The stencil design and notes are shared as recommendations only. A customer or user may find it necessary to use different parameters and fine-tune their SMT process as required for their application and tooling.

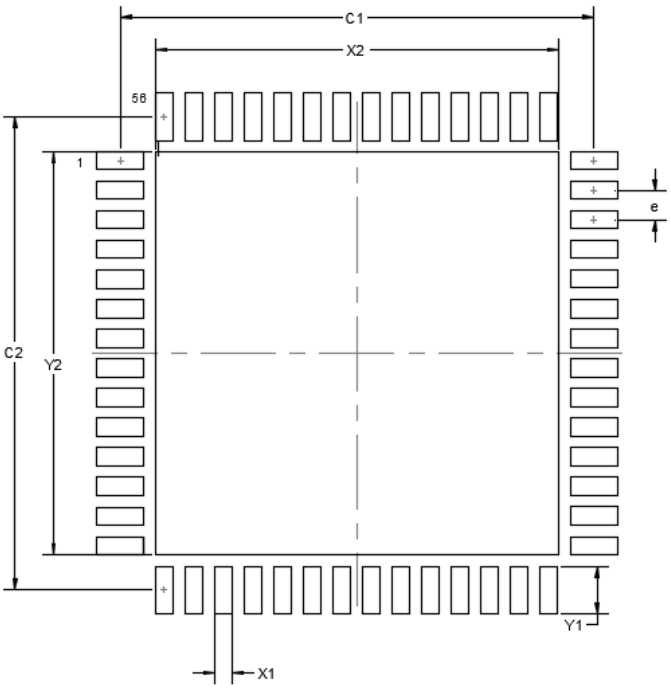


Figure 7.1. Si3473 Recommended Land Pattern

Table 7.1. PCB Land Pattern Dimensions

Symbol	mm
C1	8.00
C2	8.00
e	0.50
X1	0.30
Y1	0.80
X2	6.80
Y2	6.80

Notes:

General

1. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.
2. This Land Pattern Design is based on the IPC-7351 guidelines.

Solder Mask Design

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pins.
4. A 3 x 3 array of 1.50 mm square openings on a 2.1 mm pitch should be used for the center ground pad.

Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

7.2 Si3472 Land Pattern

The following figure illustrates the land pattern details for the Si3472. The table lists the values for the dimensions shown in the illustration. The stencil design and notes are shared as recommendations only. A customer or user may find it necessary to use different parameters and fine tune their SMT process as required for their application and tooling.

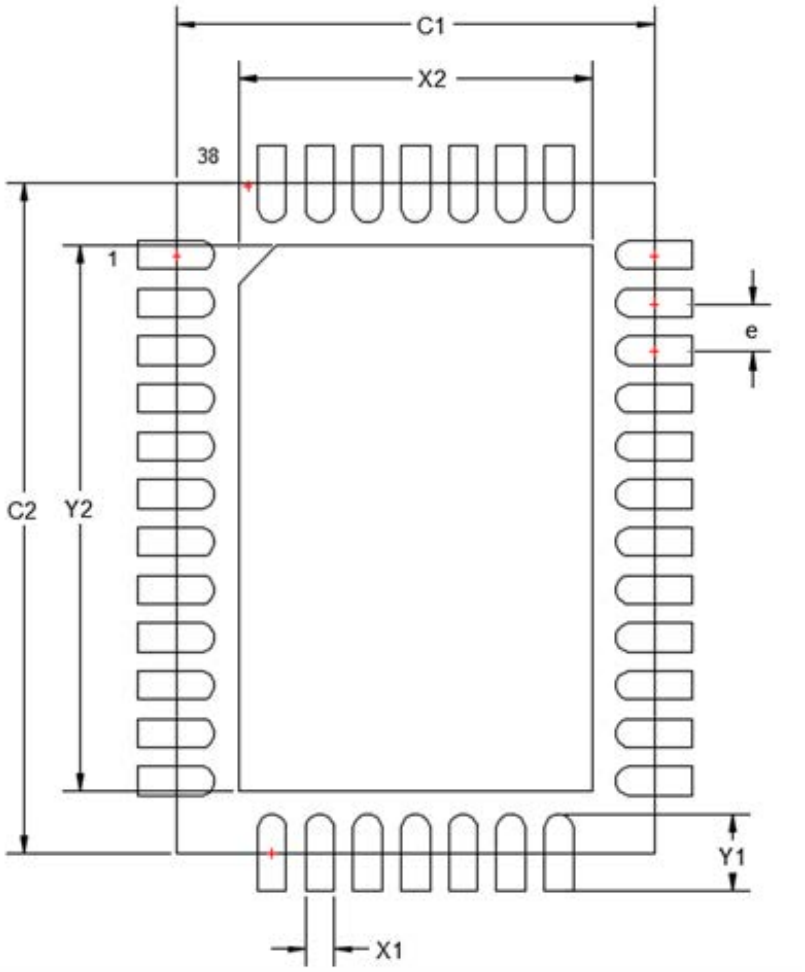


Figure 7.2. Si3472 Recommended Land Pattern

Table 7.2. PCB Land Pattern Dimensions

Symbol	mm
C1	5.00
C2	7.00
e	0.50
X1	0.30
Y1	0.80
X2	3.70
Y2	5.70

Symbol	mm

Notes:

General

1. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.
2. This Land Pattern Design is based on the IPC-7351 guidelines.

Solder Mask Design

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pins.
4. A 3x5 array of 0.90 mm square openings on 1.10 mm pitch should be used for the center ground pad.

Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

Note: Above notes and stencil design are shared as recommendations only. A customer or user may find it necessary to use different parameters and fine tune their SMT process as required for their application and tooling.

8. Top Marking

8.1 Si3473 Top Marking

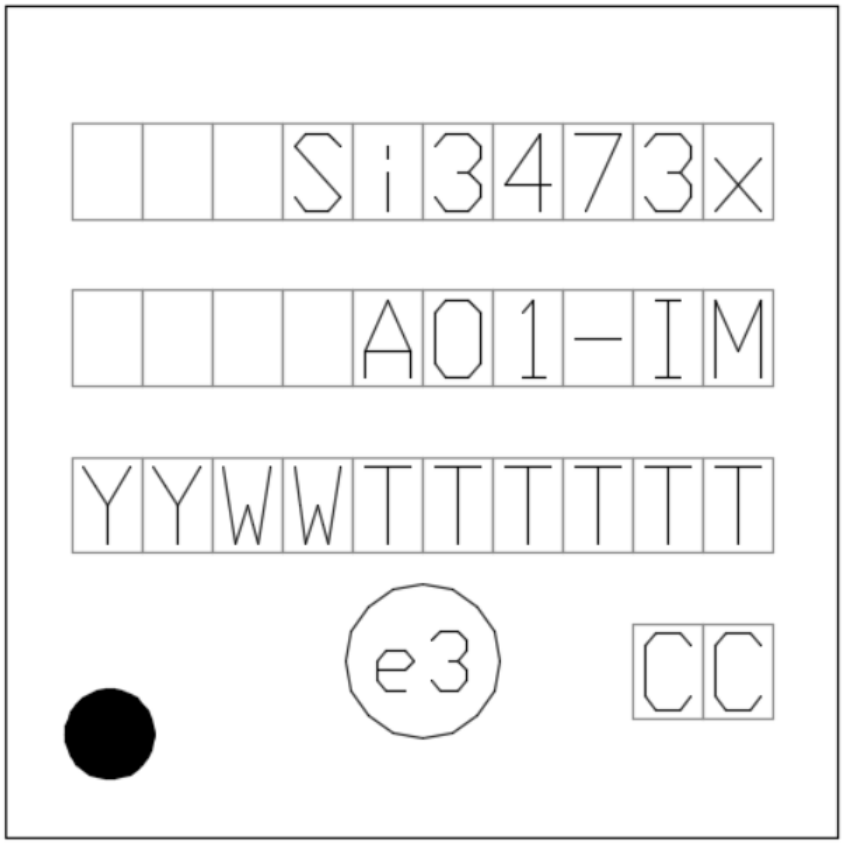


Figure 8.1. Si3473 Top Marking (QFN)

Table 8.1. Top Marking Explanation

Mark Method:	Laser	
Pin 1 Mark:	Bottom-Left-Justified	
Line 1 Mark Format:	Device Part Number	Si3473x x = A (255 mΩ sense resistor) x = B (200 mΩ sense resistor)
Line 2 Mark Format:	Device Revision Package Type	A01 IM
Line 3 Mark Format:	YY = Year WW = Work Week TTTTTT = Mfg Code	Year and Work Week of Assembly Manufacturing Code
Line 4 Mark Format:	Circle = 1.3 mm Diameter Country of Origin	“e3” Pb-Free Symbol TW = Taiwan

8.2 Si3472 Top Marking

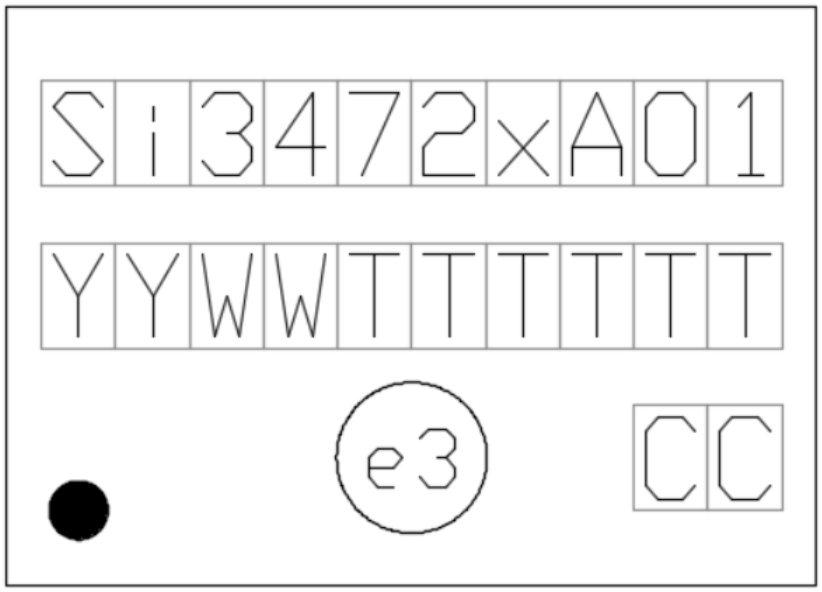


Figure 8.2. Si3472 Top Marking (QFN)

Table 8.2. Top Marking Explanation

Mark Method:	Laser	
Pin 1 Mark:	Bottom-Left-Justified	
Line 1 Mark Format:	Device Part Number	Si3472xA01 x = A (255 mΩ sense resistor) x = B (200 mΩ sense resistor)
Line 2 Mark Format:	YY = Year WW = Work Week TTTTTT = Mfg Code	Year and Work Week of Assembly Manufacturing Code
Line 3 Mark Format:	Circle = 1.3 mm Diameter Country of Origin	“e3” Pb-Free Symbol TW = Taiwan

9. Revision History

Revision 1.0

December, 2021

- Initial release.

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