



**SKYWORKS®**

## PRELIMINARY DATA SHEET

# Si82Ex Isolated Gate Driver with 6 A Drive, Dual Channels, and Low Channel-to-Channel Skew

The Si82Ex combines two isolated gate drivers into a single package for high-power applications. The Si82Ex includes devices with single or dual control inputs with independent or high-side/low-side outputs.

These drivers can operate with a 3–20 V input supply and a maximum gate driver supply voltage of 30 V.

The inputs are CMOS, which provides robust noise margin.

The Si82Ex is ideal for driving power silicon MOSFETs, IGBTs, SiC FETs, and GaN FETs used in various switched power and motor control applications. These drivers utilize Skyworks' proprietary silicon isolation technology, supporting up to 6 kV<sub>RMS</sub> for one minute isolation voltage. This technology enables high CMTI (200 kV/μs), lower propagation delays and skew, little variation with temperature and age, and tight part-to-part matching. The Si82Ex family offers longer service life and higher reliability than opto-coupled gate drivers.

The output stage operates as a voltage source with robust current output across operating conditions. The output stage features voltage mode drive technology using a familiar current-limiting resistor, allowing power designers to optimize for switching speed, emissions control, and overshoot limitation. The driver family also offers features, such as Undervoltage Lockout (UVLO), dead time programmability, and defined output states in all operating conditions.

Automotive grade is available. These products are built using automotive-specific flows at all steps in the manufacturing process to ensure the robustness and low defectivity required for automotive applications.

## Applications

- Isolated switched-mode supplies
- Motor drives
- Power inverters
- Uninterruptable power supplies
- Onboard chargers
- DC-DC converters

## Safety Regulator Approvals (Pending)

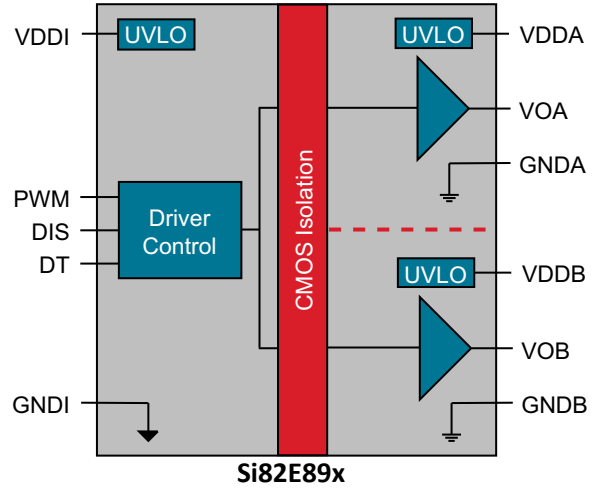
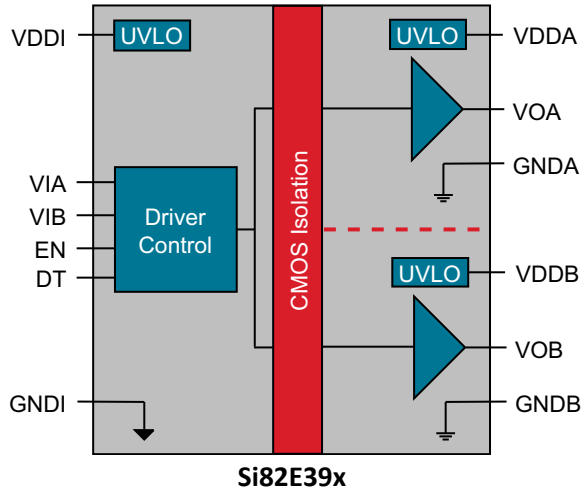
- UL 1577 recognized
  - Up to 6000 V<sub>RMS</sub> for one minute
- CSA certification conformity
  - 62368-1 (reinforced insulation)
  - 60601-1 (2 MOPP)
- VDE certification conformity
  - 60747-17 (reinforced insulation)
- CQC certification approval
  - GB4943.1

## Key Features

- Wide input range of 3–20 V
- Wide gate supply voltage of 5–30 V
- CMOS input with an optional deglitch filter
- Channel-to-channel skew < 5 ns
- Dead time control and overlap protection
- Universal and High-Side/Low-Side pinouts
- Voltage Mode Drive
- Unipolar or bipolar output voltages
- CMTI > 200 kV/μs
- 1500 V<sub>RMS</sub> working voltage
- Optimized UVLOs of 4, 8, 12, and 15 V
- 4 kV HBM ESD rating
- No unknown output states
- Increased channel-to-channel creepage
- 6 kV<sub>RMS</sub> safety rated isolation
- 10 kV bipolar surge
- Wide temperature range: –40 to 125 °C
- Narrow-body, 16-pin SOIC and wide-body, 14-pin SOIC packages
- AEC-Q100 qualification
- Automotive-grade OPNs available



Skyworks Green™ products are compliant with all applicable legislation and are halogen-free. For additional information, refer to *Skyworks Definition of Green™*, document number SQ04–0074.



# 1. Pin Descriptions

## 1.1. Device Pinouts

The Si82Ex consists of multiple die in a package with different bond-outs for different customer needs. Each bond-out corresponds to a pin-out below. See “10. Ordering Guide” on page 46 for the part numbers and features of these products.

### 1.1.1. NB SOIC-16 Pinouts

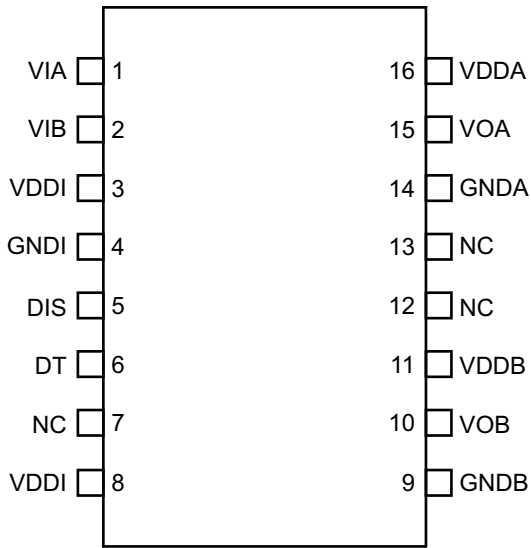


Figure 1. Si82E29x Pinout

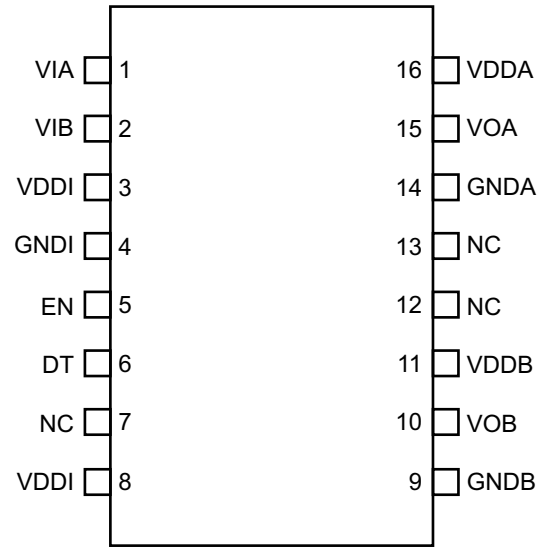


Figure 2. Si82E39x Pinout

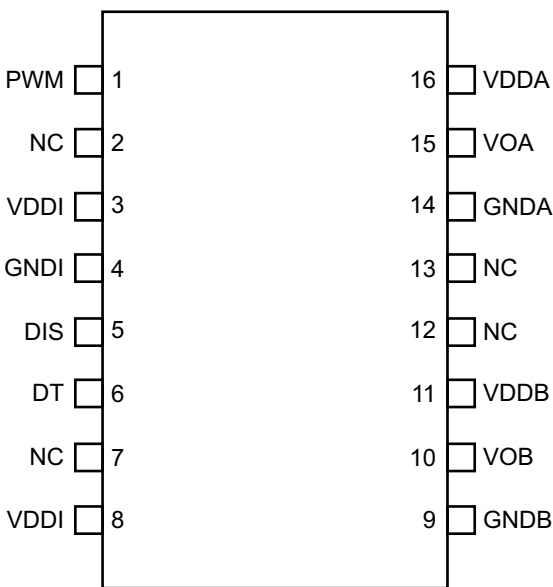


Figure 3. Si82E89x Pinout

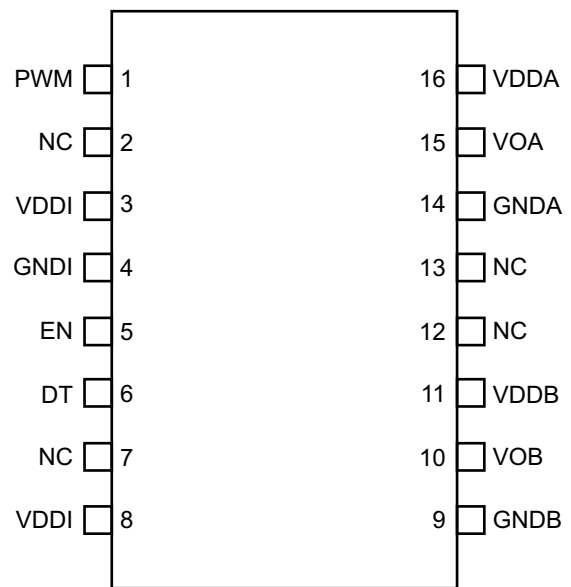


Figure 4. Si82E99x Pinout

1.1.2. WB SOIC-14 Pinouts

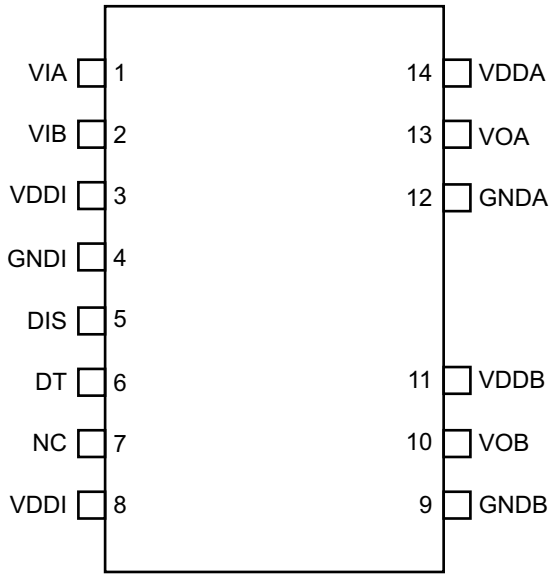


Figure 5. Si82E29x Pinout

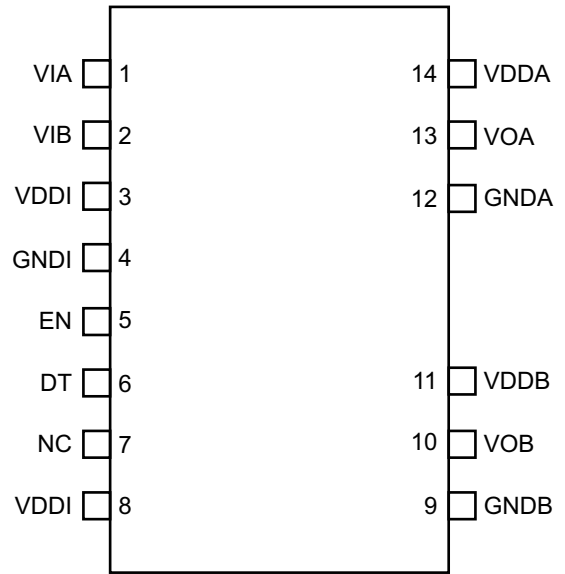


Figure 6. Si82E39x Pinout

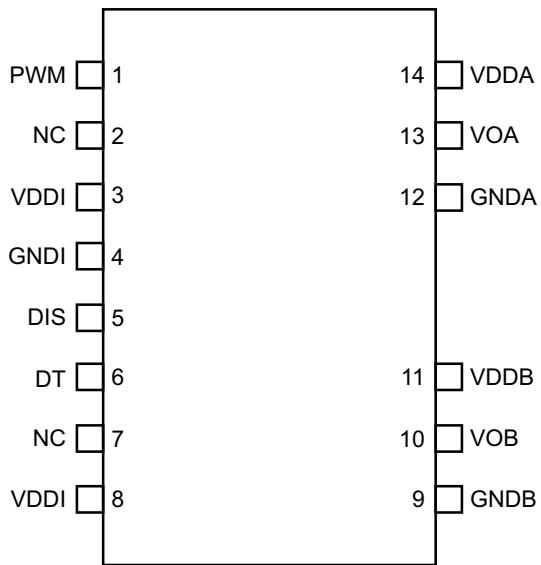


Figure 7. Si82E89x Pinout

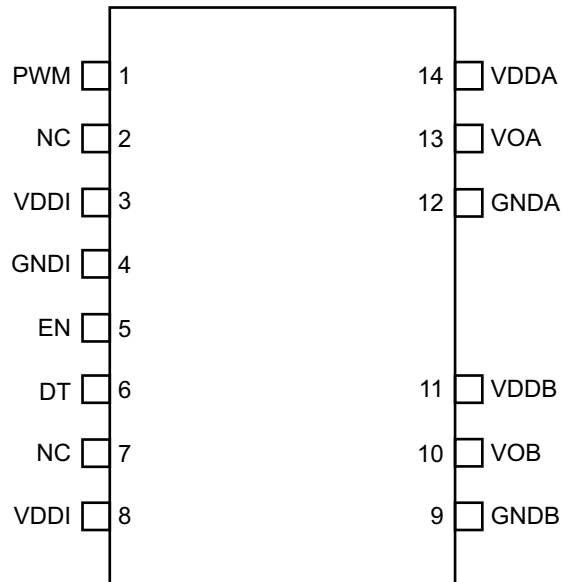


Figure 8. Si82E99x Pinout

## 1.2. Pin Details

Table 1. Si82Ex Pin Details

Pin Name	Pin Description
VDDI	Logic input power supply.
GNDI	Logic input ground terminal.
PWM	PWM logic input for gate driver A and gate driver B.
VIA	Non-inverting logic input terminal for gate driver A.
VIB	Non-inverting logic input terminal for gate driver B.
EN	Active high device ENABLE signal. When asserted (logic high), the device is enabled to perform in normal operating mode. When deasserted (logic low), this input unconditionally drives the output VOA and VOB logic low.
DIS	Active high device DISABLE signal. When asserted (logic high), this input unconditionally drives the output VOA and VOB logic low. When deasserted (logic low), the device is enabled to perform in normal operating mode.
DT	Dead time programming input. The value of the resistor connected from DT to GNDI sets the dead time between output transitions of VOA and VOB. Connecting DT to VDDI will disable dead time insertion on High-Side/Low-Side drivers. Connecting DT to VDDI will disable dead time insertion and overlap protection on Universal drivers.
VDDA	Gate driver A power supply.
GNDA	Gate driver A ground terminal.
VDDB	Gate driver B power supply.
GNDB	Gate driver B ground terminal.
VOA	Gate driver A output.
VOB	Gate driver B output.
NC	No connection. The user should not connect anything to this pin.

## 2. Device Overview

The Si82Ex is an isolated two-channel gate driver available in a Universal or High-Side/Low-Side configuration. Each configuration can be purchased with either an asynchronous enable or disable input. Additional features such as undervoltage lockout (UVLO) level and deglitch filter time can be configured through device selection. Refer to [“10. Ordering Guide” on page 46](#) for more details. Safety-rated isolation is provided from logic input to gate driver output by a pair of high-voltage silicon dioxide (SO<sub>2</sub>) capacitors. These capacitors are duplicated to form a differential path for signals modulated with an RF carrier and using an on-off keying (OOK) modulation scheme. This approach optimizes for fault tolerance and timing performance between input and output.

The digital logic inputs are high-voltage capable, CMOS-compatible, Schmitt triggered, and deglitched for high noise immunity and a wide range of compatibility. See [“4.4. Logic Input Signals” on page 12](#) for more details. Devices with a dead time input will operate as a High-Side/Low-Side driver for half-bridge circuits, inserting dead time between the two output channels and preventing shoot-through current. Additionally, for devices with a universal configuration, the dead time input can be connected to the VDDI supply to disable dead time insertion and overlap protection, enabling the device to operate as a dual driver. See [“4.5. Dead Time Control and Overlap Protection” on page 13](#) for more information. The gate driver outputs operate as a voltage source. Output current is adjusted through the selection of gate resistors. See [“5.1. Recommended Application Circuits” on page 17](#) for details.

### 3. Functional Block Diagrams

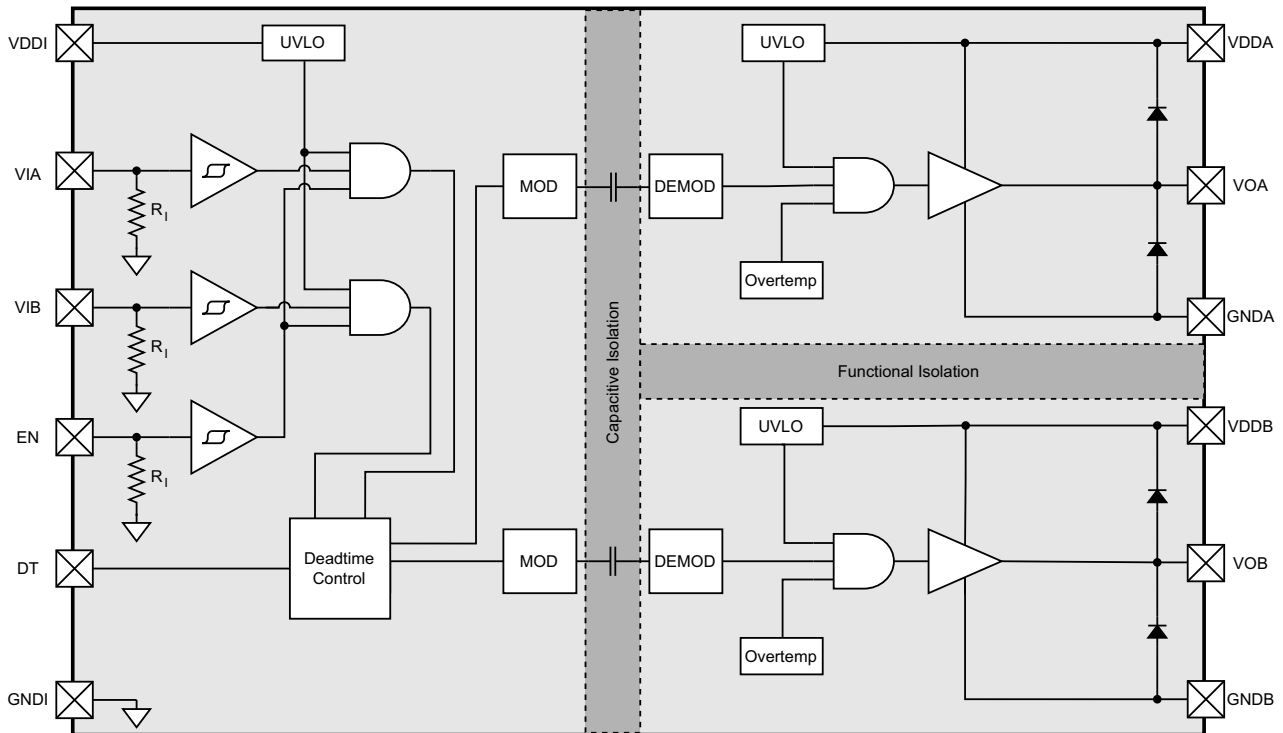


Figure 9. Si82E39x Device with Universal Configuration and Enable Input

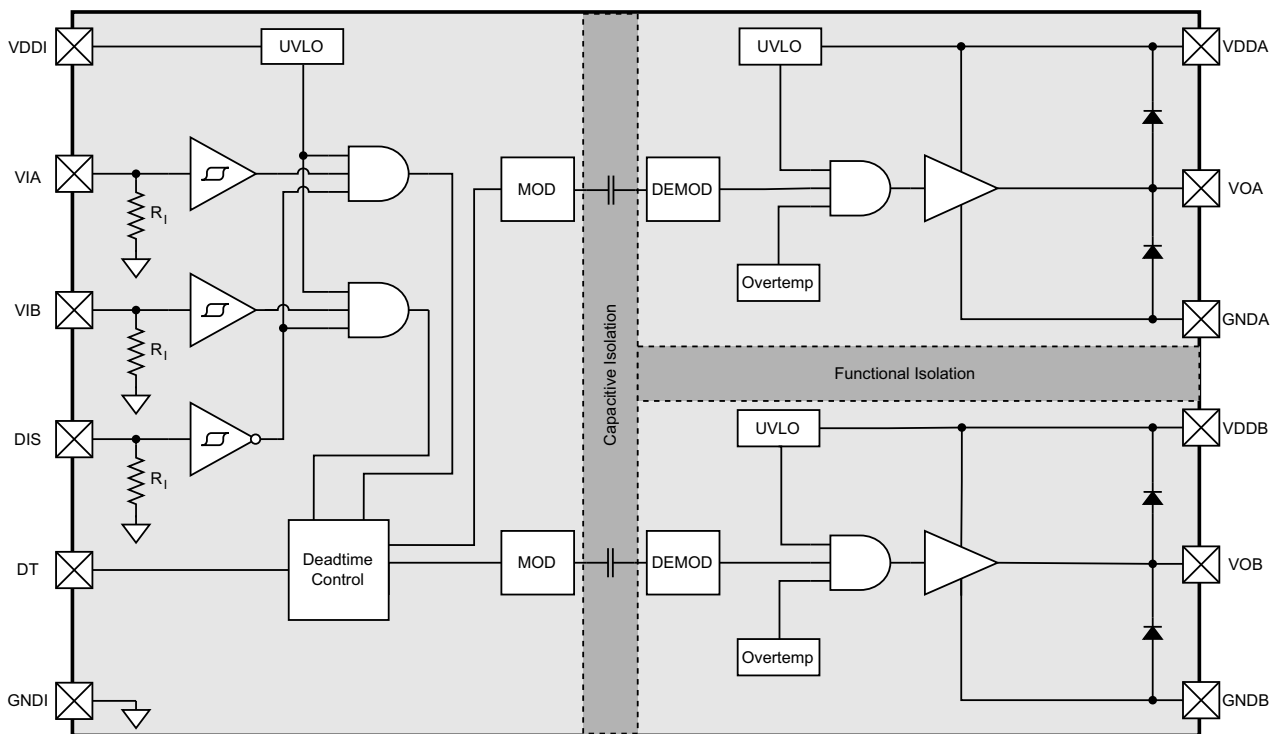


Figure 10. Si82E29x Device with Universal Configuration and Disable Input

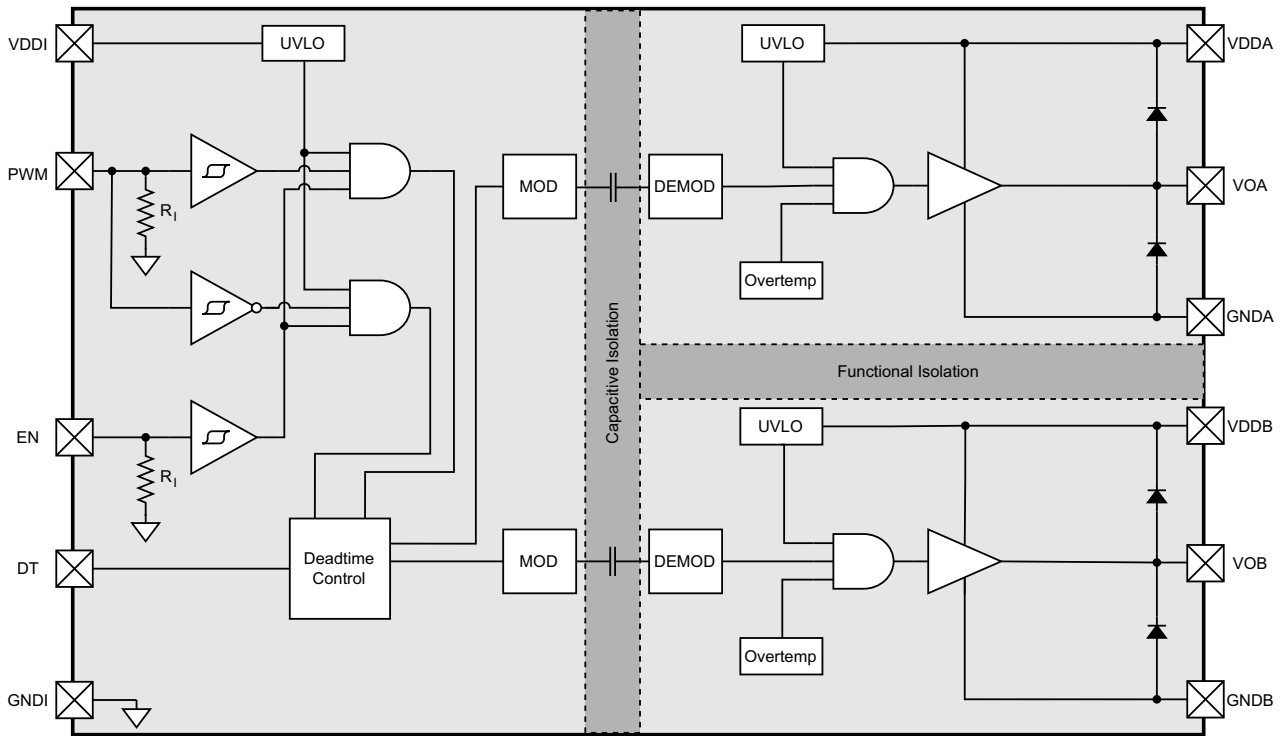


Figure 11. Si82E99x Device with High-Side/Low-Side Configuration and Enable Input

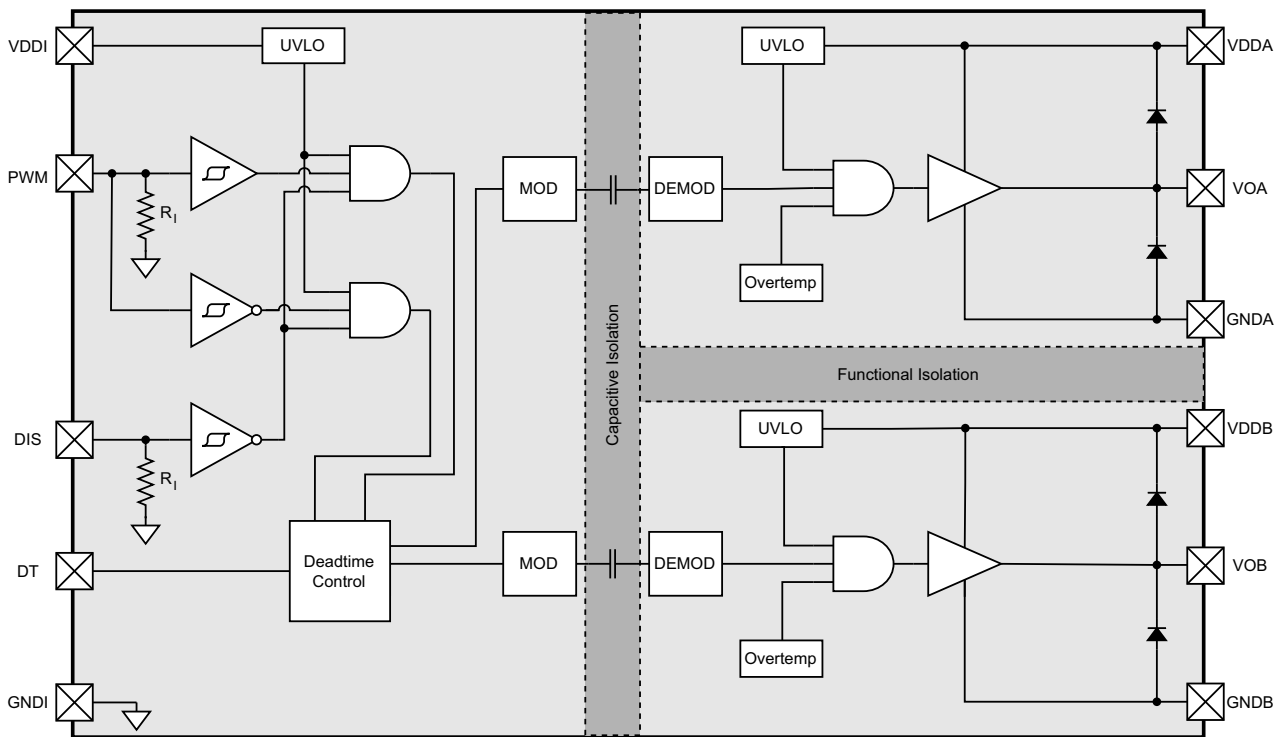


Figure 12. Si82E89x Device with High-Side/Low-Side Configuration and Disable Input



## 4. Device Operation

This section describes the capabilities of the device and how it should be used to achieve different goals within a design. Refer to “5.1. Recommended Application Circuits” on page 17 and “10. Ordering Guide” on page 46 for information on how to best utilize each device for different applications.

### 4.1. Truth Tables

The following tables describe the logical behavior of the Si82Ex Isolated Gate Driver devices.

**Table 2. Si82E2x-3x Truth Table**

Inputs <sup>1</sup>			Power Supply State <sup>2</sup>			Outputs <sup>3</sup>	
VIA	VIB	DIS/EN	VDDI <sup>4</sup>	VDDA <sup>5</sup>	Vddb <sup>5</sup>	VOA	VOB
H	L	E	P	P	—	H	L
L	H	E	P	—	P	L	H
H	H	E	P	P	P	H/L <sup>6</sup>	H/L <sup>6</sup>
L	L	X	—	—	—	L	L
X	X	D	—	—	—	L	L
X	X	X	NP	—	—	L	L
L	X	X	P	—	NP	L	L
H	H	E	P	P	NP	H <sup>6</sup>	L
X	L	X	P	NP	—	L	L
H	H	E	P	NP	P	L	H/L <sup>6</sup>

1. “X” is any logic value, “H” is a logic high (true) value, and “L” is a logic low (false) value. “E” indicates the driver is enabled (DIS = L or EN = H), “D” indicates the driver is disabled (DIS = H or EN = L). Input pins should always be connected to either logic high or low. Logic values listed in this table are assumed to transition at the same time as the power supply state.
2. “NP” is the “not powered” state, “P” is the “powered” state, and “—” is an irrelevant state.
3. “H” is a logic high (true) value, and “L” is a logic low (false). The logic low (L) value is enforced by the Shutdown Clamp if the same side gate driver’s power supply (VDDA/B) is not powered (NP).
4. “Not powered” (NP) state is defined as  $VDDI < VDDI_{UV}$ . “Powered” (P) state is defined as  $VDDI > VDDI_{UV}$ .
5. “Not powered” (NP) state is defined as  $VDDA/B < VDDA/B_{UV}$ . “Powered” (P) state is defined as  $VDDA/B > VDDA/B_{UV}$ .
6. The output state depends on the dead time pin (DT). If the dead time pin is connected to VDDI, the output will be a logic high (H). If the dead time pin is not connected to VDDI, the output will be a logic low (L). See “4.5. Dead Time Control and Overlap Protection” on page 13 for more information.

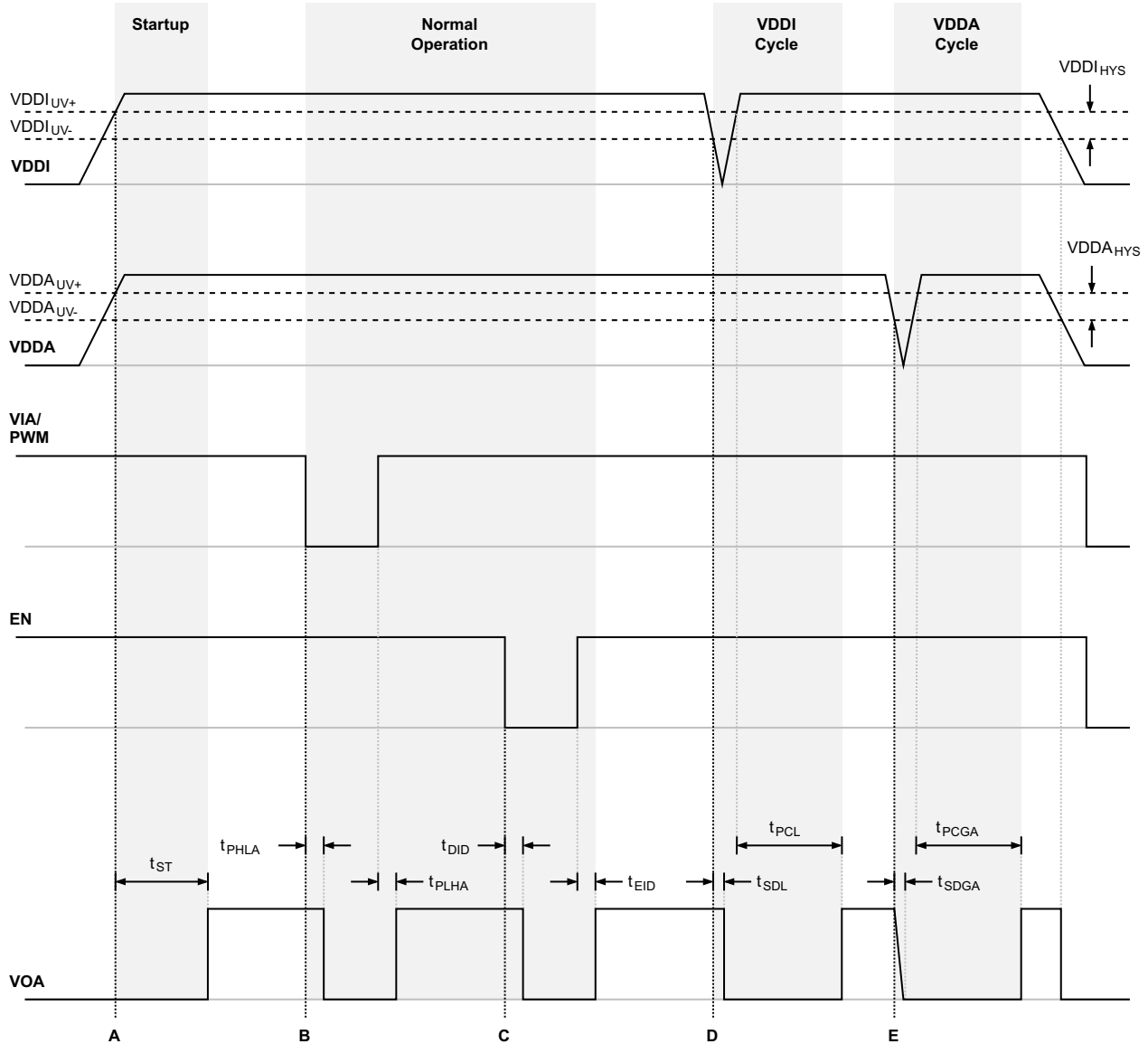
Table 3. Si82E8x-9x Truth Table

Inputs <sup>1</sup>		Power Supply State <sup>2</sup>			Outputs <sup>3</sup>	
PWM	DIS/EN	VDDI <sup>4</sup>	VDDA <sup>5</sup>	VDDB <sup>5</sup>	VOA	VOB
H	E	P	P	—	H	L
L	E	P	—	P	L	H
X	D	P	—	—	L	L
X	X	NP	—	—	L	L
H	E	P	P	NP	H	L
L	E	P	—	NP	L	L
H	E	P	NP	—	L	L
L	E	P	NP	P	L	H

1. "X" is any logic value, "H" is a logic high (true) value, and "L" is a logic low (false) value. "E" indicates the driver is enabled (DIS = L or EN = H), "D" indicates the driver is disabled (DIS = H or EN = L). Input pins should always be connected to either logic high or low. Logic values listed in this table are assumed to transition at the same time as the power supply state.
2. "NP" is the "not powered" state; "P" is the "powered" state, and "—" is an irrelevant state.
3. "H" is a logic high (true) value, and "L" is a logic low (false). The logic low (L) value is enforced by the Shutdown Clamp if the same side gate driver's supply (VDDA/B) is not powered (NP).
4. "Not powered" (NP) state is defined as  $VDDI < VDDI_{UV}$ . "Powered" (P) state is defined as  $VDDI > VDDI_{UV}$ .
5. "Not powered" (NP) state is defined as  $VDDA/B < VDDA/B_{UV}$ . "Powered" (P) state is defined as  $VDDA/B > VDDA/B_{UV}$ .

### 4.2. Power Sequence and Timing Behavior

The device exhibits different timing behavior depending on the state of the power supplies, as well as the driver inputs. In Figure 13 below, the analog power supply voltages are plotted against the digital input and output state of the device, with relevant device timings listed.



**Figure 13. Gate Driver Timing Behavior**

Note that this diagram shows the timing relationship between VDDA, VIA/PWM and VOA. However, the same timing relationship applies for VDDDB, VIB and VOB.

### 4.3. Undervoltage Lockout

Undervoltage Lockout (UVLO) is provided to prevent erroneous operation during device startup and shutdown or when VDDI or VDDA/B is below its specified operating circuits range. The power supplies associated with the logic input, gate driver A, and gate driver B, each have undervoltage lockout monitors. The device's logic input enters UVLO when  $VDDI \leq VDDI_{UV-}$ , and exits UVLO when  $VDDI > VDDI_{UV+}$ . The gate driver outputs, VOA and VOB, remain low when the logic input supply of the device is in UVLO and their respective power supply (VDDA/B) is within the specified range. Each gate driver output can enter or exit UVLO independently. For example, VOA unconditionally enters UVLO when VDDA falls below  $VDDA_{UV-}$  and exits UVLO when VDDA rises above  $VDDA_{UV+}$ , while simultaneously, VOB will behave as described in the Truth Tables if its related power supply, VDDB, is not in UVLO. See "4.1. Truth Tables" on page 9 and "4.2. Power Sequence and Timing Behavior" on page 11 for more details.

### 4.4. Logic Input Signals

#### 4.4.1. Control Inputs

VIA, VIB, PWM, EN, and DIS inputs are CMOS level-compatible, active-high inputs. When VDDI is in undervoltage lockout (UVLO), the inputs of these pins are ignored and the gate driver's outputs are pulled low. Disregarding the overlap protection behavior, for VIA/VIB input devices, the output follows the corresponding VIA or VIB input logic. For PWM input devices, VOA is high and VOB is low when the PWM input is high, and VOA is low and VOB is high when the PWM input is low. Please refer to "4.1. Truth Tables" on page 9 and "4.5. Dead Time Control and Overlap Protection" on page 13 for detailed information on overlap protection behavior.

#### 4.4.2. Enable and Disable Input

For devices with an enable (EN) input, when the EN input is driven low, it unconditionally drives VOA and VOB low regardless of the states of VIA and VIB. Device operation terminates within  $t_{DID}$  after EN falls below  $V_{IL}$  and resumes within  $t_{EID}$  after EN rises above  $V_{IH}$ . For devices with a disable (DIS) input, when the DIS input is brought high, it unconditionally drives VOA and VOB low regardless of the states of VIA and VIB. Device operation terminates within  $t_{DID}$  after DIS rises above  $V_{IH}$  and resumes within  $t_{EID}$  after DIS falls below  $V_{IL}$ . See "4.2. Power Sequence and Timing Behavior" on page 11 for more details. The EN and DIS inputs have no effect if VDDI is below its UVLO level (i.e., VOA, VOB remain low).

#### 4.4.3. Deglitch Filter

A deglitch feature is provided on some devices. The deglitch feature ignores input noise with a duration shorter than the deglitch filter setting, but also introduces additional propagation delay. See "6.2.4. Timing Characteristics" on page 28 for the delays associated with this feature. The deglitch filter can be adjusted by selecting different product options. See "10. Ordering Guide" on page 46 for more details.

#### 4.5. Dead Time Control and Overlap Protection

Dead time provides a user-programmable delay between the transitions of VOA and VOB. This delay is programmed by connecting a resistor ( $R_{DT}$ ) between the DT pin and ground. The appropriate value for  $R_{DT}$  can be determined from [Equation 1](#) below.

$$t_{DT} = 1.73 \times R_{DT} + 5.74$$

Where:

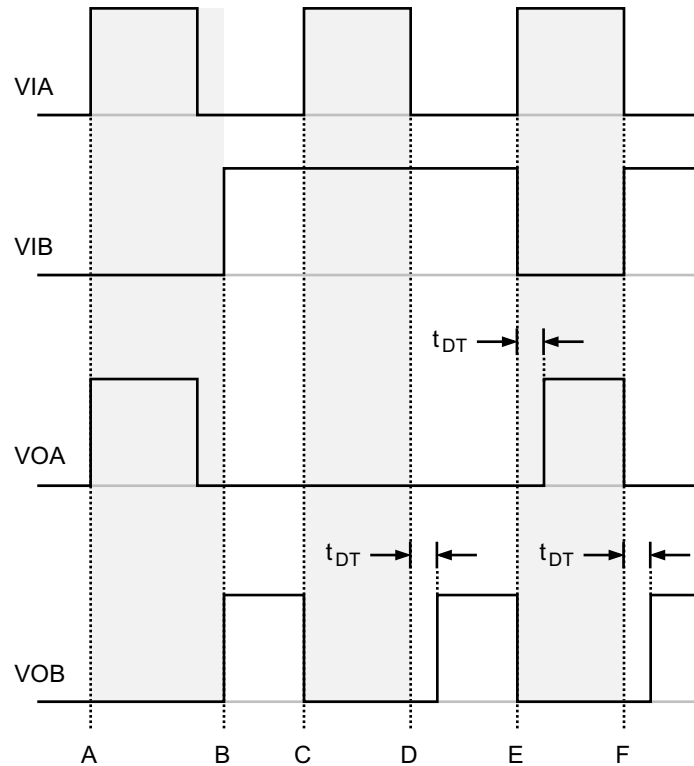
$t_{DT}$  is the Typical Dead Time delay (ns)

$R_{DT}$  is the Dead Time Resistor (k $\Omega$ )

##### Equation 1.

The DT pin operates by outputting 0.9 V and monitoring the DT pin current.  $R_{DT}$  can be varied from 10 k $\Omega$  to 110 k $\Omega$ . With larger values of  $R_{DT}$ , the DT pin current can be very small and influenced by noise in the surrounding system. To aid in noise immunity, place a 0.1  $\mu$ F ceramic capacitor in parallel with  $R_{DT}$ . The capacitor should be placed as close to the DT pin as possible.

An input signal's falling edge activates the programmed dead time for the other signal. The output's dead time is always set to the longer of either the driver's programmed dead time or the input signal's own dead time. If both inputs are high simultaneously, both outputs will be immediately driven low. This overlap protection feature is used to prevent a shoot-through event and does not affect the programmed dead time setting for normal operation. [Figure 14, "Dead Time and Overlap Protection Behavior,"](#) on [page 14](#) illustrates and explains various driver dead time logic operating conditions.



**Figure 14. Dead Time and Overlap Protection Behavior**

For signal conditions designated A through F in the figure, note the following:

- A. The output VOA follows the input VIA exactly because VIB is already low.
- B. The output VOB follows the input VIB exactly because VIA is already low.
- C. The VIA input transitions high while the VIB input is already high. This causes both outputs, VOA and VOB, to immediately transition low due to overlap protection.
- D. The VIA input transitions low and assigns the programmed dead time to VOB. Output VOB is allowed to transition high after the programmed dead time.
- E. The VIA input transitions high simultaneously with the VIB input transitioning low. Output VOB immediately transitions low and assigns the programmed dead time to output VOA. The output VOA is allowed to transition high after the programmed dead time.
- F. The VIB input transitions high simultaneously with the VIA input transitioning low. Output VOA immediately transitions low and assigns the programmed dead time to output VOB. The output VOB is allowed to transition high after the programmed dead time.

For devices in the Universal configuration, both dead time and overlap protection can be disabled by connecting the DT input pin to VDDI, forcing the device to operate as a dual driver instead of a High-Side/Low-Side driver. The output VOA tracks the VIA input and output VOB tracks the VIB input without any intervening protection mechanisms.

Refer to “10. Ordering Guide” on page 46 for details on which specific OPNs provide dead time and overlap protection.

#### 4.6. Short-Circuit Clamp

The short circuit clamp is used to clamp voltages at the driver output (VOA/B) to slightly higher than the VDDA/B voltage during short-circuit conditions. The short circuit clamp helps protect the driven switch gate from overvoltage breakdown or degradation. The clamp is implemented by adding a diode connection between VOA/B and the VDDA/B pins inside the driver. See “6.2.3. Gate Driver Characteristics” on page 27 for detailed specifications of this clamping feature. External diodes between VOA/B and VDDA/B can increase current conduction capability as needed.

#### 4.7. Thermal Protection

The device includes a temperature sensor in each gate driver. Each sensor is monitored continuously. If the temperature exceeds the Trigger Temperature ( $T_{SD+}$ ), a thermal shutdown fault will occur, and the driver will pull low. After 1 ms, if the driver temperature fails to fall below the Reset Temperature ( $T_{SD-}$ ), the driver will pull weakly low. The driver will continuously pull weakly low until the temperature falls below  $T_{SD-}$ . Once the fault is removed, normal operation resumes.

#### 4.8. Shutdown Clamp

The device includes a voltage clamp between the gate driver output (VOA/B) and ground (GNDA/B) when the gate driver is unpowered ( $VDDA/B = \text{high-Z}$ ). This clamp is sometimes referred to as an “active pull-down clamp”. It provides a path to ground for transient currents that could otherwise cause parasitic turn-on of a driven switch when the gate driver is unpowered. See “6.2.3. Gate Driver Characteristics” on page 27 and “4.1. Truth Tables” on page 9 for details.

### 4.9. ESD Structure

The Si82Ex device’s I/O pin electrostatic discharge (ESD) diodes and associated supply pin ESD clamp diodes are illustrated in Figure 15, “Device ESD Structure,” below. On the logic input side, a pair of ESD protection diodes are used on each input pin, and all upper diodes are connected to one shared clamp diode. This structure prevents the VDDI pin from being powered up through the input pin when the VDDI power supply is lost. The other clamp diode is present between the VDDI and GNDI pins. The ESD structure of the gate driver output is similar to the logic input, except that the upper diode is connected to a clamp diode at the VDDA/B pins.

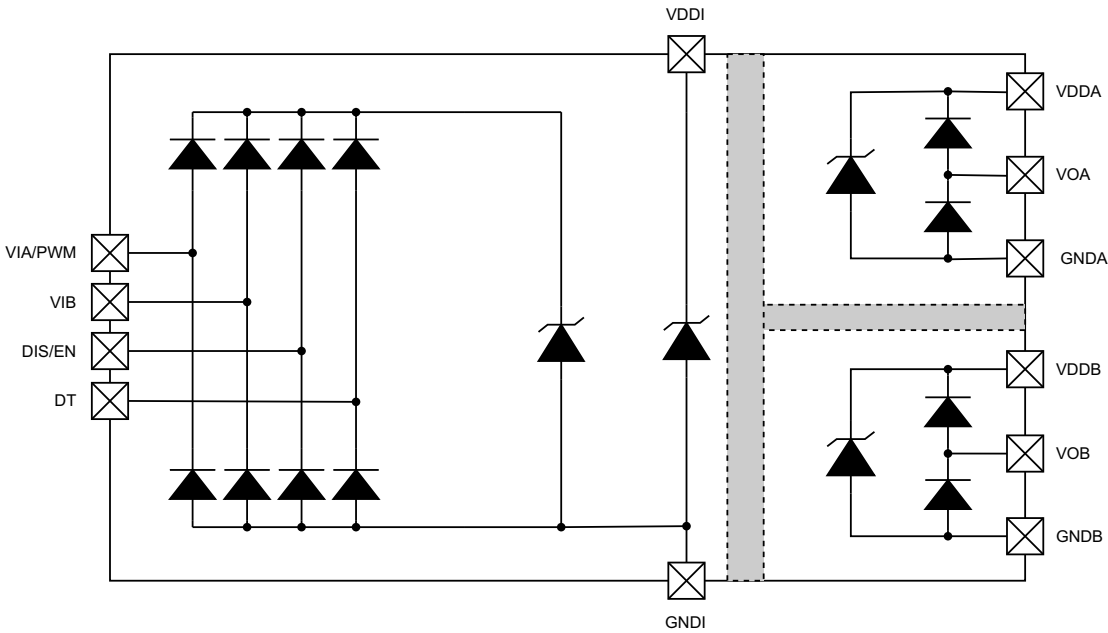


Figure 15. Device ESD Structure



## 5. Application Information

The device is designed to be both flexible and robust to meet a wide range of application requirements, safely survive overloads, and rapidly recover normal operation. To achieve these objectives, the appropriate configuration must be selected and its circuit carefully designed.

### 5.1. Recommended Application Circuits

Figure 16, “High-Side/Low-Side Configuration,” on page 18 illustrates a typical application circuit for a dual-input Si82Ex device connected in a half-bridge topology. Driver A of the Si82Ex device controls the high-side FET (Q1), and driver B controls the low-side FET (Q2). The controller provides the Si82Ex input signals (VIA and VIB) to control Driver A and Driver B. The Si82Ex device’s input overlap protection feature ensures no concurrent conduction of FETs Q1 and Q2, even if both VIA and VIB input signals are High. The dead time is inserted before the rising edge of the gate drive signals. Since Q1 and Q2 FETs do not turn on or turn off instantly, the inserted dead time guarantees the opposite FET is completely off before the Si82Ex device turns on FETs Q1 or Q2. The dead time is adjustable through the R10 resistor connected to the DT pin. The controller can also use the EN/DIS signal to turn off both drivers immediately once a system fault is detected.

On the gate driver side, the Si82Ex device’s output current is controlled by the external gate resistors R5, R6, R12, and R15. The peak sourcing current for gate drivers A and B is shown in Equation 2 and Equation 3, respectively.

$$\frac{VDDA}{R5 + R_{ONA+}}$$

Equation 2. Peak Sourcing Current Gate Driver A

$$\frac{VDDB}{R12 + R_{ONB+}}$$

Equation 3. Peak Sourcing Current Gate Driver B

The peak sinking current for gate drivers A and B is shown in Equation 4 and Equation 5, respectively.

$$\frac{VDDA}{R5 \parallel R6 + R_{ONA-}}$$

Equation 4. Peak Sinking Current Gate Driver A

$$\frac{VDDB}{R12 \parallel R15 + R_{ONB-}}$$

Equation 5. Peak Sinking Current Gate Driver B

The gate resistor values should be selected to meet the gate voltage rise-time/fall-time requirement based on the actual capacitive loading of FETs, Q1 and Q2. G2 is the reference point or the reference ground of the gate drive output circuit. Figure 16, “High-Side/Low-Side Configuration,” on page 18 also shows two possible power supply connections for the high-side gate driver A. VDDA can be powered by an isolated supply or powered by the same supply for gate driver B through the bootstrap circuit (resistor R1 and diode D1). The bootstrap circuit is the convenient way to power the high-side gate driver for the high-side / low-side circuit configuration. Its basic operation follows. When FET Q2 is turned on, capacitors C4 and C5 are charged by the low-side VDDB supply through diode D1 and the conducting FET Q2. After FET Q2 is off when FET Q1 is turned on, the reference potential of capacitors C4 and C5 jumps to VBUS, and thus diode D1 is reverse biased. In this situation, capacitors C4 and C5 act as the voltage source supplying current to gate driver A in order to maintain a logic high output. Resistor R1 is used to limit the inrush current of capacitors C4 and C5. Resistor R1 additionally limits the voltage slew rate between gate driver A’s supply pins (VDDA and GNDA). More details about the bootstrap circuit can be found in “AN486: High-Side Bootstrap Design Using ISODrivers in Power Delivery Systems”.

Two high-voltage Y2-class capacitors (not shown in the diagram) between the logic input reference (GNDI) and the two gate driver references (GNDA and GNDB) are recommended if additional radiated emissions or electrostatic discharge (ESD) mitigation is desired. The typical value for these two Y2 capacitors is between 47 pF and 100 pF. See “AN1131: Design Guide for Reducing Radiated and Conducted Emissions in Isolated Systems Using Skyworks’ Isolators” for additional techniques for mitigating radiated and conducted emissions. Note that the Si82Ex device provides excellent common-mode transient immunity (CMTI) without employing any additional components or techniques. However, if your application requires extremely high common-mode transient immunity (CMTI) performance, it is recommended to add a 10 nF capacitor between each of the logic input pins and the logic input ground (GNDI), including the no-connect (NC) pins. This will help improve CMTI performance.

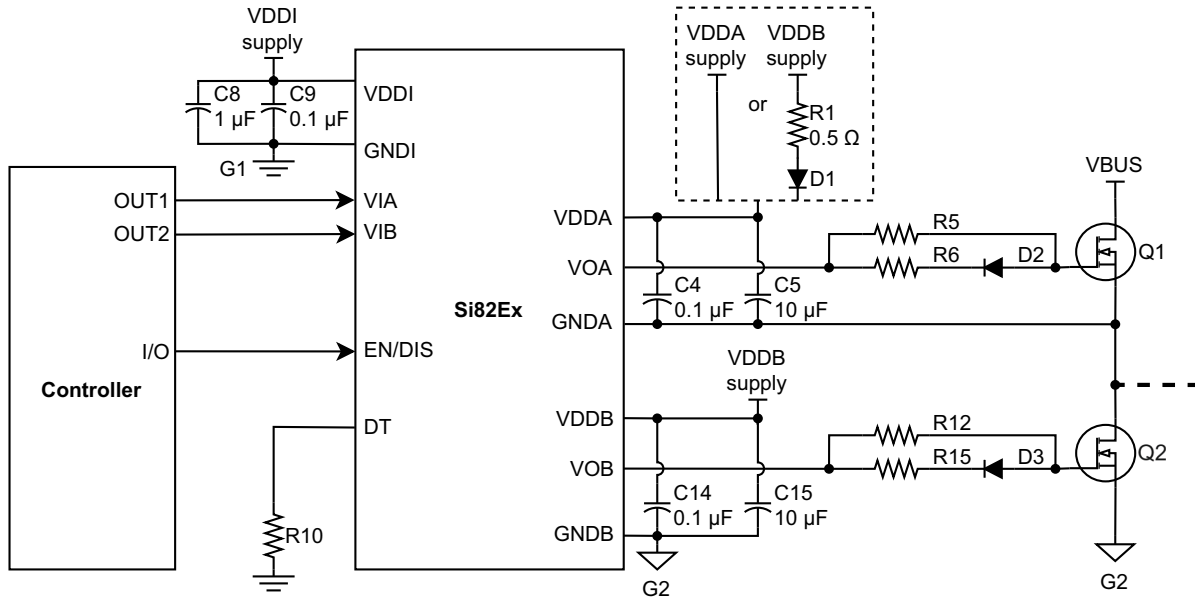


Figure 16. High-Side/Low-Side Configuration

Figure 17, “Bipolar Output Connection,” on page 19 is similar to the above high-side/low-side configuration except that the drivers produce bipolar  $V_{GS}$  output voltage. The bipolar  $V_{GS}$  output requires the system to provide positive and negative voltage sources. Please note that the bootstrap circuit cannot be used to share the low-side voltage sources with the high-side gate driver A for a bipolar  $V_{GS}$  output application. In this example, +15 V and –5 V sources are used for low-side gate driver B, and its reference point is also G2. The other set of +15 V and –5 V sources are used for the high-side gate driver A. The high-side voltage sources' reference G3 is electrically connected to FET Q1's source. Please note that the voltage potential at FET Q1's source jumps between VBUS and reference G2. Thus, the high-side voltage sources need to be isolated from reference G2 as well.

For the bipolar  $V_{GS}$  output application, the additional bypass capacitors form a capacitor divider in order to shorten the current flow loop. These capacitors should be placed close to the Si82Ex device's output power pins (VDDA/B). Taking the high-side gate driver A as an example, the ac component of the gate drive current flows from the VDDA net to the Si82Ex device's VDDA pin, VOA pin, external gate resistor, Q1's gate, Q1's source, the midpoint of capacitors C1 and C2, and back to VDDA. Since the original bypass capacitors C4 and C5 don't connect to reference G3 (which is connected to FET Q1's source), without capacitor C2, the return current needs to travel further to the system's +15 V source to complete the loop. This prolonged loop increases the chance of radiated emissions. Capacitors C11 and C12 serve the same purpose for the low-side FET Q2's gate drive return current.

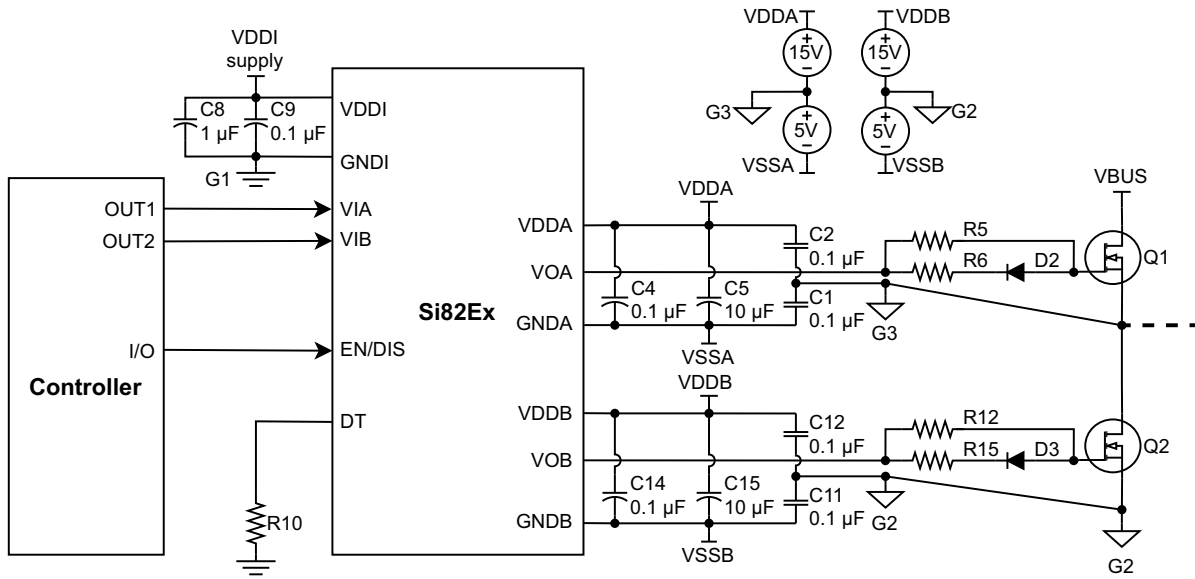


Figure 17. Bipolar Output Connection

Figure 18. "PWM Input Application Circuit" below depicts an Si82Ex device with a high-side/low-side configuration and a PWM input. This application circuit is similar to Figure 16, "High-Side/Low-Side Configuration," on page 18 above, except that the controller only provides the PWM input signal. The Si82Ex device will split the input signal phase, insert dead time, and drive the high-side and low-side FETs accordingly.

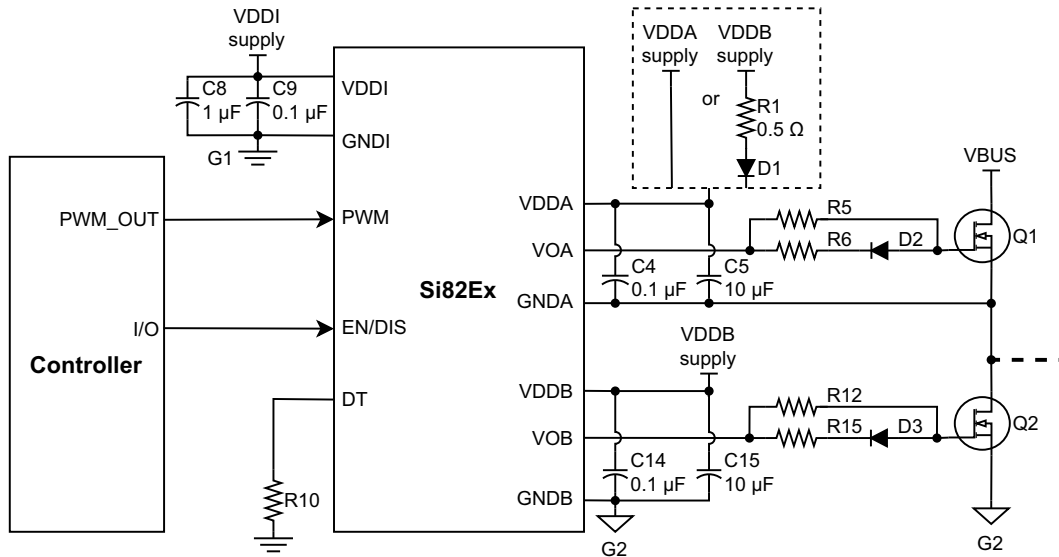


Figure 18. PWM Input Application Circuit

Figure 19, “Dual Low-Side Driver Application Circuit,” below depicts the circuit for driving dual low-side FETs. When the dead time pin (DT) is tied to the logic input supply (VDDI), the Si82Ex device operates as a dual gate driver without overlap protection or dead time insertion. In this dual driver mode, the Si82Ex device can be used for high-side/low-side, dual high-side, dual low-side, or any circuit topology. However, the controller is responsible for providing overlap protection and dead time insertion. In the dual low-side circuit topology depicted below, the +15 V and –5 V sources are shared by gate drivers A and B to generate bipolar  $V_{GS}$  outputs. For a dual high-side application, Driver A and B cannot share the same power supply and will require the individual isolated power supplies, even if the  $V_{GS}$  output is unipolar.

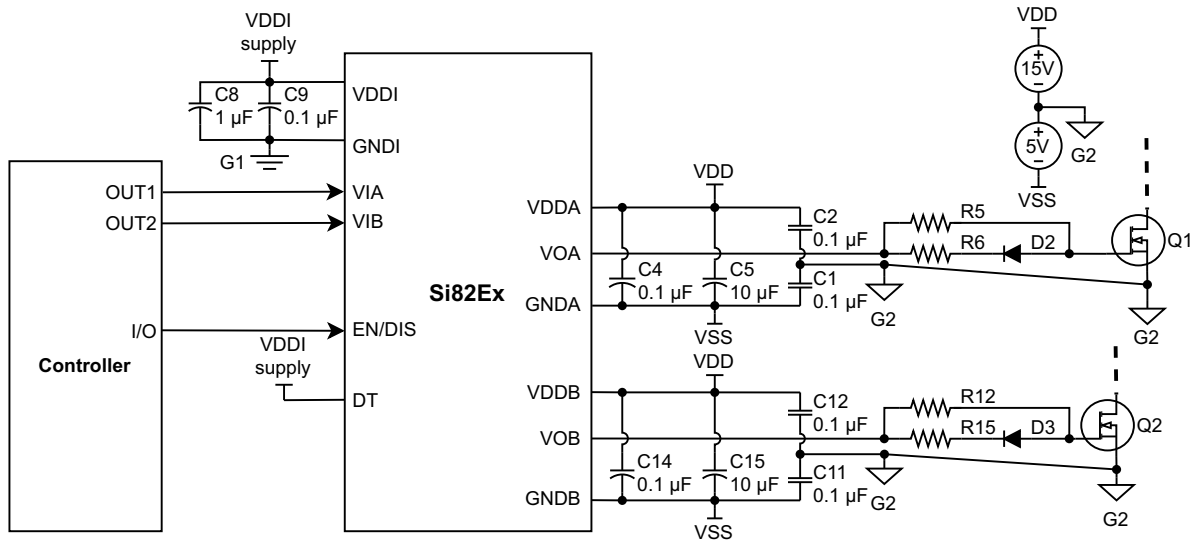


Figure 19. Dual Low-Side Driver Application Circuit

## 5.2. Layout Considerations

The layout considerations are divided into general considerations for the entire device, the logic input side of the device, and the gate driver side. Please refer to “5.1. Recommended Application Circuits” on page 17 for specific parts referenced.

### 5.2.1. General Considerations

- The bypass capacitors (usually 0.1  $\mu\text{F}$  || 10  $\mu\text{F}$ ) should be placed close to the device's power supply pins and connected to the device with thick and short traces.
- The isolation barrier should have the required distance for the traces, power planes, ground planes, and copper areas on the device's logic input and gate drive sides.
- Safety isolation between gate drivers A and B on the gate driver side is usually not required. If the system needs safety isolation between gate drivers A and B, the trace, power plane, ground plane, and the copper area between the two gate drivers should have the required distance. Even though safety isolation between gate drivers A and B is usually not required, to avoid arcing through the air, the traces operating at high voltage should have some distance (approximately 1 mm per 1 kV) from the low voltage signals.
- The Si82Ex device is often used in high-power systems with significant switching current and transient voltage. Attention should be paid to the proximity and orientation of the Si82Ex device and any high-current switching circuits. This should also apply to the traces and components surrounding the Si82Ex device to avoid unwanted noise coupling.

### 5.2.2. Logic Input Considerations

- Place resistor R10 close to the Si82Ex device's dead time (DT) pin.
- If the application requires extremely high common mode transient immunity (CMTI) performance, it is recommended to add a 10 nF capacitor between each of the logic input pins and the logic input ground (GNDI), including the no connect (NC) pins. This will help improve the CMTI performance.
- Using  $\geq 6$  mil trace width on all logic input pins is recommended. The interconnection between the controller and the Si82Ex device should be kept from any noisy signals in the system.

### 5.2.3. Gate Driver Considerations

- If the system is designed to provide a bipolar  $V_{GS}$  output, additional bypass capacitors (C1, C2, C11, and C12 in [Figure 17, “Bipolar Output Connection,” on page 19](#)) are required to minimize the return path length of the gate drive signals.
- It is recommended to use  $\geq 20$  mil trace width for the VOA/B gate driver traces and their return path.
- For a unipolar  $V_{GS}$  output, the return path of the  $V_{GS}$  gate drive signal is from the power device's source/collector to the Si82Ex device's gate driver ground pin (GNDA/B). Explicitly use  $\geq 20$  mil trace width for this return current path and route this trace close to the VOA/B gate driver traces to reduce the loop area of the whole  $V_{GS}$  gate drive signal. Moreover, it is a good practice to set the copper keep-out region along the return path trace so the system ground copper will not flood over this return trace.
- For a bipolar  $V_{GS}$  output, the return path of the  $V_{GS}$  gate drive signal is from the power device's source/collector to the midpoint of capacitors C1/C2 or C11/C12. Therefore, these capacitors must be placed close to the Si82Ex device to minimize this current loop. Explicitly use  $\geq 20$  mil trace width for the return current path and route this return trace close to the VOA/VOB gate driver traces to reduce the loop area of the whole  $V_{GS}$  gate drive signal. Moreover, it is a good practice to set the copper keep-out region along the return path trace so the system ground copper will not flood over this return trace.
- For a multiple-layer PCB design, ground and power planes are recommended to create a power supply current path with the least inductance. If there is no dedicated power or ground plane on the gate driver side, please use  $\geq 20$  mil trace width for the power supply connections.
- If the design utilizes Y2 capacitors between the logic input and gate drivers, the Y2 capacitors across the isolation barrier should be placed as close as possible to the sides of the Si82Ex device without pins.

### 5.3. Power Dissipation Considerations

The device's average power dissipation is often required in order to estimate the silicon junction temperature and can be estimated using the equation provided in [“AN1339: Driver Power Dissipation Considerations”](#). To solve the equation, the intended supply voltages, the load characteristics, the gate resistor values, and the switching frequency need to be collected. Skyworks provides a Microsoft Excel® based calculator as part of [AN1339](#) to easily estimate the device's power dissipation and silicon junction temperature.

## 6. Specifications

### 6.1. Absolute Maximum Ratings

**Table 4. Absolute Maximum Ratings<sup>1</sup>**

Parameter	Symbol	Condition	Min	Max	Unit
Storage temperature	T <sub>STG</sub>		-65	150	°C
Operating temperature	T <sub>A</sub>		-40	125	°C
Junction temperature	T <sub>J</sub>		—	150	°C
Logic input supply voltage	VDDI		-0.30	24.0	V
Gate driver supply voltage	VDDA, VDDB		-0.30	36.0	V
Input signal voltage	VIA, VIB, PWM, DT, EN, DIS		-0.30	VDDI + 0.30	V
	VIA, VIB, PWM, EN, DIS	Transient for 100 ns <sup>2</sup>	-5.00	VDDI + 0.30	V
Output signal voltage	VOA, VOB		-0.30	V <sub>DDA/B</sub> + V <sub>SCCA/B</sub>	V
		Transient for 200 ns <sup>2</sup>	-2.00	V <sub>DDA/B</sub> + V <sub>SCCA/B</sub>	V
Lead solder temperature		Duration = 10 s	—	260	°C
<b>ESD per AEC-Q100</b>					
Human body model	HBM		-4	4	kV
Charged device model	CDM		-2	2	kV

1. Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. This parameter is not subject to production test. It is guaranteed by characterization.

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*ESD Handling: Industry-standard ESD handling precautions must be adhered to at all times to avoid damage to this device.*

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## 6.2. Electrical Characteristics

The following tables provide electrical parametric data for this device.

### 6.2.1. Power Supply Characteristics

**Table 5. Power Supply Characteristics<sup>1</sup>**

Operating range for the following specifications: VDDI = 3.0–20 V; VDDA/B = 5.0–30 V; T<sub>A</sub> = –40 to +125 °C; F<sub>IN</sub> ≤ 1 MHz.

Typical specifications: VDDI = 5 V; VDDA/B = 6 V for 4 V UVLO devices, 10 V for 8 V UVLO devices, 15 V for 12 V UVLO devices, 18 V for 15 V UVLO devices; T<sub>A</sub> = 25 °C unless otherwise noted.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>Supply Voltage</b>						
Logic Input Supply	VDDI		3.00	—	20.0	V
Gate Driver Supply	VDDA, VDDB		5.00	—	30.0	V
<b>Supply Current</b>						
<b>Logic Input Supply</b>						
Quiescent Current	IDDI <sub>Q</sub>	EN = logic low or DIS = logic high	—	1.03	1.35	mA
Active Current	IDDI	VIA/B = 1 MHz; 50% duty cycle	—	2.04	2.39	mA
<b>Gate Driver Supply</b>						
<b>4 V Undervoltage Lockout (Si82ExxxGx) Devices</b>						
Quiescent Current	IDDA <sub>Q</sub> , IDDB <sub>Q</sub>	EN = logic low or DIS = logic high	—	2.40	3.50	mA
Active Current	IDDA, IDDB	VOA/B = 1 MHz; 50% duty cycle; no load	—	5.59	12.58	mA
<b>8 V Undervoltage Lockout (Si82ExxxBx) Devices</b>						
Quiescent Current	IDDA <sub>Q</sub> , IDDB <sub>Q</sub>	EN = logic low or DIS = logic high	—	2.43	3.50	mA
Active Current	IDDA, IDDB	VOA/B = 1 MHz; 50% duty cycle; no load	—	6.72	12.58	mA
<b>12 V Undervoltage Lockout (Si82ExxxCx) Devices</b>						
Quiescent Current	IDDA <sub>Q</sub> , IDDB <sub>Q</sub>	EN = logic low or DIS = logic high	—	2.46	3.50	mA
Active Current	IDDA, IDDB	VOA/B = 1 MHz; 50% duty cycle; no load	—	7.95	12.58	mA
<b>15 V Undervoltage Lockout (Si82ExxxEx) Devices</b>						
Quiescent Current	IDDA <sub>Q</sub> , IDDB <sub>Q</sub>	EN = logic low or DIS = logic high	—	2.49	3.50	mA
Active Current	IDDA, IDDB	VOA/B = 1 MHz; 50% duty cycle; no load	—	8.67	12.58	mA



**Table 5. Power Supply Characteristics<sup>1</sup> (Continued)**

Operating range for the following specifications: VDDI = 3.0–20 V; VDDA/B = 5.0–30 V; T<sub>A</sub> = –40 to +125 °C; F<sub>IN</sub> ≤ 1 MHz.

Typical specifications: VDDI = 5 V; VDDA/B = 6 V for 4 V UVLO devices, 10 V for 8 V UVLO devices, 15 V for 12 V UVLO devices, 18 V for 15 V UVLO devices; T<sub>A</sub> = 25 °C unless otherwise noted.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>Undervoltage Lockout</b>						
<b>Logic Input Supply</b>						
Positive-Going Threshold	VDDI <sub>UV+</sub>	VDDI rising	2.76	2.88	2.99	V
Negative-Going Threshold	VDDI <sub>UV–</sub>	VDDI falling	2.64	2.78	2.94	
Threshold Hysteresis	VDDI <sub>HYS</sub>		—	100	—	mV
<b>Gate Driver Supply</b>						
<b>4 V Undervoltage Lockout (Si82ExxxGx) Devices</b>						
Positive-Going Threshold	VDDA <sub>UV+</sub> , VDDB <sub>UV+</sub>	VDDA/B rising	4.09	4.30	4.54	V
Negative-Going Threshold	VDDA <sub>UV–</sub> , VDDB <sub>UV–</sub>	VDDA/B falling	3.89	4.10	4.33	
Threshold Hysteresis	VDDA <sub>HYS</sub> , VDDB <sub>HYS</sub>		—	200	—	mV
<b>8 V Undervoltage Lockout (Si82ExxxBx) Devices</b>						
Positive-Going threshold	VDDA <sub>UV+</sub> , VDDB <sub>UV+</sub>	VDDA/B rising	7.58	8.07	8.55	V
Negative-Going Threshold	VDDA <sub>UV–</sub> , VDDB <sub>UV–</sub>	VDDA/B falling	7.14	7.57	8.05	
Threshold Hysteresis	VDDA <sub>HYS</sub> , VDDB <sub>HYS</sub>		—	500	—	mV
<b>12 V Undervoltage Lockout (Si82ExxxCx) Devices</b>						
Positive-Going Threshold	VDDA <sub>UV+</sub> , VDDB <sub>UV+</sub>	VDDA/B rising	11.21	11.90	12.61	V
Negative-Going Threshold	VDDA <sub>UV–</sub> , VDDB <sub>UV–</sub>	VDDA/B falling	10.29	10.90	11.52	
Threshold Hysteresis	VDDA <sub>HYS</sub> , VDDB <sub>HYS</sub>		—	1.00	—	V
<b>15 V Undervoltage Lockout (Si82ExxxEx) Devices</b>						
Positive-Going Threshold	VDDA <sub>UV+</sub> , VDDB <sub>UV+</sub>	VDDA/B rising	14.19	15.15	16.13	V
Negative-Going Threshold	VDDA <sub>UV–</sub> , VDDB <sub>UV–</sub>	VDDA/B falling	13.81	14.70	15.66	
Threshold Hysteresis	VDDA <sub>HYS</sub> , VDDB <sub>HYS</sub>		—	450	—	mV

1. Adding the suffix A/B to any symbol, parameter, or test condition variable denotes that the term applies interchangeably to either Gate Driver A or Gate Driver B.

## 6.2.2. Logic Input Characteristics

**Table 6. Logic Input Characteristics**

Operating range for the following specifications: VDDI = 3.0–20 V; VDDA/B = 5.0–30 V;  $T_A = -40$  to  $+125$  °C;  $F_{IN} \leq 1$  MHz.

Typical specifications: VDDI = 5 V; VDDA/B = 6 V for 4 V UVLO devices, 10 V for 8 V UVLO devices, 15 V for 12 V UVLO devices, 18 V for 15 V UVLO devices;  $T_A = 25$  °C unless otherwise noted.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>Input Threshold</b>						
High Input	$V_{IH}$	VIA, VIB, PWM, EN, DIS rising	VDDI x 0.75	—	—	V
Low Input	$V_{IL}$	VIA, VIB, PWM, EN, DIS falling	—	—	VDDI x 0.25	V
Hysteresis	$V_{HYS}$	VIA, VIB, PWM, EN, DIS	VDDI x 0.10	VDDI x 0.15	—	V
Input Pull-Down Resistance	$R_I$	VIA, VIB, PWM, EN, DIS	125	200	320	k $\Omega$
Input Leakage Current	$ I_{LKG} $	VIA, VIB, PWM, EN, DIS	—	—	140	$\mu$ A

6.2.3. Gate Driver Characteristics

Table 7. Gate Driver Characteristics<sup>1</sup>

Operating range for the following specifications: VDDI = 3.0–20 V; VDDA/B = 5.0–30 V; T<sub>A</sub> = –40 to +125 °C; F<sub>IN</sub> ≤ 1 MHz

Typical specifications: VDDI = 5 V; VDDA/B = 6 V for 4 V UVLO devices, 10 V for 8 V UVLO devices, 15 V for 12 V UVLO devices, 18 V for 15 V UVLO devices; T<sub>A</sub> = 25 °C unless otherwise noted.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>Output Voltage</b>						
Logic high (sourcing)	V <sub>OHA</sub> , V <sub>OHB</sub>	I <sub>OA/B</sub> = –20 mA	VDDA/B x 0.98	—	—	V
Logic low (sinking)	V <sub>OLA</sub> , V <sub>OLB</sub>	I <sub>OA/B</sub> = 20 mA	—	—	0.10	V
<b>Output Resistance</b>						
Logic high (sourcing)	R <sub>ONA+</sub> , R <sub>ONB+</sub>		0.50	1.00	2.50	Ω
Logic low (sinking)	R <sub>ONA-</sub> , R <sub>ONB-</sub>		0.30	0.70	2.20	Ω
<b>Peak Output Current</b>						
Logic high (sourcing)	I <sub>OA+</sub> , I <sub>OB+</sub>	VDDA/B = 6 V, VOA/B = 1.5 V	—	3.80	—	A
		VDDA/B = 10 V, VOA/B = 3 V	—	5.40	—	A
		VDDA/B = 15 V, VOA/B = 5 V	—	6.65	—	A
		VDDA/B = 18 V, VOA/B = 6 V	5.50	7.50	—	A
Logic Low (sinking)	I <sub>OA-</sub> , I <sub>OB-</sub>	VDDA/B = 6 V, VOA/B = 4.5 V	—	5.10	—	A
		VDDA/B = 10 V, VOA/B = 7 V	—	6.55	—	A
		VDDA/B = 15 V, VOA/B = 10 V	—	7.40	—	A
		VDDA/B = 18 V, VOA/B = 12 V	5.50	7.50	—	A
<b>Switch Short Circuit Clamp</b>						
Clamping voltage	V <sub>SCCA</sub> , V <sub>SCCB</sub>	VOA/B – VDDA/B or GNDA/B – VOA/B, I <sub>OA/B</sub> = 70 mA	—	70.0	—	mV
		VOA/B – VDDA/B or GNDA/B – VOA/B, I <sub>OA/B</sub> = 500 mA, t <sub>SCCA/B</sub> = 10 μs	—	530	—	mV
<b>Thermal shutdown</b>						
Threshold temperature	T <sub>SD+</sub>	T <sub>J</sub> rising	—	163	—	°C
Release temperature	T <sub>SD-</sub>	T <sub>J</sub> falling	—	131	—	°C
Shutdown clamp output voltage	V <sub>SDCA</sub> , V <sub>SDCB</sub>	VDDA/B = high-Z, I <sub>OA/B</sub> = 50 mA	—	1.55	2.00	V

1. Adding the suffix A/B to any symbol, parameter, or test condition variable denotes that the term applies interchangeably to either gate driver A or gate driver B.

6.2.4. Timing Characteristics

**Table 8. Timing Characteristics<sup>1</sup>**

Operating range for the following specifications: VDDI = 3.0–20 V; VDDA/B = 5.0–30 V; T<sub>A</sub> = –40 to +125 °C; F<sub>IN</sub> ≤ 1 MHz.

Typical specifications: VDDI = 5 V; VDDA/B = 6 V for 4 V UVLO devices, 10 V for 8 V UVLO devices, 15 V for 12 V UVLO devices, 18 V for 15 V UVLO devices; T<sub>A</sub> = 25 °C unless otherwise noted.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>Minimum Pulse Width</b>						
Si82ExxAx Devices	PW <sub>MINA</sub> , PW <sub>MINB</sub>	No load	—	10.0	—	ns
Si82ExxBx Devices			—	30.0	—	ns
<b>Propagation Delay</b>						
<b>Positive-Going Control Input Delay<sup>2</sup></b>						
0 ns Deglitch (Si82ExxAx) Devices	t <sub>PLHA</sub> , t <sub>PLHB</sub>	VIA, VIB, PWM rising; no load	20.0	30.0	40.0	ns
30 ns Deglitch (Si82ExxBx) Devices			45.0	52.5	65.0	ns
<b>Negative-Going Control Input Delay<sup>2</sup></b>						
0 ns Deglitch (Si82ExxAx) Devices	t <sub>PLHA</sub> , t <sub>PLHB</sub>	VIA, VIB, PWM rising; no load	20.0	30.0	40.0	ns
30 ns Deglitch (Si82ExxBx) Devices			45.0	52.5	65.0	ns
Enable Input Delay <sup>3</sup>	t <sub>EID</sub>	EN rising or DIS falling, no load	20.0	30.0	40.0	ns
Disable Input Delay <sup>3</sup>	t <sub>DID</sub>	EN falling or DIS rising, no load	20.0	30.0	40.0	ns
Pulse Width Distortion	PWD <sub>A</sub> , PWD <sub>B</sub>	t <sub>PLHA/B</sub> – t <sub>PHLA/B</sub>	—	5.00	10.0	ns
<b>Propagation Delay Skew</b>						
<b>Channel-to-Channel<sup>4</sup></b>						
0 ns Deglitch (Si82ExxAx) Devices	t <sub>PSK(CC)</sub>	MAX{  t <sub>PLHA</sub> – t <sub>PLHB</sub>  ,  t <sub>PHLA</sub> – t <sub>PHLB</sub>   }	—	—	5.00	ns
30 ns Deglitch (Si82ExxBx) Devices			—	—	8.00	ns
<b>Part-to-Part<sup>5</sup></b>						
0 ns Deglitch (Si82ExxAx) Devices	t <sub>PSK(PP)</sub>	MAX{  t <sub>PLHX</sub> – t <sub>PLHY</sub>  ,  t <sub>PHLX</sub> – t <sub>PHLY</sub>   }	—	—	5.00	ns
30 ns Deglitch (Si82ExxBx) Devices			—	—	8.00	ns
Output Rise Time <sup>2</sup>	t <sub>RA</sub> , t <sub>RB</sub>	VDDA/B = 6 V, C <sub>L</sub> = 1 nF, R <sub>G</sub> = 0 Ω	—	7.50	—	ns
		VDDA/B = 10 V, C <sub>L</sub> = 1 nF, R <sub>G</sub> = 0 Ω	—	7.20	—	ns
		VDDA/B = 15 V, C <sub>L</sub> = 1 nF, R <sub>G</sub> = 0 Ω	—	7.90	—	ns
		VDDA/B = 18 V, C <sub>L</sub> = 1 nF, R <sub>G</sub> = 0 Ω	—	8.30	—	ns

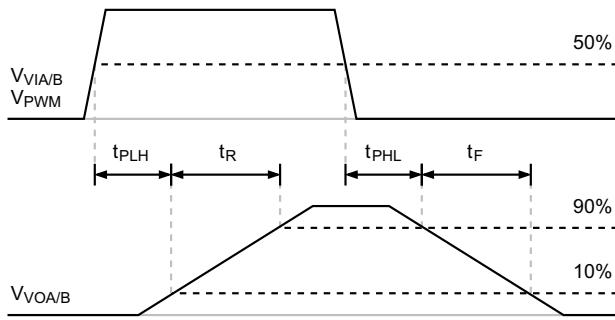
**Table 8. Timing Characteristics<sup>1</sup> (Continued)**

Operating range for the following specifications: VDDI = 3.0–20 V; VDDA/B = 5.0–30 V; T<sub>A</sub> = –40 to +125 °C; F<sub>IN</sub> ≤ 1 MHz.

Typical specifications: VDDI = 5 V; VDDA/B = 6 V for 4 V UVLO devices, 10 V for 8 V UVLO devices, 15 V for 12 V UVLO devices, 18 V for 15 V UVLO devices; T<sub>A</sub> = 25 °C unless otherwise noted.

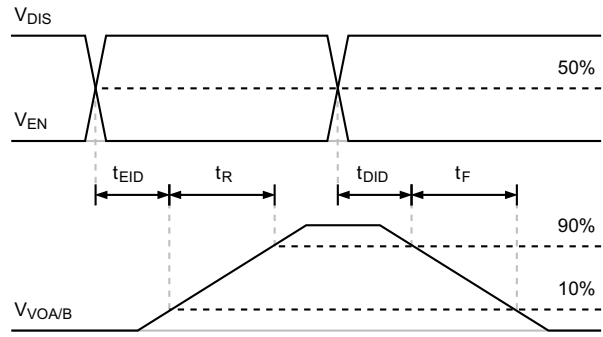
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Fall Time <sup>2</sup>	t <sub>FA</sub> , t <sub>FB</sub>	VDDA/B = 6 V, C <sub>L</sub> = 1 nF, R <sub>G</sub> = 0 Ω	—	6.60	—	ns
		VDDA/B = 10 V, C <sub>L</sub> = 1 nF, R <sub>G</sub> = 0 Ω	—	7.00	—	ns
		VDDA/B = 15 V, C <sub>L</sub> = 1 nF, R <sub>G</sub> = 0 Ω	—	7.95	—	ns
		VDDA/B = 18 V, C <sub>L</sub> = 1 nF, R <sub>G</sub> = 0 Ω	—	8.60	—	ns
Dead Time Control <sup>6</sup>	t <sub>DT</sub>	R <sub>DT</sub> = 10 kΩ	10.0	20.0	30.0	ns
		R <sub>DT</sub> = 60 kΩ	—	110	—	ns
		R <sub>DT</sub> = 110 kΩ	170	200	240	ns
Startup Time <sup>7</sup>	t <sub>ST</sub>		—	125	—	μs
VDDI Logic Input Power Cycle Time <sup>7</sup>	t <sub>PCL</sub>		—	60.0	—	μs
VDDI Logic Input Shutdown Time <sup>7</sup>	t <sub>SDL</sub>		—	90.0	—	μs
VDDA/B Gate Driver Power Cycle Time <sup>7</sup>	t <sub>PCGA</sub> , t <sub>PCGB</sub>		—	125	—	μs
VDDA/B Gate Driver Shutdown Time <sup>7</sup>	t <sub>SDGA</sub> , t <sub>SDGB</sub>		—	7.00	—	μs
Common Mode Transient Immunity	CMTI		200	—	—	kV/μs

1. Adding the suffix A/B to any symbol, parameter, or test condition variable denotes that the term applies interchangeably to either gate driver A or gate driver B.
2. See Figure 20, “Control Input Timing Measurements,” on page 30 for details.
3. See Figure 21, “Enable or Disable Input Timing Measurements,” on page 30 for details.
4. t<sub>PSK(CC)</sub> is the largest absolute value difference in propagation delays between the two channels of a single unit operating at the same supply voltages, load, and ambient temperature. See Figure 22, “Propagation Delay Parameters,” on page 30 for details
5. t<sub>PSK(PP)</sub> is the largest absolute value difference in propagation delays measured between different channels on different units operating at the same supply voltages, load, and ambient temperature.
6. The dead time pin (DT) can be pulled to VDDI to disable dead time control. Using less than 10 kΩ dead time resistor is not recommended. See Figure 23, “Dead Time Timing Measurement,” on page 30 for more information.
7. Startup, power cycle, and shutdown timing are detailed in “4.2. Power Sequence and Timing Behavior” on page 11.



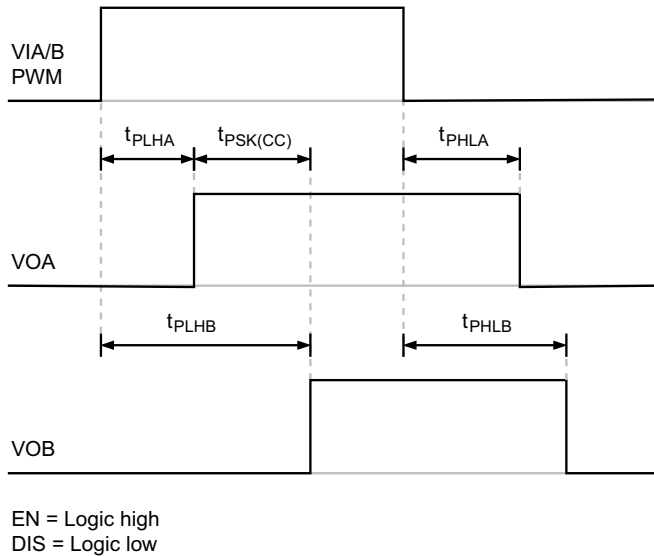
EN = Logic high  
DIS = Logic low

Figure 20. Control Input Timing Measurements



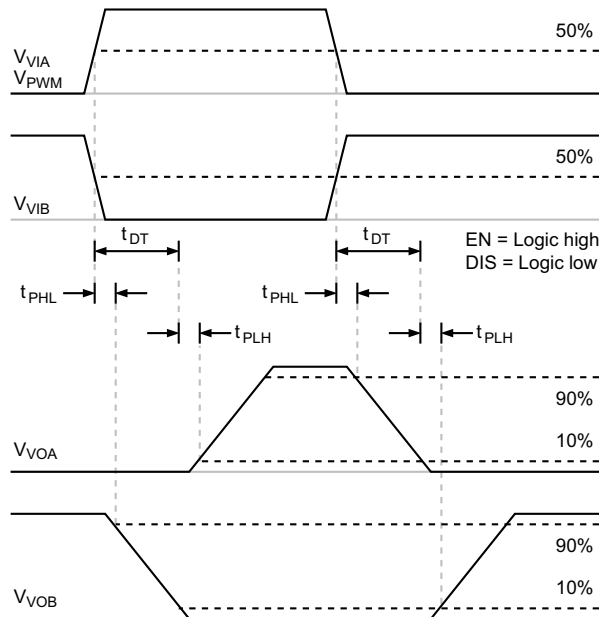
VIA/B or PWM = Logic High

Figure 21. Enable or Disable Input Timing Measurements



EN = Logic high  
DIS = Logic low

Figure 22. Propagation Delay Parameters

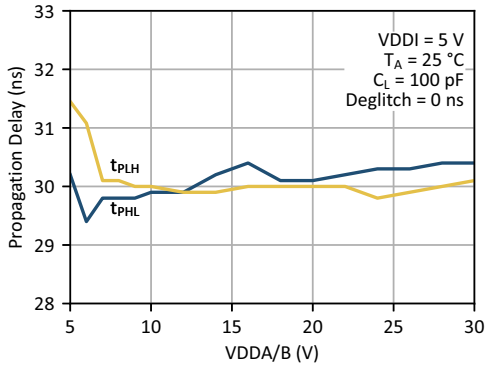


EN = Logic high  
DIS = Logic low

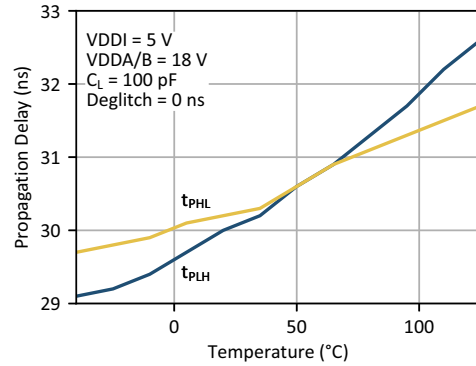
Figure 23. Dead Time Timing Measurement

### 6.3. Typical Performance Characteristics

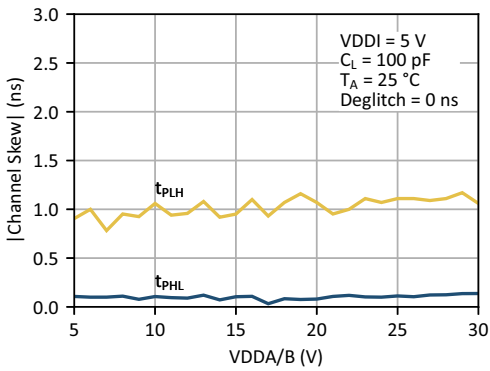
The typical performance characteristics depicted in the figures below are for information purposes only. Refer to the data tables in “6.2. Electrical Characteristics” on page 24 for actual specification limits.



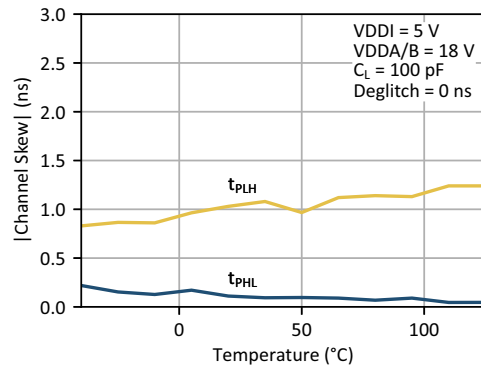
**Figure 24. Propagation Delay vs. Gate Driver Supply Voltage**



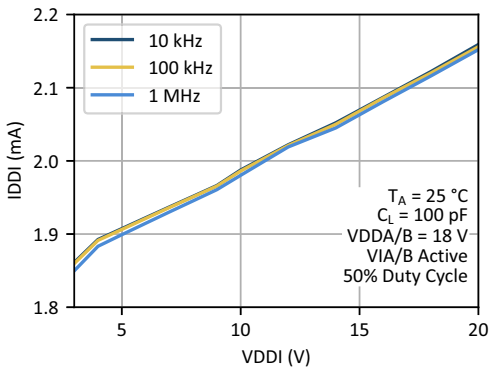
**Figure 25. Propagation Delay vs. Ambient Temperature**



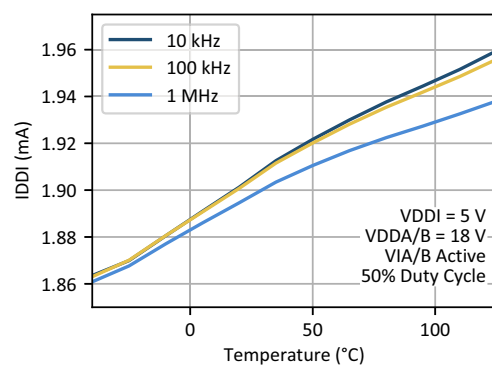
**Figure 26. Channel-to-Channel Skew vs. Gate Driver Supply Voltage**



**Figure 27. Channel-to-Channel Skew vs. Ambient Temperature**



**Figure 28. Logic Input Active Supply Current vs. Logic Input Supply Voltage**



**Figure 29. Logic Input Active Supply Current vs. Ambient Temperature**

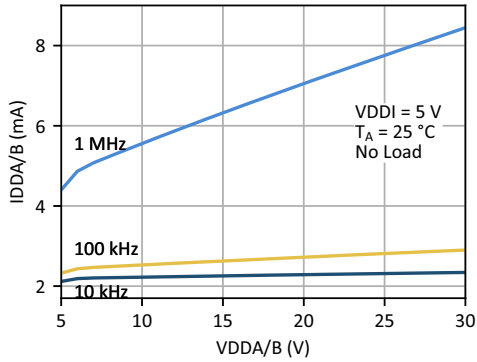


Figure 30. Gate Driver Active Supply Current vs. Gate Driver Supply Voltage

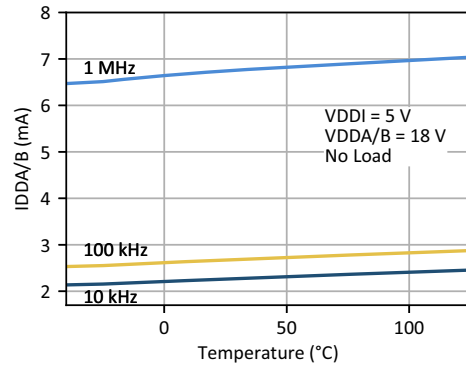


Figure 31. Gate Driver Active Supply Current vs. Ambient Temperature

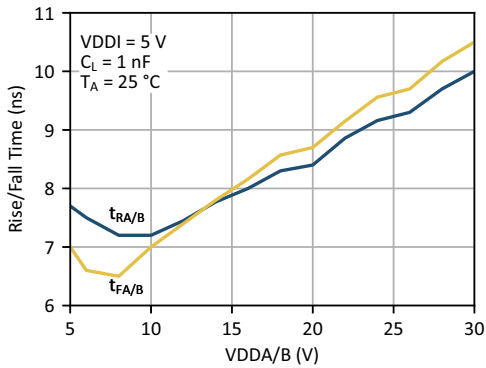


Figure 32. Output Rise/Fall Time vs. Gate Driver Supply Voltage

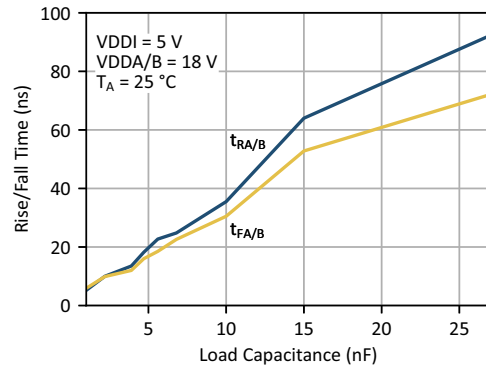


Figure 33. Output Rise/Fall Time vs. Output Load

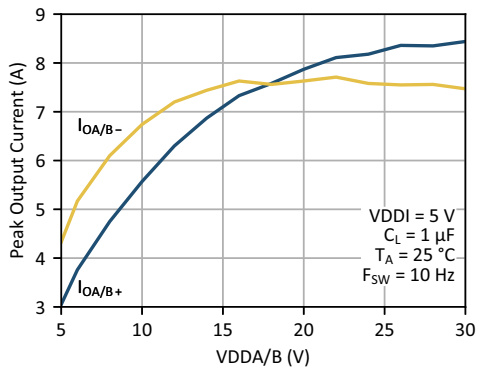


Figure 34. Peak Output Current vs. Gate Driver Supply Voltage

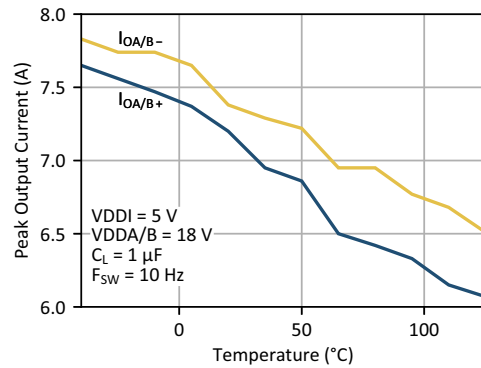
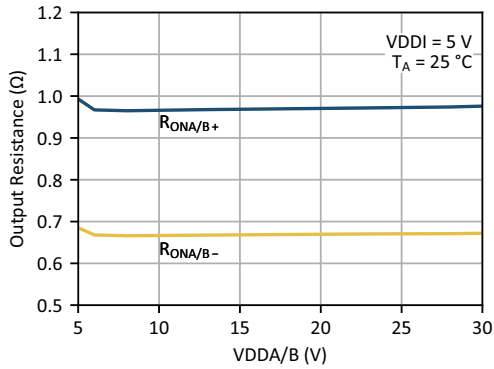
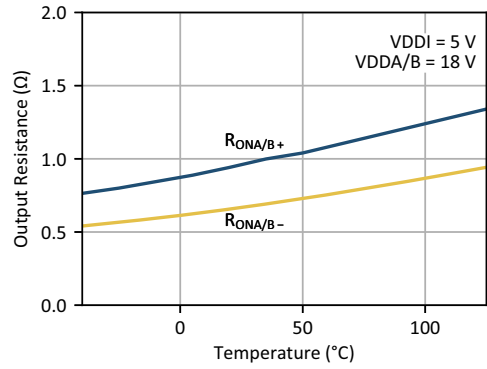


Figure 35. Peak Output Current vs. Ambient Temperature

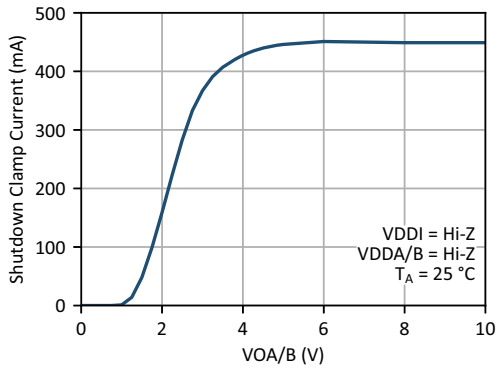




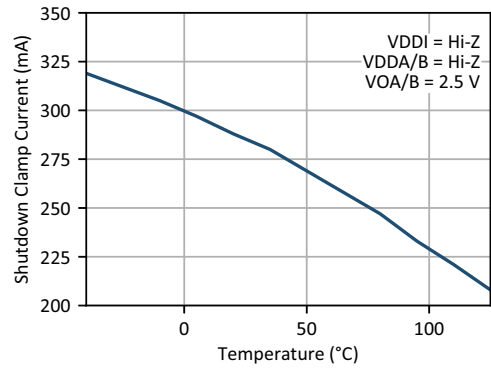
**Figure 36. Output Resistance vs. Gate Driver Supply Voltage**



**Figure 37. Output Resistance vs. Ambient Temperature**



**Figure 38. Shutdown Clamp Current vs. Shutdown Clamp Voltage**



**Figure 39. Shutdown Clamp Current vs. Ambient Temperature**

### 6.4. Thermal Characteristics

Table 9. Thermal Characteristics

Parameter	Symbol	Test Condition	NB SOIC-16	WB SOIC-14	Unit
<b>Thermal Resistance</b>					
Junction-to-Ambient	$\theta_{JA}$	4-layer, 2s2p JEDEC test board	63	59	°C/W
<b>Characterization Parameter</b>					
Junction-to-Top	$\Psi_{JT}$	4-layer, 2s2p JEDEC test board	7.5	14	°C/W
Junction-to-Board	$\Psi_{JB}$	4-layer, 2s2p JEDEC test board	31	34	°C/W

### 6.5. Safety Certifications and Specifications

**Table 10. Regulatory Information<sup>1</sup>**

<b>CSA</b>
The Si82Ex is certified under CSA. For more details, see Master Contract Number 232873.
62368-1: Up to 600 V <sub>RMS</sub> reinforced insulation working voltage; up to 1000 V <sub>RMS</sub> basic insulation working voltage.
60601-1: Up to 250 V <sub>RMS</sub> working voltage and two means of patient protection (MOPP).
<b>VDE</b>
The Si82Ex is certified under VDE. For more details, see File 5028467.
60747-17: Up to 2121 V <sub>PEAK</sub> for reinforced insulation working voltage.
<b>UL</b>
The Si82Ex is certified under UL1577 component recognition program. For more details, see File E257455.
Rated up to 6.0 kV <sub>RMS</sub> V <sub>ISO</sub> isolation voltage for basic protection.
<b>CQC</b>
The Si82Ex is certified under GB4943.1.
Rated up to 250 V <sub>RMS</sub> reinforced insulation working voltage at 5000 meters tropical climate.

1. For more information, see “10. Ordering Guide” on page 46.

**Table 11. Insulation and Safety-Related Specifications**

Parameter	Symbol	Test Condition	Value		Unit
			NB SOIC-16	WB SOIC-14	
Nominal External Air Gap (Clearance)	CLR		3.90	8.00	mm
Nominal External Tracking (Creepage)	CRP		3.90	8.00	mm
Minimum Internal Gap (Internal Clearance)	DTI		0.036	0.036	mm
Tracking Resistance	CTI or PTI	IEC60112	600	600	V <sub>RMS</sub>
Erosion Depth	ED		0.031	0.019	mm
Resistance (Input-Output) <sup>1</sup>	R <sub>IO</sub>	Test voltage = 500 V, 25 °C	10 <sup>12</sup>	10 <sup>12</sup>	Ω
Capacitance (Input-Output) <sup>1</sup>	C <sub>IO</sub>	f = 1 MHz	1.10	1.00	pF
Input Capacitance <sup>2</sup>	C <sub>I</sub>	f = 100 kHz	2.00	2.00	pF

1. To determine resistance and capacitance, the device is converted into a 2-terminal device. Pins on Side A are shorted together to form the first terminal, and pins on Side B are shorted together to form the second terminal. The parameters are then measured between these two terminals.  
 2. Measured from input pin to ground.

Table 12. IEC-60664-1 Ratings

Parameter	Test Conditions	Specification	
		NB SOIC-16	WB SOIC-14
Material group		I	I
Overvoltage category	Rated mains voltage $\leq 150 V_{RMS}$	I-IV	I-IV
	Rated mains voltage $\leq 300 V_{RMS}$	I-III	I-IV
	Rated mains voltage $\leq 600 V_{RMS}$	I-II	I-IV
	Rated mains voltage $\leq 1000 V_{RMS}$	I	I-III

Table 13. IEC60747-17 Insulation Characteristics<sup>1</sup>

Parameter	Symbol	Test Condition	Characteristic		Unit
			NB SOIC-16	WB SOIC-14	
Maximum working isolation voltage	$V_{IOWM}$	According to Time-Dependent Dielectric Breakdown (TDDB) Test	445	1500	$V_{RMS}$
Maximum repetitive isolation voltage	$V_{IORM}$	According to Time-Dependent Dielectric Breakdown (TDDB) Test	630	2121	$V_{PEAK}$
Apparent charge	$Q_{PD}$	Method b: At routine test (100% production) and preconditioning (type test); $V_{INI} = 1.2 \times V_{IOTM}$ , $t_{INI} = 1$ s; $V_{PD(M)} = 1.875 \times V_{IORM}$ , $t_M = 1$ s (method b1) or $V_{PD(M)} = V_{INI}$ , $t_M = t_{INI}$ (method b2)	$\leq 5$	$\leq 5$	pC
Maximum transient isolation voltage	$V_{IOTM}$	$V_{TEST} = V_{IOTM}$ , $t = 60$ s (qualification); $V_{TEST} = 1.2 \times V_{IOTM}$ , $t = 1$ s (100% production)	5302	8484	$V_{PEAK}$
Maximum surge isolation voltage	$V_{IOSM}$	Tested in oil with $1.3 \times V_{IMP}$ or 10 kV minimum and 1.2 $\mu$ s/50 $\mu$ s profile (qualification)	10400	10400	$V_{PEAK}$
Maximum impulse voltage	$V_{IMP}$	Tested in air with 1.2 $\mu$ s/50 $\mu$ s profile (qualification)	5000	8000	$V_{PEAK}$
Isolation resistance	$R_{IO\_S}$	$T_{AMB} = T_S$ , $V_{IO} = 500$ V	$>10^9$	$>10^9$	$\Omega$
Pollution degree			2	2	
Climatic category			40/125/21	40/125/21	

1. This coupler is suitable for “safe electrical insulation” only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.

Table 14. UL1577 Insulation Characteristics

Parameter	Symbol	Test Condition	Characteristic		Unit
			NB SOIC-16	WB SOIC-14	
Maximum withstanding isolation voltage	$V_{ISO}$	$V_{TEST} = V_{ISO}$ , $t = 60$ s (qualification); $V_{TEST} = 1.2 \times V_{ISO}$ , $t = 1$ s (100% production)	3750	6000	$V_{RMS}$

Table 15. IEC Safety Limiting Values

Parameter	Symbol	Test Condition	Max <sup>1</sup>		Unit
			NB SOIC-16	WB SOIC-14	
Safety Temperature	T <sub>S</sub>		150	150	°C
Safety Input, Output, or Supply Current	I <sub>S</sub>	Refer to $\phi_{JA}$ in "6.4. Thermal Characteristics" on page 34; VDDI = 5 V, VDDA/B = 30 V, T <sub>J</sub> = 150 °C, T <sub>A</sub> = 25 °C	66	70	mA
Safety Input, Output, or Total Power	P <sub>S</sub>		1.98	2.11	W

1. Maximum value allowed in the event of a failure; also see the temperature derating curves below.

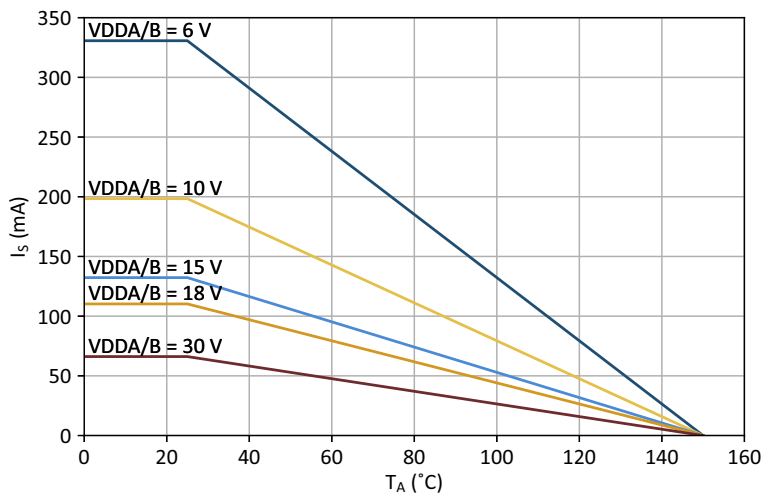


Figure 40. NB SOIC-16 Safety Current vs. Ambient Temperature Derating Curve

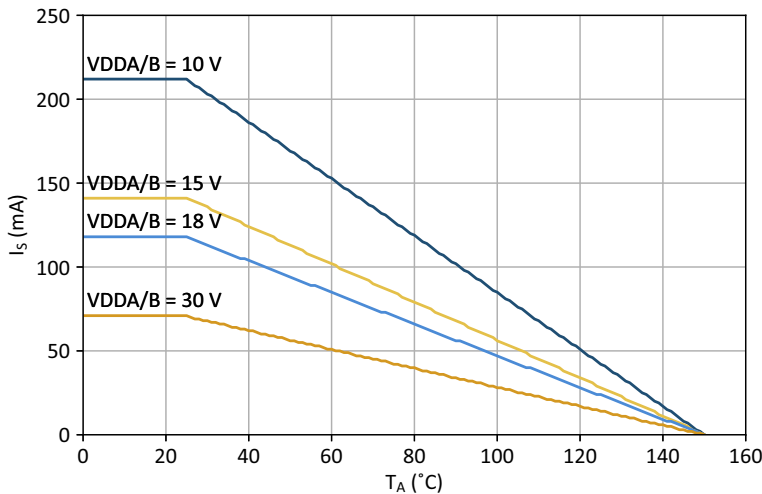


Figure 41. WB SOIC-14 Safety Current vs. Ambient Temperature Derating Curve

## 7. Package Drawings

### 7.1. NB SOIC-16 Package Drawing

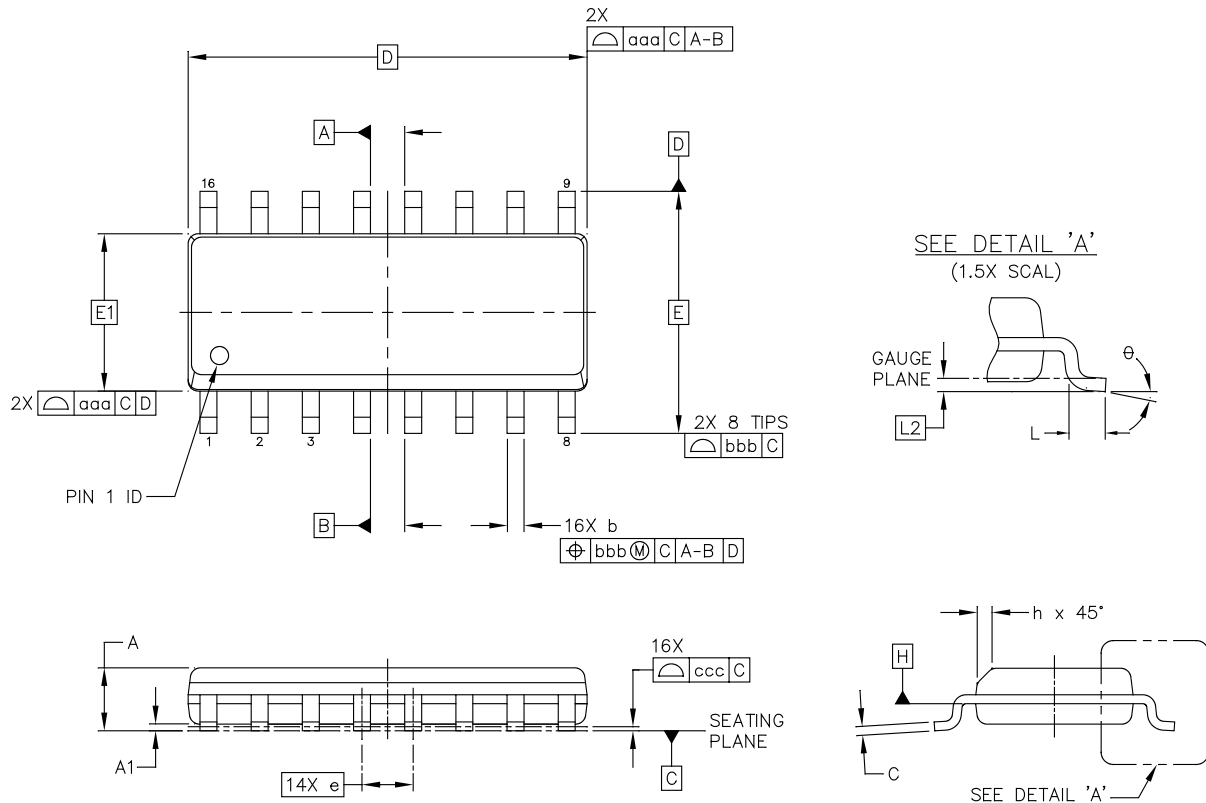


Figure 42. NB SOIC-16 Package Drawing

Table 16. NB SOIC-16 Package Drawing Dimensions<sup>1,2,3,4</sup>

Dimension	Min	Max
A	—	1.75
A1	0.10	0.25
b	0.31	0.51
c	0.17	0.25
D	9.90 BSC	
E	6.00 BSC	
E1	3.90 BSC	
e	1.27 BSC	
L	0.40	1.27
L2	0.25 BSC	
h	0.25	0.50
θ	0°	8°

Table 16. NB SOIC-16 Package Drawing Dimensions<sup>1,2,3,4</sup> (Continued)

Dimension	Min	Max
aaa	0.10	
bbb	0.20	
ccc	0.10	
ddd	0.25	

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MS-012, Variation AC.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

7.2. WB SOIC-14 Package Drawing

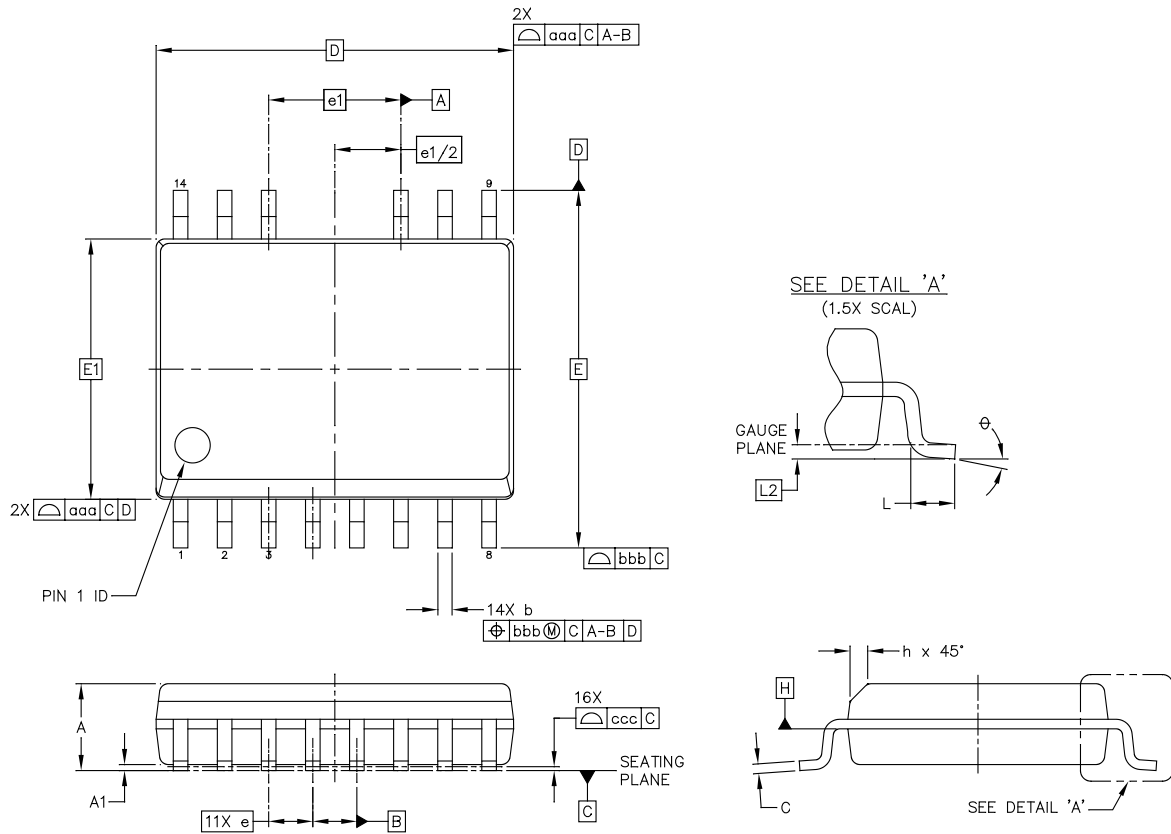


Figure 43. WB SOIC-14 Package Drawing

Table 17. WB SOIC-14 Package Drawing Dimensions<sup>1,2,3</sup>

Dimension	Min	Max
A	—	2.65
A1	0.10	0.30
b	0.35	0.49
c	0.23	0.32
D	10.30 BSC	
E	10.30 BSC	
E1	7.50 BSC	
e	1.27 BSC	
e1	3.81 BSC	
L	0.40	1.27
L2	0.25 BSC	
h	0.25	0.75
θ	0°	8°



Table 17. WB SOIC-14 Package Drawing Dimensions<sup>1,2,3</sup> (Continued)

Dimension	Min	Max
aaa		0.10
bbb		0.25
ccc		0.10
ddd		0.25

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. Recommended reflow profile per the JEDEC J-STD-020C specification for small body, lead-free components.

## 8. Land Patterns

### 8.1. NB SOIC-16 Land Pattern

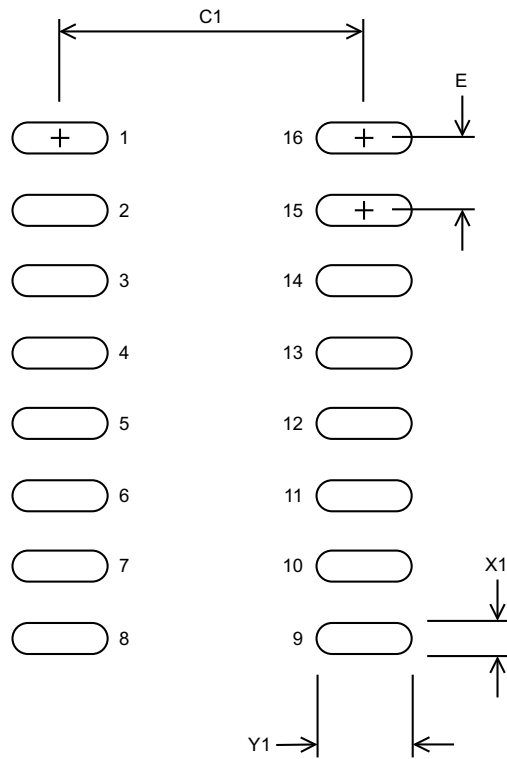


Figure 44. NB SOIC-16 Land Pattern

Table 18. NB SOIC-16 PCB Land Pattern Dimension<sup>1,2</sup>

Dimension	Feature	mm
C1	Pad Column Spacing	5.40
E	Pad Row Pitch	1.27
X1	Pad Width	0.60
Y1	Pad Length	1.55

1. This Land Pattern Design is based on IPC-7351 pattern SOIC127P600X165-16N for Density Level B (Median Land Protrusion).  
 2. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.

8.2. WB SOIC-14 Land Pattern

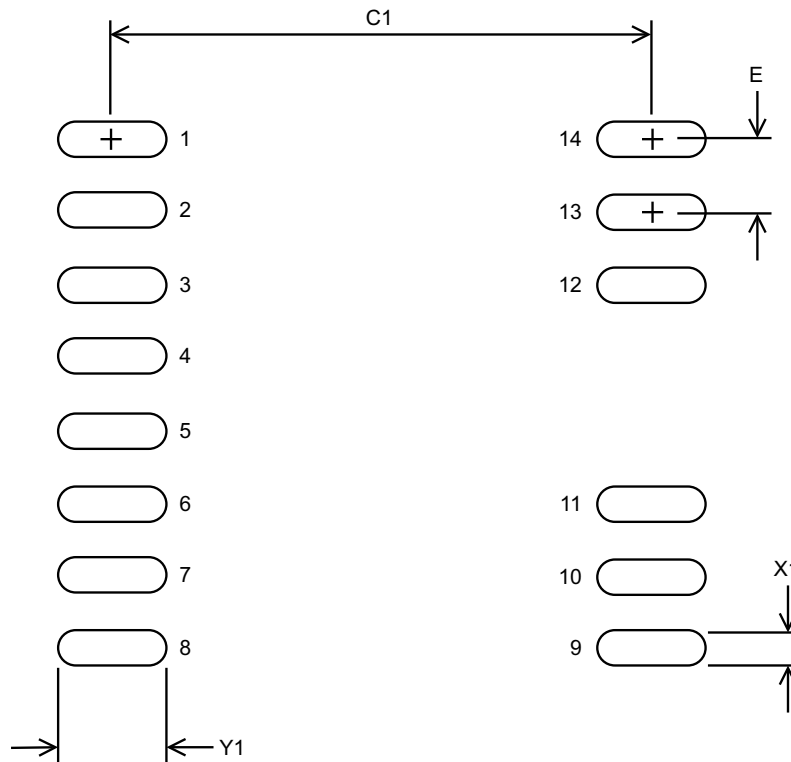


Figure 45. WB SOIC-14 PCB Land Pattern

Table 19. WB SOIC-14 PCB Land Pattern Dimensions<sup>1,2</sup>

Dimension	Feature	mm
C1	Pad Column Spacing	9.80
E	Pad Row Pitch	1.27
X1	Pad Width	0.60
Y1	Pad Length	1.60

1. This Land Pattern Design is based on IPC-7351 pattern SOIC127P1032X265-16AN for Density Level B (Median Land Protrusion).  
 2. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.

## 9. Top Markings

### 9.1. NB SOIC-16 Top Marking

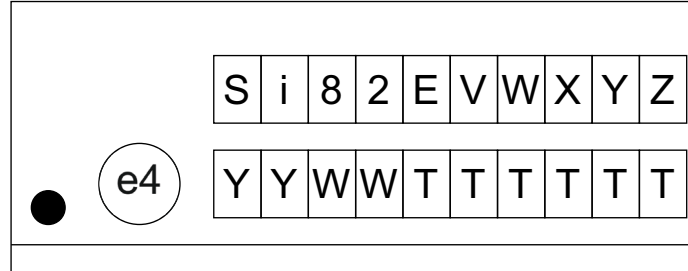


Figure 46. 16-Pin Narrow-Body SOIC Top Marking

Table 20. 16-Pin Narrow-Body SOIC Top Marking Explanation

<p><b>Line 1 Marking:</b></p>	<p>Base Part Number Ordering Options (See “10. Ordering Guide” on page 46 for more information)</p>	<p>Si82E = Two-channel Value IsoDriver product series</p> <p>V = Input Pinout</p> <p>2 = VIA, VIB, DT and DIS inputs (Universal configuration)</p> <p>3 = VIA, VIB, DT and EN inputs (Universal configuration)</p> <p>8 = PWM, DT, and DIS inputs (High-Side/Low-Side configuration)</p> <p>9 = PWM, DT, and EN inputs (High-Side/Low-Side configuration)</p> <p>W = Output Pinout</p> <p>9 = Combined Source/Sink Driver Output</p> <p>X = Input Configuration</p> <p>A = No deglitch filter</p> <p>B = 30 ns deglitch filter</p> <p>Y = Output Configuration</p> <p>G = 4 V UVLO</p> <p>B = 8 V UVLO</p> <p>C = 12 V UVLO</p> <p>E = 15 V UVLO</p> <p>Z = Isolation Rating</p> <p>C = 3.75 kV<sub>RMS</sub></p>
<p><b>Line 2 Marking:</b></p>	<p>YY = Year</p> <p>WW = Workweek</p> <p>TTTTT = Mfg. Trace Code</p> <p>e4 circle is 1.3 mm diameter</p>	<p>Assigned by the assembly house. Corresponds to the year and workweek of the mold date.</p> <p>Manufacturing Traceability Code The Manufacturing Traceability Code represented by “TTTTTT” contains, as its first character, a letter in the range A through M to indicate Industrial-Grade, or a letter in the range N through Z to indicate Automotive-Grade.</p> <p>The “e4” symbol indicates Pb-free lead finish.</p>

9.2. WB SOIC-14 Top Marking

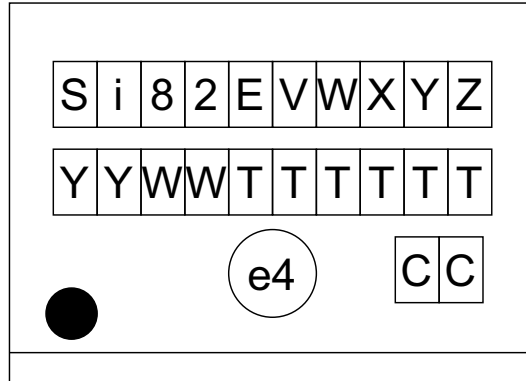


Figure 47. 14-Pin Wide Body SOIC Top Marking

Table 21. 14-Pin Wide Body SOIC Top Marking Explanation

<p><b>Line 1 Marking:</b></p>	<p>Base Part Number Ordering Options (See “10. Ordering Guide” on page 46 for more information)</p>	<p>Si82E = Two-channel Value IsoDriver product series</p> <p>V = Input Pinout</p> <p>2 = VIA, VIB, DT and DIS inputs (Universal configuration)</p> <p>3 = VIA, VIB, DT and EN inputs (Universal configuration)</p> <p>8 = PWM, DT, and DIS inputs (High-Side/Low-Side configuration)</p> <p>9 = PWM, DT, and EN inputs (High-Side/Low-Side configuration)</p> <p>W = Output Pinout</p> <p>9 = Combined Source/Sink Driver Output</p> <p>X = Input Configuration</p> <p>A = No deglitch filter</p> <p>B = 30 ns deglitch filter</p> <p>Y = Output Configuration</p> <p>B = 8 V UVLO</p> <p>C = 12 V UVLO</p> <p>E = 15 V UVLO</p> <p>Z = Isolation Rating</p> <p>E = 6.0 kV<sub>RMS</sub></p>
<p><b>Line 2 Marking:</b></p>	<p>YY = Year WW = Workweek</p>	<p>Assigned by the assembly house. Corresponds to the year and workweek of the mold date.</p>
<p><b>Line 2 Marking:</b></p>	<p>TTTTTT = Mfg. Trace Code</p>	<p>Manufacturing Traceability Code The Manufacturing Traceability Code represented by “TTTTTT” contains, as its first character, a letter in the range A through M to indicate Industrial-Grade, or a letter in the range N through Z to indicate Automotive-Grade.</p>
<p><b>Line 3 Marking:</b></p>	<p>e4 circle is 1.7 mm diameter</p>	<p>The “e4” symbol indicates Pb-free lead finish.</p>
	<p>CC = Country of Origin ISO Code Abbreviation</p>	<p>TW = Taiwan TH = Thailand</p>

### 10. Ordering Guide

Table 22. Si82Ex Ordering Guide<sup>1,2,3,4,5,6</sup>

Ordering Part Number (OPN)	Automotive OPN	Inputs	Configuration	Enable/Disable	Deglintch Filter	Undervoltage Lockout (UVLO)	Isolation Rating	Package Type
<b>NB SOIC-16 Package Options</b>								
Si82E29AGC-IS1	Si82E29AGC-AS1	VIA, VIB	Universal	Disable	NA	4 V	3.75 kV <sub>RMS</sub>	NB SOIC-16
Si82E29ABC-IS1	Si82E29ABC-AS1	VIA, VIB	Universal	Disable	NA	8 V	3.75 kV <sub>RMS</sub>	NB SOIC-16
Si82E29ACC-IS1	Si82E29ACC-AS1	VIA, VIB	Universal	Disable	NA	12 V	3.75 kV <sub>RMS</sub>	NB SOIC-16
Si82E29AEC-IS1	Si82E29AEC-AS1	VIA, VIB	Universal	Disable	NA	15 V	3.75 kV <sub>RMS</sub>	NB SOIC-16
Si82E39AGC-IS1	Si82E39AGC-AS1	VIA, VIB	Universal	Enable	NA	4 V	3.75 kV <sub>RMS</sub>	NB SOIC-16
Si82E39ABC-IS1	Si82E39ABC-AS1	VIA, VIB	Universal	Enable	NA	8 V	3.75 kV <sub>RMS</sub>	NB SOIC-16
Si82E39ACC-IS1	Si82E39ACC-AS1	VIA, VIB	Universal	Enable	NA	12 V	3.75 kV <sub>RMS</sub>	NB SOIC-16
Si82E39AEC-IS1	Si82E39AEC-AS1	VIA, VIB	Universal	Enable	NA	15 V	3.75 kV <sub>RMS</sub> <sup>S</sup>	NB SOIC-16
Si82E39BGC-IS1	Si82E39BGC-AS1	VIA, VIB	Universal	Enable	30 ns	4 V	3.75 kV <sub>RMS</sub>	NB SOIC-16
Si82E39BBC-IS1	Si82E39BBC-AS1	VIA, VIB	Universal	Enable	30 ns	8 V	3.75 kV <sub>RMS</sub>	NB SOIC-16
Si82E39BCC-IS1	Si82E39BCC-AS1	VIA, VIB	Universal	Enable	30 ns	12 V	3.75 kV <sub>RMS</sub>	NB SOIC-16
Si82E39BEC-IS1	Si82E39BEC-AS1	VIA, VIB	Universal	Enable	30 ns	15 V	3.75 kV <sub>RMS</sub>	NB SOIC-16
Si82E89AGC-IS1	Si82E89AGC-AS1	PWM	High-Side/ Low-Side	Disable	NA	4 V	3.75 kV <sub>RMS</sub>	NB SOIC-16
Si82E89ABC-IS1	Si82E89ABC-AS1	PWM	High-Side/ Low-Side	Disable	NA	8 V	3.75 kV <sub>RMS</sub>	NB SOIC-16
Si82E89ACC-IS1	Si82E89ACC-AS1	PWM	High-Side/ Low-Side	Disable	NA	12 V	3.75 kV <sub>RMS</sub>	NB SOIC-16
Si82E89AEC-IS1	Si82E89AEC-AS1	PWM	High-Side/ Low-Side	Disable	NA	15 V	3.75 kV <sub>RMS</sub>	NB SOIC-16
Si82E99AGC-IS1	Si82E99AGC-AS1	PWM	High-Side/ Low-Side	Enable	NA	4 V	3.75 kV <sub>RMS</sub>	NB SOIC-16
Si82E99ABC-IS1	Si82E99ABC-AS1	PWM	High-Side/ Low-Side	Enable	NA	8 V	3.75 kV <sub>RMS</sub>	NB SOIC-16
Si82E99ACC-IS1	Si82E99ACC-AS1	PWM	High-Side/ Low-Side	Enable	NA	12 V	3.75 kV <sub>RMS</sub>	NB SOIC-16
Si82E99AEC-IS1	Si82E99AEC-AS1	PWM	High-Side/ Low-Side	Enable	NA	15 V	3.75 kV <sub>RMS</sub>	NB SOIC-16
Si82E99BGC-IS1	Si82E99BGC-AS1	PWM	High-Side/ Low-Side	Enable	30 ns	4 V	3.75 kV <sub>RMS</sub>	NB SOIC-16
Si82E99BBC-IS1	Si82E99BBC-AS1	PWM	High-Side/ Low-Side	Enable	30 ns	8 V	3.75 kV <sub>RMS</sub>	NB SOIC-16
Si82E99BCC-IS1	Si82E99BCC-AS1	PWM	High-Side/ Low-Side	Enable	30 ns	12 V	3.75 kV <sub>RMS</sub>	NB SOIC-16
Si82E99BEC-IS1	Si82E99BEC-AS1	PWM	High-Side/ Low-Side	Enable	30 ns	15 V	3.75 kV <sub>RMS</sub>	NB SOIC-16

Table 22. Si82Ex Ordering Guide<sup>1,2,3,4,5,6</sup>

Ordering Part Number (OPN)	Automotive OPN	Inputs	Configuration	Enable/Disable	Deglintch Filter	Undervoltage Lockout (UVLO)	Isolation Rating	Package Type
<b>WB SOIC-14 Package Options</b>								
Si82E29ABE-IS3	Si82E29ABE-AS3	VIA, VIB	Universal	Disable	NA	8 V	6 kV <sub>RMS</sub>	WB SOIC-14
Si82E29ACE-IS3	Si82E29ACE-AS3	VIA, VIB	Universal	Disable	NA	12 V	6 kV <sub>RMS</sub>	WB SOIC-14
Si82E29AEE-IS3	Si82E29AEE-AS3	VIA, VIB	Universal	Disable	NA	15 V	6 kV <sub>RMS</sub>	WB SOIC-14
Si82E39ABE-IS3	Si82E39ABE-AS3	VIA, VIB	Universal	Enable	NA	8 V	6 kV <sub>RMS</sub>	WB SOIC-14
Si82E39ACE-IS3	Si82E39ACE-AS3	VIA, VIB	Universal	Enable	NA	12 V	6 kV <sub>RMS</sub>	WB SOIC-14
Si82E39AEE-IS3	Si82E39AEE-AS3	VIA, VIB	Universal	Enable	NA	15 V	6 kV <sub>RMS</sub>	WB SOIC-14
Si82E39BBE-IS3	Si82E39BBE-AS3	VIA, VIB	Universal	Enable	30 ns	8 V	6 kV <sub>RMS</sub>	WB SOIC-14
Si82E39BCE-IS3	Si82E39BCE-AS3	VIA, VIB	Universal	Enable	30 ns	12 V	6 kV <sub>RMS</sub>	WB SOIC-14
Si82E39BEE-IS3	Si82E39BEE-AS3	VIA, VIB	Universal	Enable	30 ns	15 V	6 kV <sub>RMS</sub>	WB SOIC-14
Si82E89ABE-IS3	Si82E89ABE-AS3	PWM	High-Side/ Low-Side	Disable	NA	8 V	6 kV <sub>RMS</sub>	WB SOIC-14
Si82E89ACE-IS3	Si82E89ACE-AS3	PWM	High-Side/ Low-Side	Disable	NA	12 V	6 kV <sub>RMS</sub>	WB SOIC-14
Si82E89AEE-IS3	Si82E89AEE-AS3	PWM	High-Side/ Low-Side	Disable	NA	15 V	6 kV <sub>RMS</sub>	WB SOIC-14
Si82E99ABE-IS3	Si82E99ABE-AS3	PWM	High-Side/ Low-Side	Enable	NA	8 V	6 kV <sub>RMS</sub>	WB SOIC-14
Si82E99ACE-IS3	Si82E99ACE-AS3	PWM	High-Side/ Low-Side	Enable	NA	12 V	6 kV <sub>RMS</sub>	WB SOIC-14
Si82E99AEE-IS3	Si82E99AEE-AS3	PWM	High-Side/ Low-Side	Enable	NA	15 V	6 kV <sub>RMS</sub>	WB SOIC-14
Si82E99BBE-IS3	Si82E99BBE-AS3	PWM	High-Side/ Low-Side	Enable	30 ns	8 V	6 kV <sub>RMS</sub>	WB SOIC-14
Si82E99BCE-IS3	Si82E99BCE-AS3	PWM	High-Side/ Low-Side	Enable	30 ns	12 V	6 kV <sub>RMS</sub>	WB SOIC-14
Si82E99BEE-IS3	Si82E99BEE-AS3	PWM	High-Side/ Low-Side	Enable	30 ns	15 V	6 kV <sub>RMS</sub>	WB SOIC-14

1. "Si" and "SI" are used interchangeably.
2. An "R" at the end of the Ordering Part Number indicates tape and reel packaging option.
3. All packages are RoHS-compliant with peak reflow temperatures of 260 °C according to the JEDEC industry standard classifications and peak solder temperatures.
4. All High-Side/Low-Side drivers have built-in overlap protection while dual drivers do not.
5. Automotive-Grade devices (with an "-A" suffix) are identical in construction materials and electrical parameters to their Industrial Grade (with an "-I" suffix) version counterpart. Automotive-Grade products are produced utilizing full automotive process flows and additional statistical process controls throughout the manufacturing flow. The Automotive-Grade part number is included on shipping labels.
6. In Top Markings, the Manufacturing Code represented by either "RTTTTT" or "TTTTTT" contains as its first character a letter in the range A through M to indicate Industrial-Grade, or N through Z to indicate Automotive-Grade.

## 11. Revision History

Revision	Date	Description	Notes
A	May, 2024	Initial release.	CN0124939



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