

**DATA SHEET**

# SKY12408-321LF: 50-600 MHz, 6 dB 100 Ω Differential Digital Attenuator

**Applications**

- Cellular/3G infrastructure
- IF/RF systems

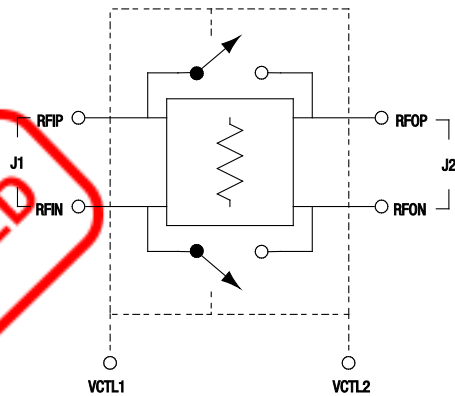
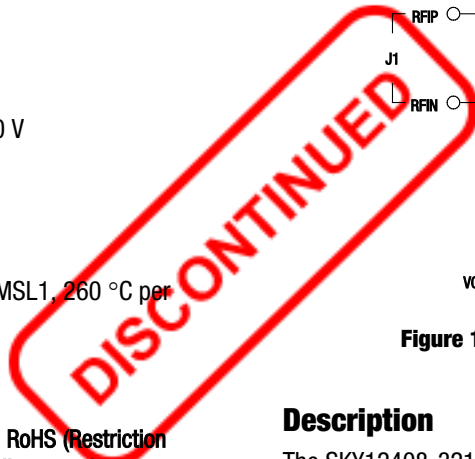
**Features**

- Dual, positive voltage operation: 0/1.8-5.0 V
- High bit accuracy: ±0.3 dB @ 200 MHz
- Low insertion loss: 0.3 dB @ 200 MHz
- Absorptive in 100 Ω differential systems
- Small, QFN (12-pin, 3 x 3 mm) package (MSL1, 260 °C per JEDEC J-STD-020)

**NEW**



Skyworks Green™ products are RoHS (Restriction of Hazardous Substances)-compliant, conform to the EIA/EICTA/JEITA Joint Industry Guide (JIG) Level A guidelines, are halogen free according to IEC-61249-2-21, and contain <1,000 ppm antimony trioxide in polymeric materials.



**Figure 1. SKY12408-321LF Block Diagram**

**Description**

The SKY12408-321LF is a GaAs pHEMT two-bit attenuator I/C. The device is provided in a 3 x 3 mm 12-pin Quad Flat No-Lead (QFN) package.

The SKY12408-321LF is particularly suited for 100 Ω differential systems for which high attenuation accuracy, low insertion loss, and low intermodulation products are required.

The attenuator's differential input and output impedance is 100 Ω. The device is controlled by two positive DC voltage control pins. The differential attenuator paths are controlled together and can be in either an insertion loss or a 6 dB attenuation state. In a differential system, the attenuator presents a 100 Ω impedance, but can be used as two single-ended attenuators, each with a 50 Ω impedance.

A functional block diagram is shown in Figure 1. The pin configuration and package are shown in Figure 2. Signal pin assignments and functional pin descriptions are provided in Table 1.

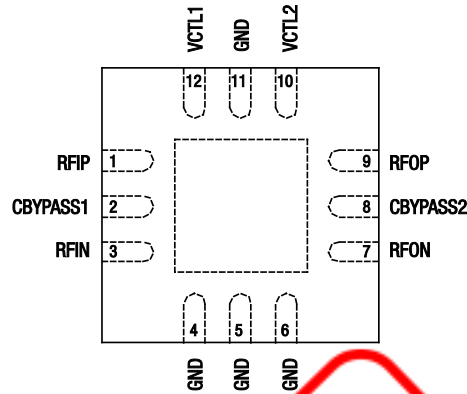


Figure 2. SKY12408-321LF Pinout – 12-Pin QFN (Top View)

Table 1. SKY12408-321LF Signal Descriptions

Pin #	Name	Description	Pin #	Name	Description
1	RFIP	Positive RF input. Comprises J1 along with pin 3. Must be DC blocked from external circuit.	7	RFON	Negative RF output. Comprises J2 along with pin 9. Must be DC blocked from external circuit.
2	CBYPASS1	Must be AC-coupled to external circuit ground.	8	CBYPASS2	Must be AC-coupled to external circuit ground.
3	RFIN	Negative RF input. Comprises J1 along with pin 1. Must be DC blocked from external circuit.	9	RFOP	Positive RF output. Comprises J2 along with pin 7. Must be DC blocked from external circuit.
4	GND	Ground	10	VCTL2	Control voltage input.
5	GND	Ground	11	GND	Ground
6	GND	Ground	12	VCTL1	Control voltage input.

Note: Exposed pad must be grounded.

Table 2. SKY12408-321LF Absolute Maximum Ratings

Parameter	Symbol	Minimum	Maximum	Units
RF input power @ 5 V	P <sub>IN</sub>		+32	dBm
Control voltage	V <sub>CTL</sub>		6	V
Operating temperature	T <sub>OP</sub>	-40	+85	°C
Storage temperature	T <sub>STG</sub>	-65	+150	°C

Note: Exposure to maximum rating conditions for extended periods may reduce device reliability. There is no damage to device with only one parameter set at the limit and all other parameters set at or below their nominal value. Exceeding any of the limits listed here may result in permanent damage to the device.

**CAUTION:** Although this device is designed to be as robust as possible, Electrostatic Discharge (ESD) can damage this device. This device must be protected at all times from ESD. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD precautions should be used at all times.

### Electrical and Mechanical Specifications

The absolute maximum ratings of the SKY12408-321LF are provided in Table 2. Electrical specifications are provided in Table 3.

Typical performance characteristics of the SKY12408-321LF are illustrated in Figures 3 through 6.

The state of the SKY12408-321LF is determined by the logic provided in Table 4.

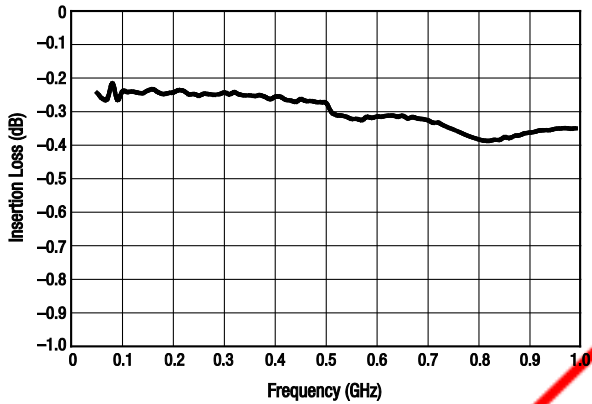
**Table 3. SKY12408-321LF Electrical Specifications (Note 1)****( $V_{CTL} = 0$  to 3 V,  $T_{OP} = +25$  °C,  $P_{IN} = 0$  dBm, Characteristic Impedance [ $Z_0$ ] = 50  $\Omega$  (Single Ended), Unless Otherwise Noted)**

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
Insertion loss	IL	f = 50 to 600 MHz		0.30	0.40	dB
Attenuation (normalized to insertion loss)	Attn	f = 50 to 400 MHz	5.6	6.0	6.4	dB
		f = 400 to 600 MHz	5.5	6.0	6.5	dB
Return loss, insertion loss state	RL_IL	f = 50 to 600 MHz		30		dB
Return loss, attenuation state	RL_AT	f = 50 to 600 MHz		25		dB
Switching speed, on	T <sub>ON</sub>	50% control to 90% RF		36		ns
Switching speed, off	T <sub>OFF</sub>	50% control to 10% RF		36		ns
Switching speed, rise	T <sub>RISE</sub>	10/90% RF		20		ns
Switching speed, fall	T <sub>FALL</sub>	90/10% RF		28		ns
Attenuation settling time	AT <sub>SET</sub>	Attenuation change from 200 ns to 5 ms			0.15	dB
Attenuation phase setting (Note 2)	AT <sub>PS</sub>	Phase change from 200 ns to 5 ms	-2		+2	deg
1 dB Input Compression Point	IP1dB	Insertion loss state, $V_{CTL} = 3.3$ V: f = 50 MHz f = 75 MHz f = 100 MHz		+31		dBm
				+34		dBm
				+34		dBm
0.5 dB Input Compression Point	IP0.5dB	Attenuation state, $V_{CTL} = 3.3$ V: f = 50 MHz f = 75 MHz		+33		dBm
				+33		dBm
3 <sup>rd</sup> Order Input Intercept Point	IIP3	$V_{CTL} = 3.3$ V: f = 50 MHz, insertion loss state, $P_{IN} = +6$ dBm f = 50 MHz, attenuation state, $P_{IN} = +12$ dBm f = 75 MHz, attenuation state, $P_{IN} = +12$ dBm		+46		dBm
				+49		dBm
				+47		dBm
2 <sup>nd</sup> harmonic	2fo	f = 50 MHz, insertion loss state, $P_{IN} = +6$ dBm f = 50 MHz, attenuation state, $P_{IN} = +12$ dBm		-80		dBc
				-70		dBc
3 <sup>rd</sup> harmonic	3fo	f = 50 MHz, insertion loss state, $P_{IN} = +6$ dBm f = 50 MHz, attenuation state, $P_{IN} = +12$ dBm		-98		dBc
				-98		dBc
Control current	I <sub>CTL</sub>	$V_{CTL} = 3$ V		10		$\mu$ A
Control voltage		$V_{CTL} = \text{low}$	0		0.2	V
		$V_{CTL} = \text{high}$	1.8		5.0	V

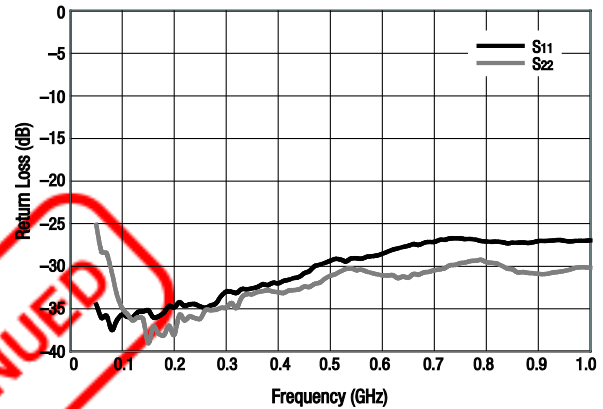
**Note 1:** Performance is guaranteed only under the conditions listed in this Table.**Note 2:** Phase performance guaranteed by design, not measured.

**Typical Performance Characteristics**

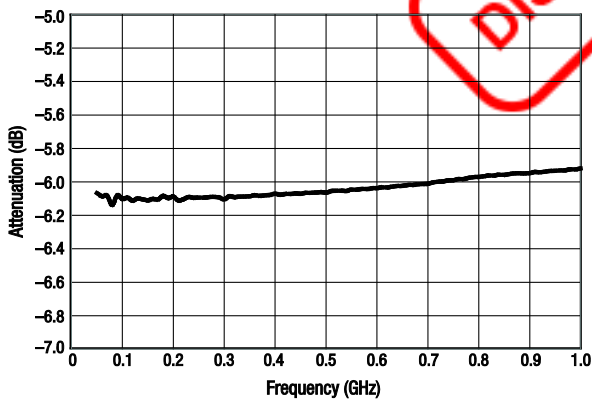
( $C_{BLK} = 1000 \text{ pF}$ ,  $C_{BYPASS} = 1000 \text{ pF}$ ,  $V_{CTL} = 3 \text{ V}$ ,  $T_{OP} = +25 \text{ }^\circ\text{C}$ , Characteristic Impedance [ $Z_0$ ] =  $50 \text{ } \Omega$ , Driven and Measured Single-Ended, Unless Otherwise Noted)



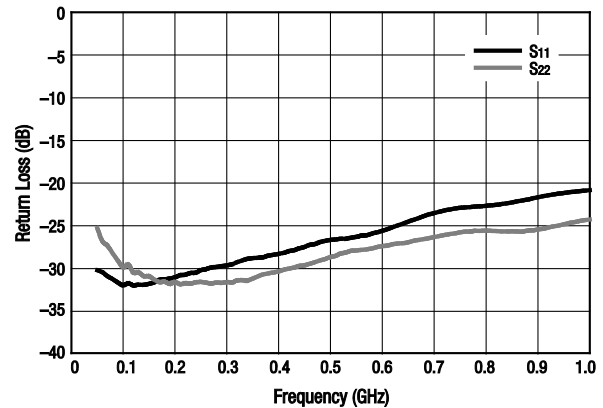
**Figure 3. Typical Insertion Loss**



**Figure 4. Return Loss Insertion State**



**Figure 5. Typical Attenuation (Normalized to Insertion Loss)**



**Figure 6. Return Loss Attenuation State**



**Table 4. SKY12408-321LF Truth Table**

State (J1-J2)	VCTL1	VCTL2
Reference insertion loss	high	low
6 dB attenuation	low	high

**Note:** high = +1.8 to 5.0 V  
 low = 0 V  
 Any state other than described in this Table places the attenuator into an undefined state.

**Evaluation Board Description**

The SKY12408-321LF Evaluation Board is used to test the performance of the SKY12408-321LF digital attenuator. An assembly drawing for the Evaluation Board is shown in Figure 7 and an Evaluation Board schematic diagram is shown in Figure 8. Table 5 provides the Bill of Materials (BOM) list for Evaluation Board components.

**Package Dimensions**

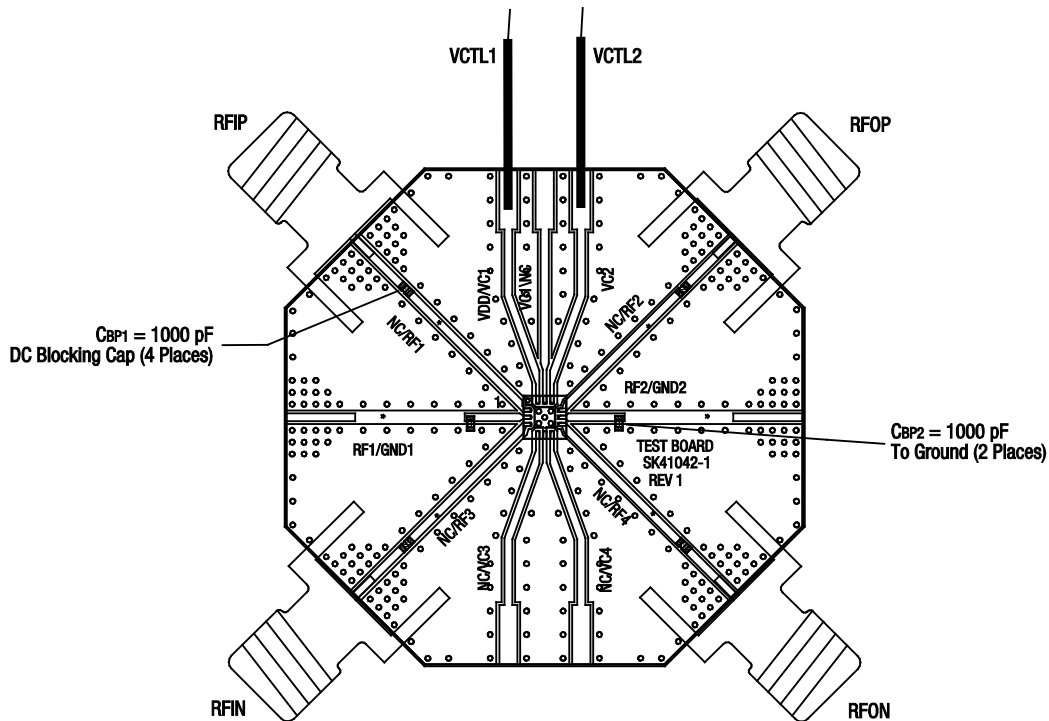
The PCB layout footprint for the SKY12408-321LF is shown in Figure 9. Typical case markings are noted in Figure 10. Package dimensions for the 12-pin QFN are shown in Figure 11, and tape and reel dimensions are provided in Figure 12.

**Package and Handling Information**

Instructions on the shipping container label regarding exposure to moisture after the container seal is broken must be followed. Otherwise, problems related to moisture absorption may occur when the part is subjected to high temperature during solder assembly.

THE SKY12408-321LF is rated to Moisture Sensitivity Level 1 (MSL1) at 260 °C. It can be used for lead or lead-free soldering. For additional information, refer to the Skyworks Application Note, *Solder Reflow Information*, document number 200164.

Care must be taken when attaching this product, whether it is done manually or in a production solder reflow environment. Production quantities of this product are shipped in a standard tape and reel format.



**Figure 7. SKY12408-321LF Evaluation Board Assembly Diagram**

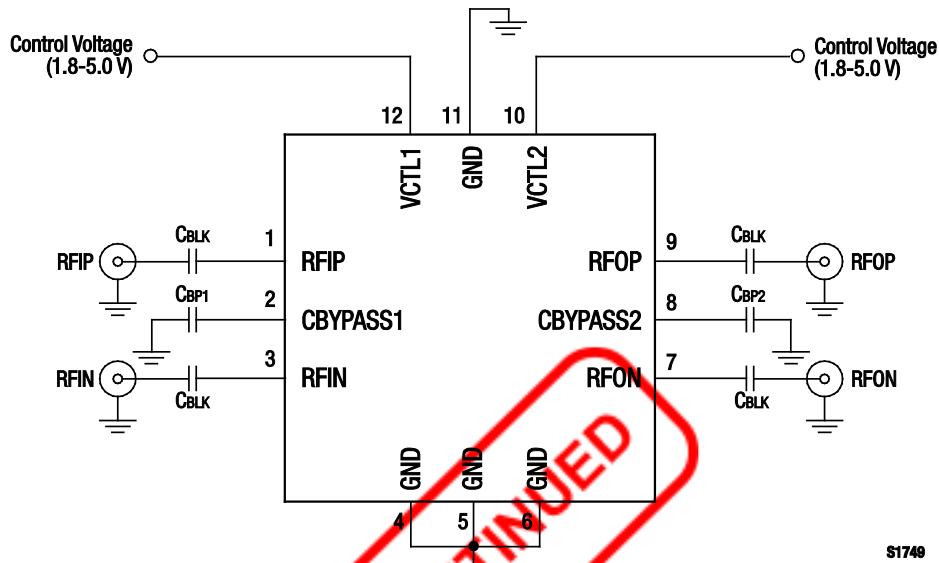


Figure 8. SKY12408-321LF Evaluation Board Schematic Diagram

Table 5. SKY12408-321LF Evaluation Board bill of Materials

Component	Value	Size	Manufacturer/Part Series
CBLK	1000 pF	0402	Murata GRM
CBP1, CBP2	1000 pF	0402	Murata GRM

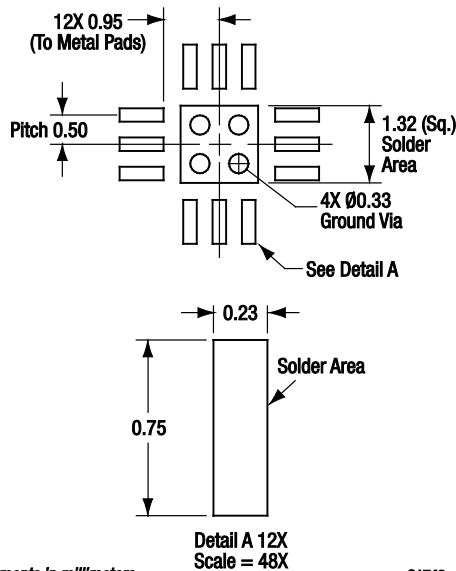


Figure 9. SKY12408-321LF PCB Layout Footprint

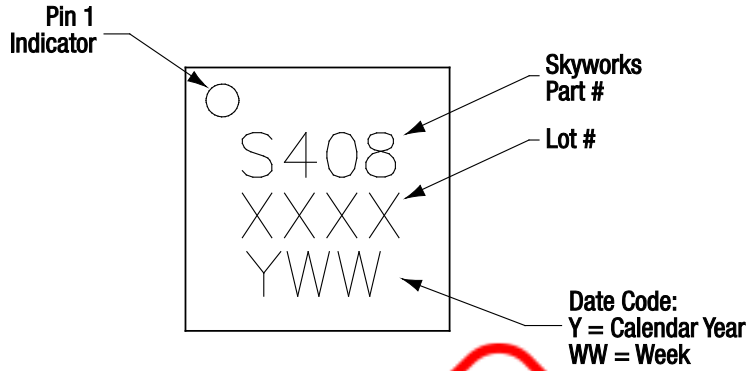
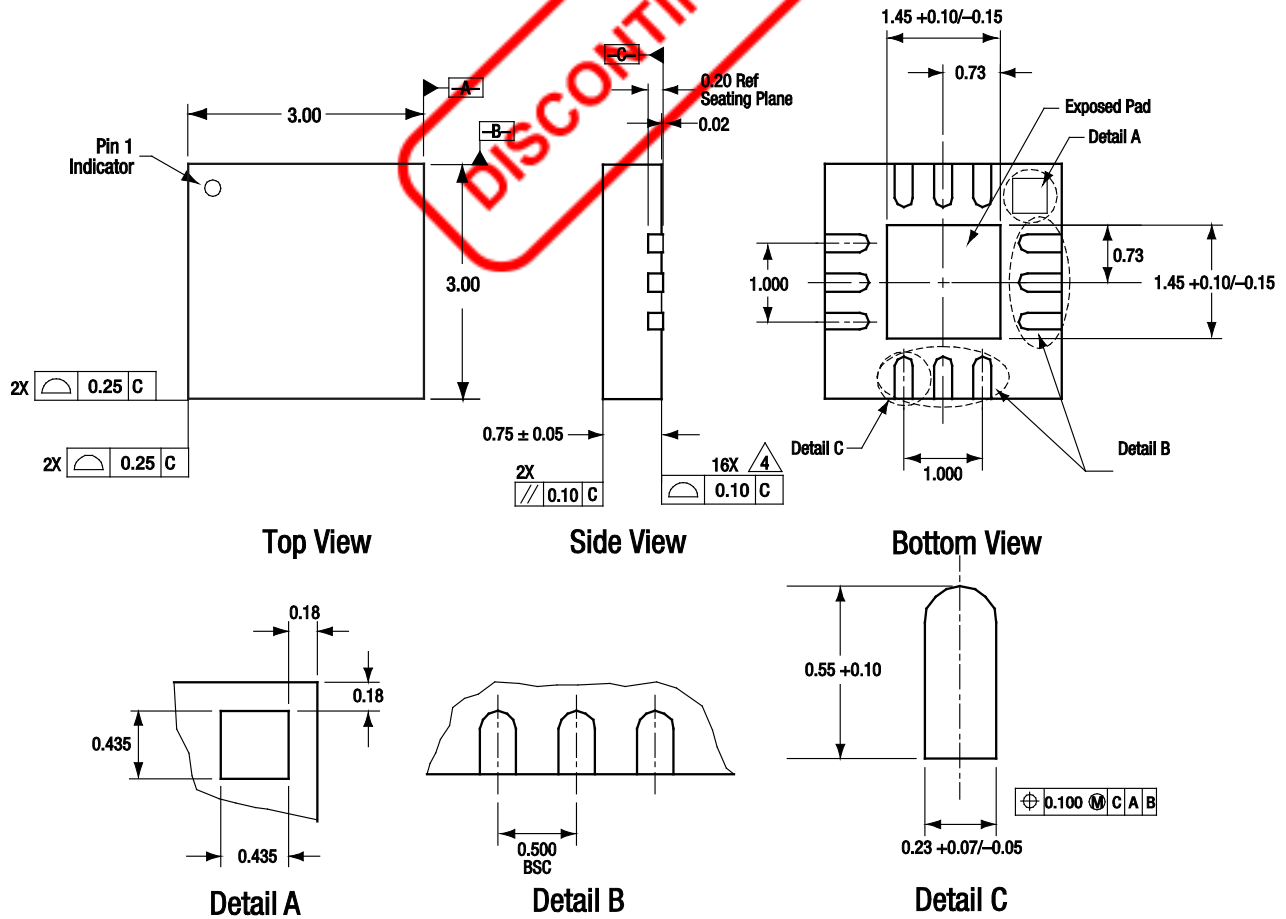


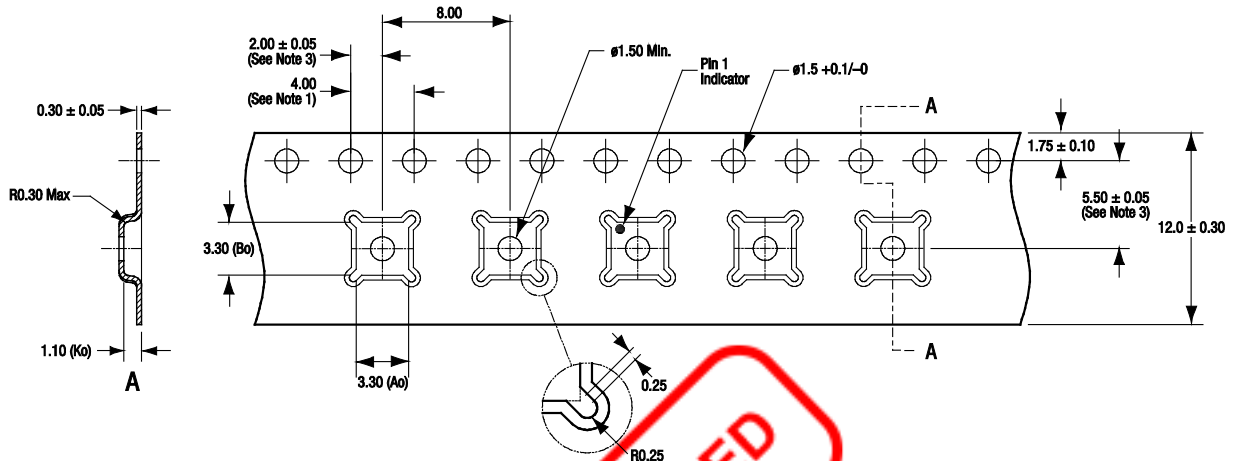
Figure 10. Typical Part Markings (Top View)



All measurements are in millimeters.  
Dimensioning and tolerancing according to ASME Y14.5M-1994.  
Coplanarity applies to the exposed heat sink slug as well as the terminals.  
Plating requirement per source control drawing (SCD) 2504.  
All contact points are Au-plated, Pb-free surfaces.

S1542

Figure 11. SKY12408-321LF 12-Pin QFN Package Dimensions



**Notes:**

1. Sprocket hole pitch cumulative tolerance:  $\pm 0.2$ .
2. Carrier tape: black conductive polystyrene.
3. Pocket position relative to sprocket hole, measure as true position of pocket, not pocket hole.
4. Cover tape material: transparent conductive PSA, 9.30 mm wide.
5. All dimensions are in millimeters.

S2892

Figure 12. SKY12408-321LF Tape and Reel Dimensions



**Ordering Information**

Model Name	Manufacturing Part Number	Evaluation Board Part Numbers
SKY12408-321LF Differential Digital Attenuator	SKY12408-321LF	SKY12408-321LF-EVB



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