

DATA SHEET

SKY13278-313LF: 100 MHz to 2.5 GHz GaAs SPDT Switch

Applications

- Transmit/receive switching for telematic systems at elevated power levels

Features

- Broadband frequency range: 100 MHz to 2.5 GHz
- Very low insertion loss, 0.4 dB typical @ 900 MHz
- High isolation: 26 dB typical @ 900 MHz
- Low current consumption: <100 μ A @ 3 V
- Miniature QFN (6-pin, 2 x 3 mm) package (MSL1, 260 °C per JEDEC J-STD-020)

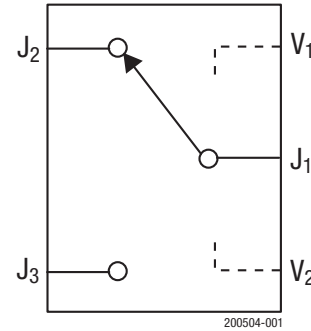


Figure 1. SKY13278-313LF Block Diagram



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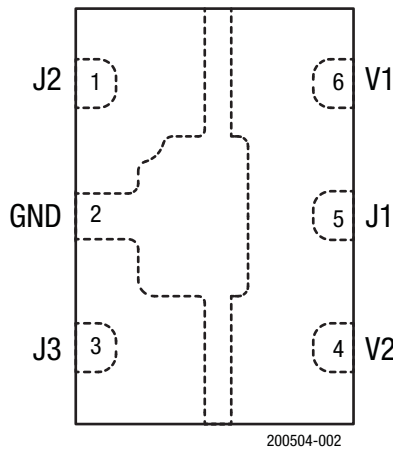


Figure 2. SKY13278-313LF Pinout (Top View)

Description

The SKY13278-313LF is a pHEMT GaAs FET IC high linearity SPDT switch. This wideband switch has been designed for use from 100 MHz to 2.5 GHz, where extremely high linearity, low control voltage, high isolation, low insertion loss and ultra-miniature package size are required. It can be controlled with positive, negative or a combination of both voltages. The RF signal paths within the SKY13278-313LF are fully bilateral.

Some standard implementations include T/R switching and diversity switching over 3 W. The SKY13278-313LF switch can be used in many analog and digital wireless communication systems including cellular, GSM and UMTS applications.

Switching is controlled via two control voltage inputs. Depending upon the voltage level applied to the control voltage pins, the common RF port (J1) is connected to one of two RF ports (J2 or J3) via a low insertion loss path, while the path between J1 and the other RF port is in its isolation state. When the control voltages are toggled, the states between J1 and J2, as well as J1 and J3, are also toggled.

The SKY13278-313LF is available in a lead(Pb)-free, RoHS-compliant, QFN-6 2 x 3 mm plastic package. A functional block diagram is shown in Figure 1. The pin configuration and package are shown in Figure 2. Signal pin assignments and functional pin descriptions are provided in Table 1.

Table 1. SKY13278-313LF Signal Descriptions

Pin	Name	Description	Pin	Name	Description
1	J2	RF input/output. According to the logic voltage levels applied to the V1 and V2 pins, this port is either connected to J1 using a low insertion loss path or isolated from J1. ¹	4	V2	DC control voltage input #2. The logic voltage applied to this pin, along with the voltage level applied to the V1 pin, determines the states of the RF paths between J1/J2 and J1/J3.
2	GND	Ground. Equipotential port, internal circuit common, which must be connected to the PCB ground or common using the lowest possible impedance.	5	J1	RF input/output. According to the logic voltage levels applied to the V1 and V2 pins, this port is either connected to J2 or to J3 using a low insertion loss path and isolated from the other RF port. ¹
3	J3	RF input/output. According to the logic voltage levels applied to the V1 and V2 pins, this port is either connected to J1 using a low insertion loss path or isolated from J1. ¹	6	V1	DC control voltage input #1. The logic voltage applied to this pin, along with the voltage level applied to the V2 pin, determines the states of the RF paths between J1/J2 and J1/J3.

¹ A 47 pF blocking capacitor is required for >500 MHz operation. Use larger value capacitors for lower frequency operation.

Electrical and Mechanical Specifications

The absolute maximum ratings of the SKY13278-313LF are provided in Table 2. Electrical specifications are provided in Table 3 and the operating characteristics are specified in Table 4.

The state of the SKY13278-313LF is determined by the logic provided in Table 5.

Typical performance characteristics of the SKY13278-313LF are illustrated in Figures 3 through 8.

Table 2. SKY13278-313LF Absolute Maximum Ratings¹

Parameter	Symbol	Minimum	Maximum	Units
RF input power @ 5 V	P _{IN}		10 W, f > 900 MHz @ 25 °C	dBm
Control voltage	V _{CTL}		-0.2 < V1, V2 < 8 V	V
Operating temperature	T _{OP}	-40	+85	°C
Storage temperature	T _{STG}	-65	+150	°C
Electrostatic discharge: Human Body Model (HBM), Class 1A			250	V

¹ Exposure to maximum rating conditions for extended periods may reduce device reliability. There is no damage to device with only one parameter set at the limit and all other parameters set at or below their nominal value.

ESD HANDLING: *Although this device is designed to be as robust as possible, electrostatic discharge (ESD) can damage this device. This device must be protected at all times from ESD when handling or transporting. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD handling precautions should be used at all times.*

Table 3. SKY13278-313LF Electrical Specifications¹

($V_{CTL} = 0$ to 3 V, $T_{OP} = +25$ °C, $P_{IN} = 0$ dBm, Characteristic Impedance = 50 Ω , Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Insertion loss		0.1 to 0.5 GHz		0.40	0.5	dB
		0.5 to 1.0 GHz		0.40	0.5	dB
		1.0 to 2.0 GHz		0.45	0.6	dB
		2.0 to 2.5 GHz		0.55	0.7	dB
Isolation		0.1 to 0.5 GHz	29	32		dB
		0.5 to 1.0 GHz	23	26		dB
		1.0 to 2.0 GHz	17	20		dB
		2.0 to 2.5 GHz	15	18		dB
Return loss ²		0.1 to 0.5 GHz		20		dB
		1.0 to 2.0 GHz		20		dB
Switching characteristics:						
Rise/fall		10/90% or 90/10% RF		650		ns
On/off		50% V_{CTL} to 90/10% RF		800		ns
0.1 dB input compression point (900 MHz)	IP0.1dB	@ 900 MHz		+40		dBm
2 nd and 3 rd harmonics		$P_{IN} = 34.5$ dBm, $f_{IN} = 900$ MHz		-75		dBc
2 nd and 3 rd harmonics		$P_{IN} = 32$ dBm, $f_{IN} = 1800$ MHz		-70		dBc
Blocker performance		T1 = 1950 MHz @ +20 dBm T2 = 1760 MHz @ -15 dBm IMD3 measured at 2140 MHz		-105		dBm
Thermal resistance				45		°C/W
Control voltage		$V_{LOW} = 0$ V @ 20 μ A max $V_{HIGH} = 2.8$ V @ 100 μ A max to 5 V @ 200 μ A max				

¹ Performance is guaranteed only under the conditions listed in this table.

² Return loss state. Lower frequency return loss is dependent on value of the DC blocking capacitors.

Table 4. Truth Table (2.8 V \leq $V_{HIGH} \leq$ 5 V, 0 \leq $V_{LOW} \leq$ 0.2 V)

V1	V2	J1-J2	J1-J3
V_{LOW}	V_{HIGH}	Isolation	Insertion loss
V_{HIGH}	V_{LOW}	Insertion loss	Isolation
V_{LOW}	V_{LOW}	Not recommended ¹	
V_{HIGH}	V_{HIGH}	Not recommended ¹	

¹ Switch is in an undefined state.

Typical Performance Characteristics

($V_{CTL} = 0$ to 3 V, $T_{OP} = +25\text{ }^{\circ}\text{C}$, $P_{IN} = 0$ dBm, Characteristic Impedance [Z_0] = 50 Ω , $C_{BL} = 100$ pF, Unless Otherwise Noted)

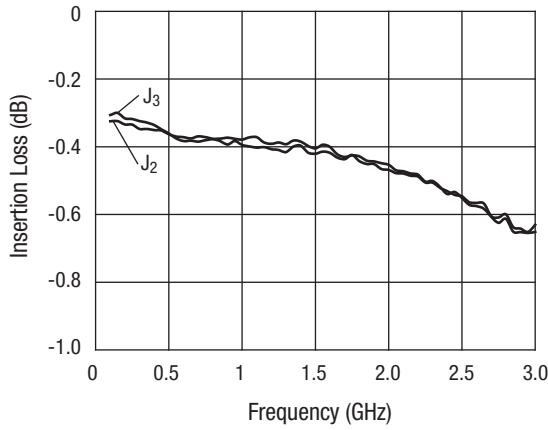


Figure 3. Insertion Loss vs Frequency

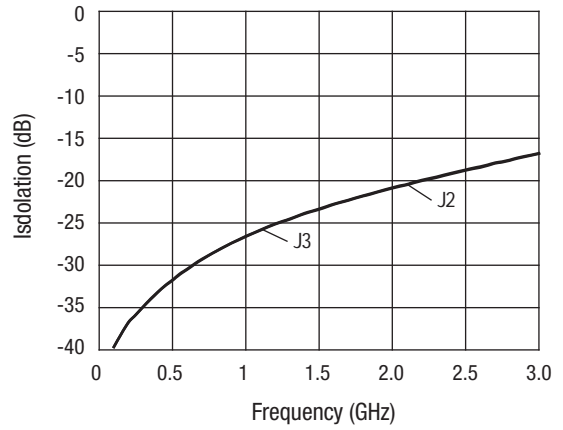


Figure 4. Isolation vs Frequency

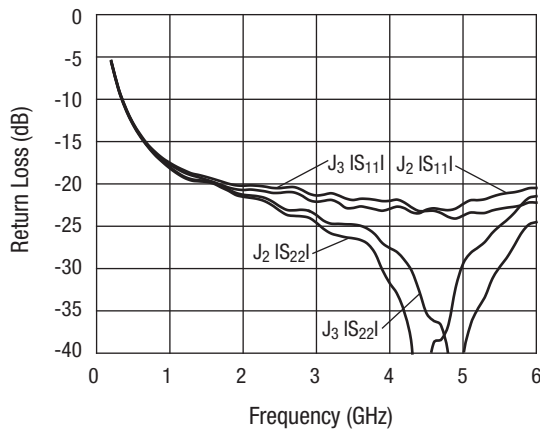


Figure 5. Return Loss vs Frequency

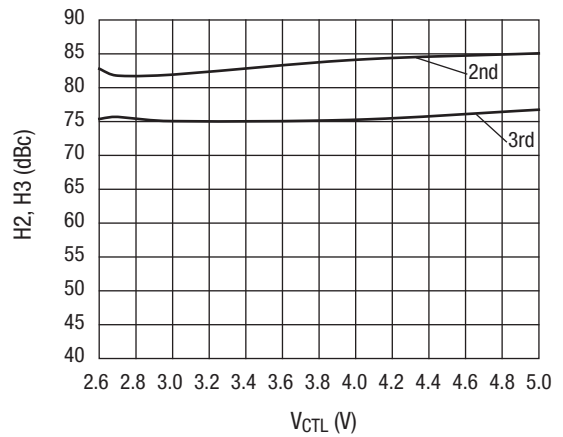


Figure 6. Second and Third Harmonics vs Control Voltage
($F_{IN} = 900$ MHz $P_{IN} = +34.5$ dBm)

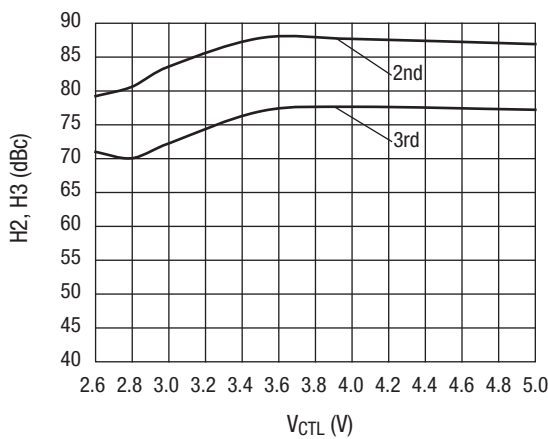


Figure 7. Second and Third Harmonics vs Control Voltage
($F_{IN} = 1800$ MHz $P_{IN} = +32$ dBm)

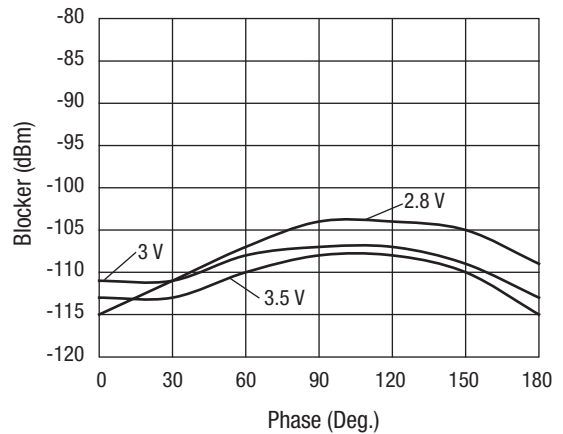


Figure 8. Blocker Performance vs Phase
($f_1 = 1950$ MHz, $P_{IN} = +20$ dBm; $f_2 = 1760$ MHz, $P_{IN} = -15$ dBm, Blocker Measured at 2140 MHz)

Evaluation Board Description

The Evaluation Board for the SKY13278-313 allows the switch to be fully exercised. The RF common port is marked J1, and the two switched RF ports are marked J2 and J3. All of the RF ports have SMA connectors mounted. The control voltage inputs are marked V1 and V2.

The printed circuit board material is FR4. The RF dielectric layer is 0.012 inch thick, ½ oz. copper. The RF transmission lines are each 50 Ω (nominal) microstrip.

There are three DC blocking capacitors on the board (C1, C2, and C3), each of which is in series with one of the RF ports. These capacitors are 47 pF. For improved insertion loss at signal frequencies below approximately 500 MHz these capacitors should be replaced with larger capacitance capacitors, such as 1000 pF.

The Evaluation Board schematic is shown in Figure 9. An assembly diagram of the Evaluation Board is shown in Figure 10.

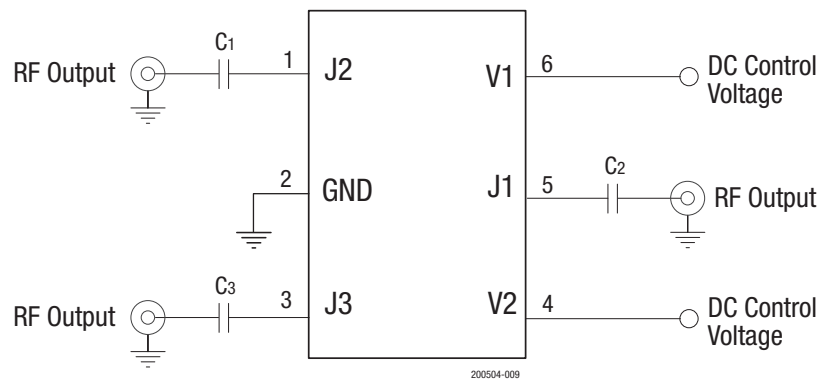
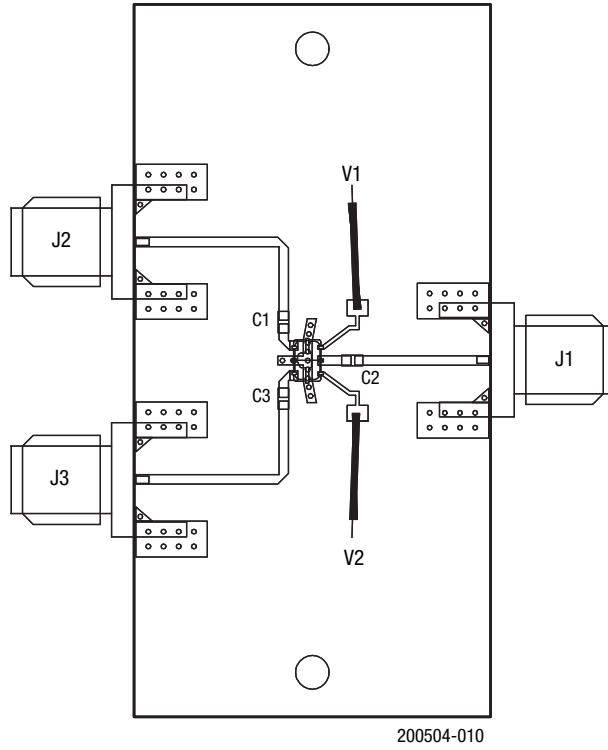


Figure 9. SKY13278-313LF Evaluation Board Schematic



200504-010
Figure 10. SKY13278-313LF Evaluation Board Assembly Diagram

Package Dimensions

The PCB layout footprint for the SKY13278-313LF is shown in Figure 11. Typical part markings are shown in Figure 12. Package dimensions are shown in Figure 13, and tape and reel dimensions are provided in Figure 14.

Package and Handling Information

Instructions on the shipping container label regarding exposure to moisture after the container seal is broken must be followed. Otherwise, problems related to moisture absorption may occur when the part is subjected to high temperature during solder assembly.

The SKY13278-313LF is rated to Moisture Sensitivity Level 1 (MSL1) at 260 °C. It can be used for lead or lead-free soldering.

Care must be taken when attaching this product, whether it is done manually or in a production solder reflow environment. Production quantities of this product are shipped in a standard tape and reel format.

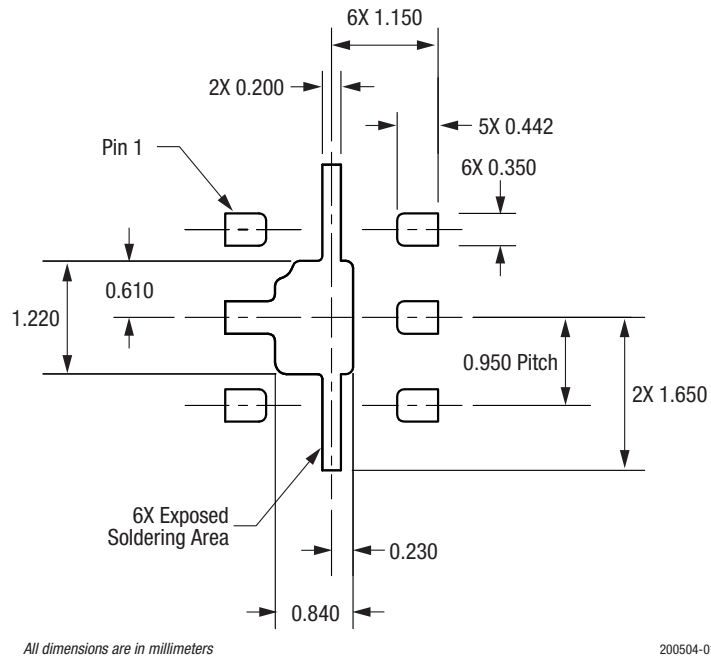


Figure 11. SKY13278-313LF PCB Layout Footprint

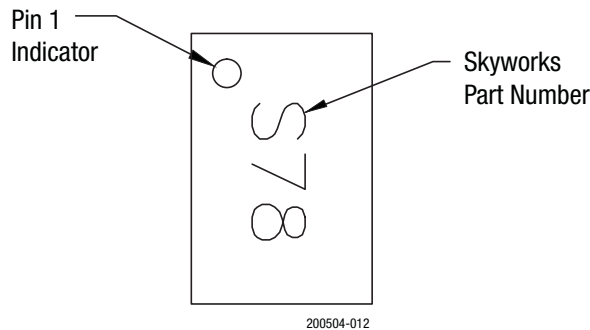
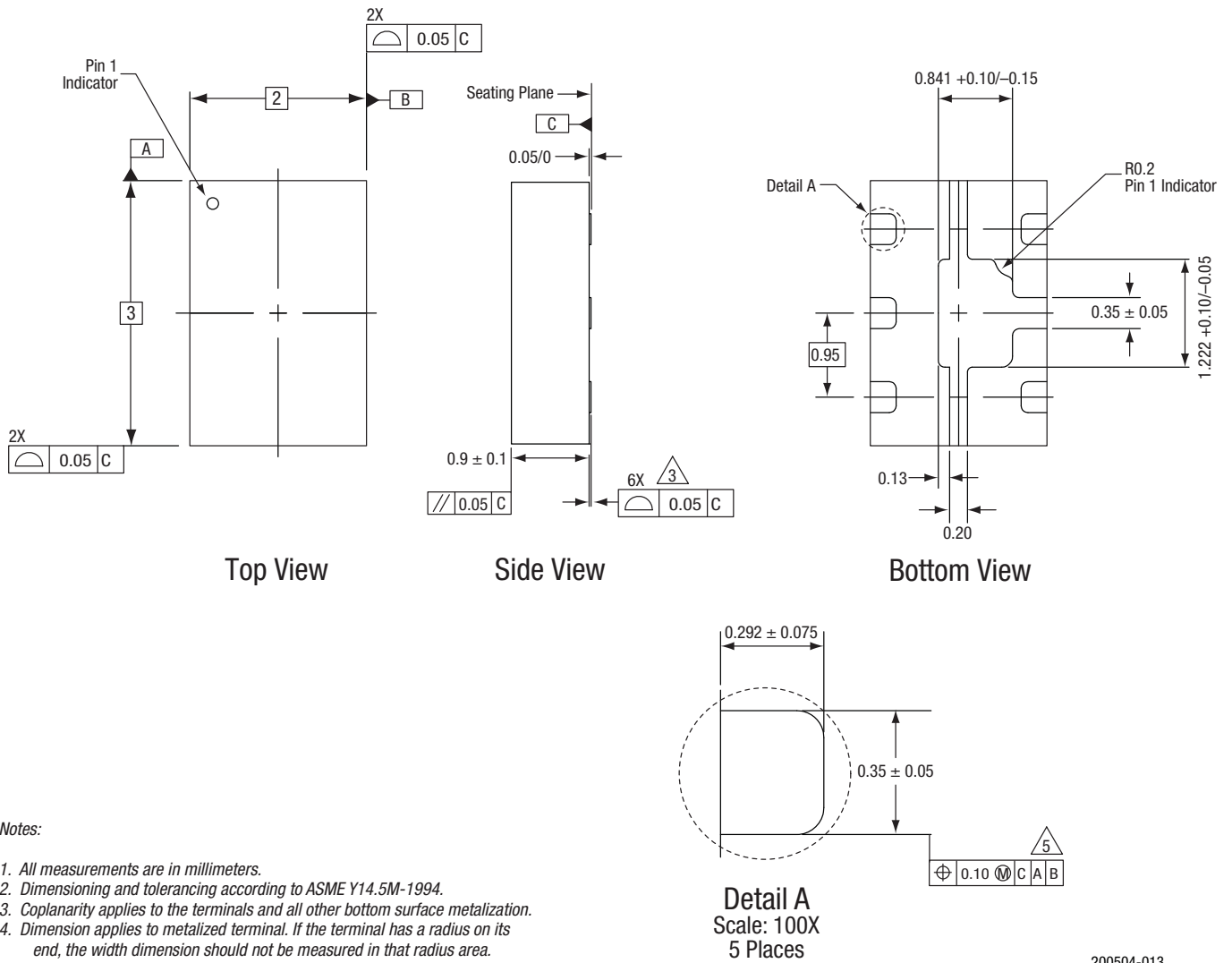


Figure 12. Typical Part Markings (Top View)

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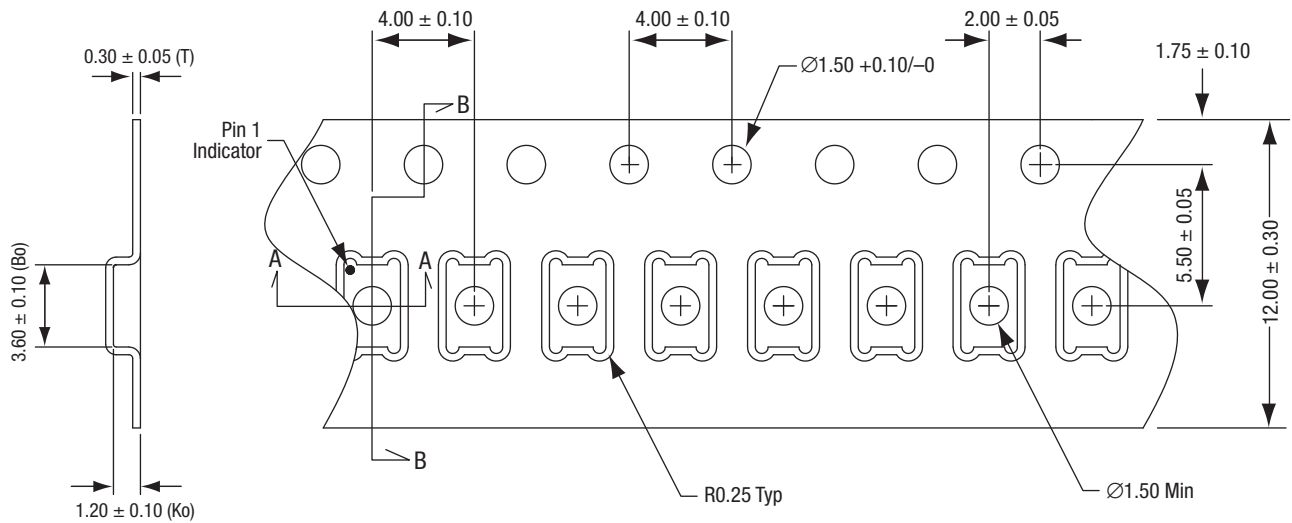


Notes:

1. All measurements are in millimeters.
2. Dimensioning and tolerancing according to ASME Y14.5M-1994.
3. Coplanarity applies to the terminals and all other bottom surface metalization.
4. Dimension applies to metalized terminal. If the terminal has a radius on its end, the width dimension should not be measured in that radius area.

Figure 13. SKY13278-313LF Package Dimensions

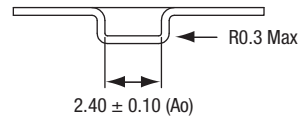
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Detail B

Notes:

1. Carrier tape: black conductive polystyrene, non-bakeable material.
2. Cover tape material: transparent conductive HSA with 9.20 mm width.
3. ESD-surface resistivity is $\geq 1 \times 10^5 \sim \leq 1 \times 10^{10}$ Ohms/square per EIA, JEDEC TNR Specification.
4. All measurements are in millimeters.



Detail A

200504-014

Figure 14. SKY13278-313LF Tape and Reel Dimensions

Ordering Information

Model Name	Manufacturing Part Number	Evaluation Board Part Number
SKY13278-313LF SPDT Switch	SKY13278-313LF	SKY13278-313LF-EVB

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