DATA SHEET

SKY65111-348LF: ISM 600–1100 MHz Band 2 Watt InGaP HBT Power Amplifier

Features

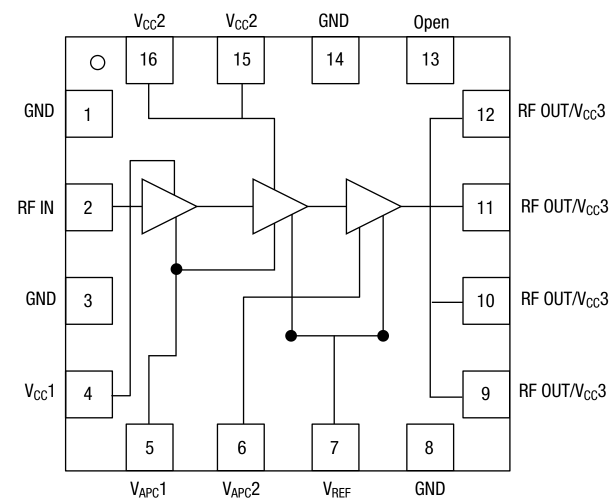
- Optimized for 800–1100 MHz operation
- Output power greater than 33 dBm @915 MHz
- 3.5 V nominal operating voltage
- Integrated analog power control voltage, V_{APC} = 0.1–2.8 V
- High PAE at maximum output power
- Ultrasmall, thermally enhanced micro lead frame package.
- Low current in standby mode of < 10 µA
- Available on tape and reel
- Available lead (Pb)-free and RoHS-compliant

Description

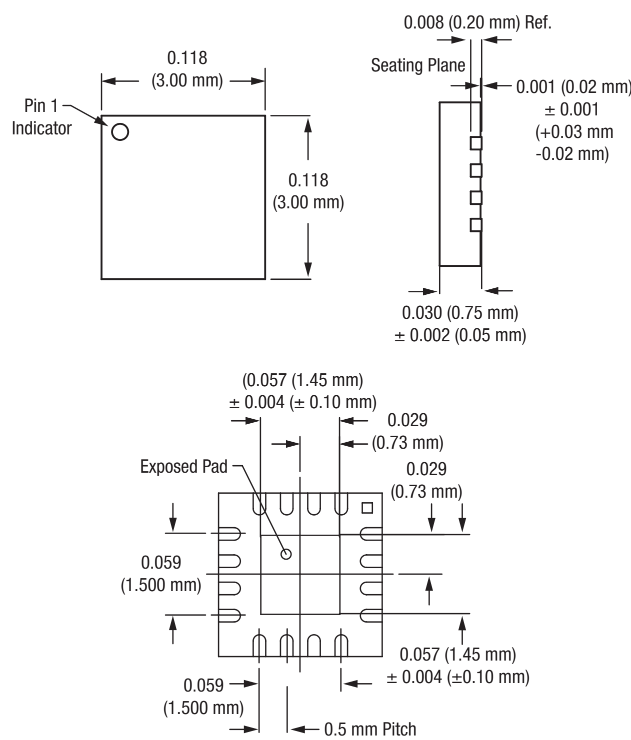
The SKY65111-348LF is a high-performance 3-stage, high-power amplifier IC designed for use in 600–1100 MHz ISM band applications such as automatic meter readers and RFID. It has an integrated analog power control voltage for achieving the desired output power levels. The IC is manufactured on an advanced InGaP HBT process. The SKY65111-348LF is packaged in a thermally enhanced, ultrasmall, micro lead frame package.

NEW Skyworks offers lead (Pb)-free, RoHS (Restriction of Hazardous Substances)-compliant packaging.

Block Diagram



Package Dimensions



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Pin Assignments

Pin	Symbol	Description
1, 3, 8, 14	GND	Connect this pin to the printed circuit board common via lowest possible impedance.
2	RF IN	RF input port.
4	$V_{CC}1$	DC power supply input to the first gain stage.
5	$V_{APC}1$	Power control voltage input to the first and second gain stages.
6	$V_{APC}2$	Power control voltage input to the third gain stage.
7	V_{REF}	Control voltage input to bias control circuit.
9, 10, 11, 12	RF OUT/ $V_{CC}3$	RF output ports and DC supply voltage inputs to third gain stage.
13	OPEN	No connection. Do not connect this pin to ground.
15, 16	$V_{CC}2$	DC power supply input to the second gain stage.

Absolute Maximum Ratings

Characteristic	Value
Supply voltage (V_{CC} & V_{REF})	5.5 V
Power control voltage ($V_{APC}1$ & $V_{APC}2$)	3.0 V
RF input power	10 dBm
Operating temperature	-40 °C to +85 °C
Storage temperature	-65 °C to +85 °C

Performance is guaranteed only under the conditions listed in the specifications table and is not guaranteed under the full range(s) described by the Absolute Maximum specifications. Exceeding any of the absolute maximum/minimum specifications may result in permanent damage to the device and will void the warranty.
Each absolute maximum rating listed is an individual parameter. Basing and driving the amplifier with all absolute maximum ratings listed simultaneously may result in permanent damage to the device.

CAUTION: *Although this device is designed to be as robust as possible, ESD (Electrostatic Discharge) can damage this device. This device must be protected at all times from ESD. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD precautions must be employed at all times.*

General DC Electrical Specifications

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply voltage	V_{CC}		2.5	3.5	5	V
Power control voltage	V_{APC}		0	2.7	2.8	V
Power control range				45		dB
Power control current	IVAPC				5	mA
Leakage current		P_{IN} < -30 dBm, $V_{APC}1$, 2 = 0.1 V			10	µA
Thermal resistance	R_{TH}			50		° C/W

Guaranteed Performance

V_{CC} = 3.5 V, V_{REF} = 3.5 V, V_{APC} = 2.7 V, T_A = 25 °C

Parameter	Symbol	Condition	Specification	Unit
Critical gain	$\|S_{21}\|$	902–928 NHz, -30 dBm input	36 min.	dB
Saturated power	P_{SAT}	915 MHz	30 min.	dBm

Guaranteed performance is as measured in the application's PC board as defined in this data sheet.

General RF Transmit Electrical Specifications

Conditions: V_{CC} = 3.5 V, V_{REF} = 3.5 V, V_{APC} = 2.7 V, P_{IN} = -30 dBm, T_A = 25 °C

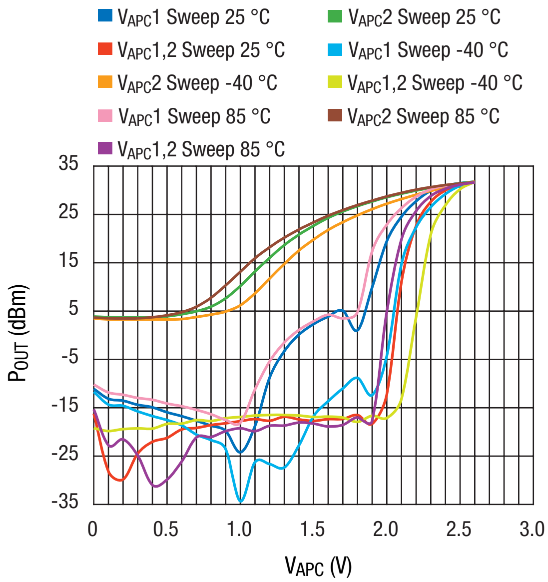
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Frequency range	F		902		928	MHz
Gain	$\|S_{21}\|$	Small signal		40		dB
Gain variation over frequency	$\|\Delta S_{21}\|$	Small signal		0.3		dB
Input return loss	$\|S_{11}\|$	Small signal		-12		dB
Output return loss	$\|S_{22}\|$	Small signal		-15		dB
Quiescent current	I_{CQ}	(No RF signal)		0.25		A
Output $P_{1\ dB}$	$P_{1\ dB}$	CW		29.5		dBm
Current consumption	I_{CC}	Output $P_{1\ dB}$		0.7		A
Saturated power @ 915 MHz	P_{SAT}	V_{CC} = 3.5 V, V_{REF} = 3.5 V, V_{APC}1, 2 = 2.7 V		33		dBm
Power added efficiency	PAE	P_{SAT}		50		%
Second harmonic	F_2	Output $P_{1\ dB}$		-28		dBm
Third harmonic	F_3	Output $P_{1\ dB}$		-38		dBm
Ruggedness		Output VSWR = 8:1, All phase angles, V_{CC} = 5 V, P_{IN} = -5 dBm, V_{APC} = 2.7 V V_{REF} = 5 V	No module damage or permanent performance degradation			
Stability		Output VSWR = 8:1, All phase angles, V_{CC} = 5 V, P_{IN} = -10 dBm, V_{APC} = 2.7 V V_{REF} = 5 V		-36		dBm

Conditions: V_{CC} = 3.5 V, V_{REF} = 3.5 V, V_{APC} = 2.7 V, P_{IN} = -30 dBm, T_A = 25 °C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Frequency range	F		800		1100	MHz
Gain	$\|S_{21}\|$	Small signal		39.5		dB
Gain variation over frequency	$\|\Delta S_{21}\|$	Small signal		1.0		dB
Input return loss	$\|S_{11}\|$	Small signal		-11		dB
Output return loss	$\|S_{22}\|$	Smal signal		-8		dB
Output $P_{1\ dB}$	$P_{1\ dB}$	CW		27		dBm
Quiescent current	I_{CQ}	(No RF signal)		0.25		A
Current consumption	I_{CC}	Output $P_{1\ dB}$		0.7		A
Second harmonic	F_2	Output $P_{1\ dB}$		-17		dBm
Third harmonic	F_3	Output $P_{1\ dB}$		-35		dBm
Ruggedness		Output VSWR = 8:1, All phase angles, V_{CC} = 5 V, P_{IN} = -5 dBm, V_{APC} = 2.7 V V_{REF} = 5 V	No module damage or permanent performance degradation			
Stability		Output VSWR = 8:1, All phase angles, V_{CC} = 5 V, P_{IN} = -10 dBm, V_{APC} = 2.7 V, V_{REF} = 5 V		36		dBm
Saturated power @ 800 MHz	P_{SAT}	V_{CC} = 3.5 V, V_{REF} = 3.5 V, V_{APC}1, 2 = 2.7 V		32		dBm
Power added efficiency @ 800 MHz	PAE	P_{SAT}		45		%
Saturated power @ 1100 MHz	P_{SAT}	V_{CC} = 3.5 V, V_{REF} = 3.5 V, V_{APC}1, 2 = 2.7 V		30		dBm
Power added efficiency @ 1100 MHz	PAE	P_{SAT}		40		%

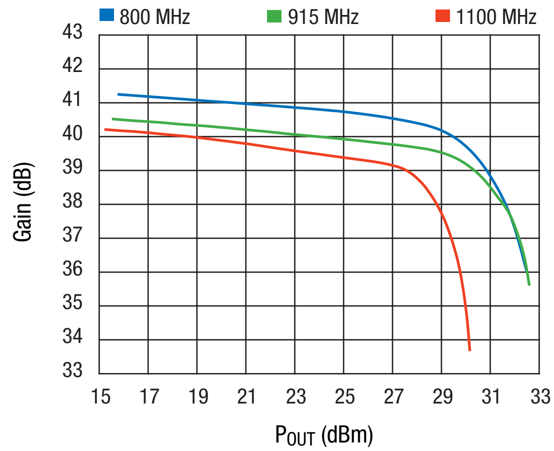
Unless otherwise stated V_{REF} = V_{CC}.

Typical Performance Data

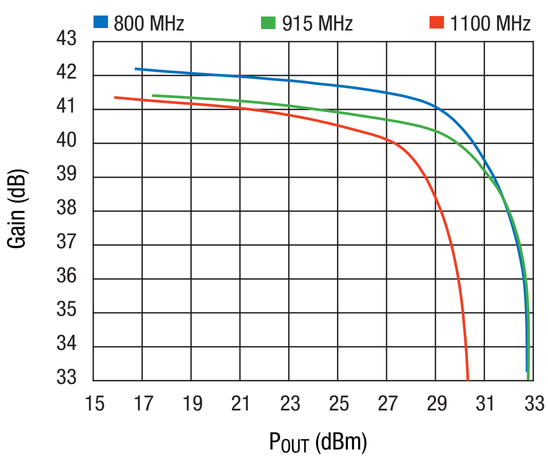


P_{OUT} vs. V_{APC}
915 MHz, P_{IN} = -5 dBm

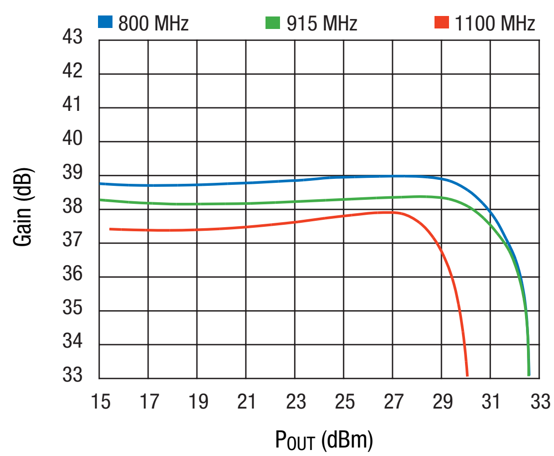
$V_{APC}1$ varied from 0 V–2.6 V, $V_{APC}2$ held at 2.6 V.
$V_{APC}2$ varied from 0 V–2.6 V, $V_{APC}1$ held at 2.6 V.
$V_{APC}1$ and $V_{APC}2$ varied from 0 V–2.6 V together.



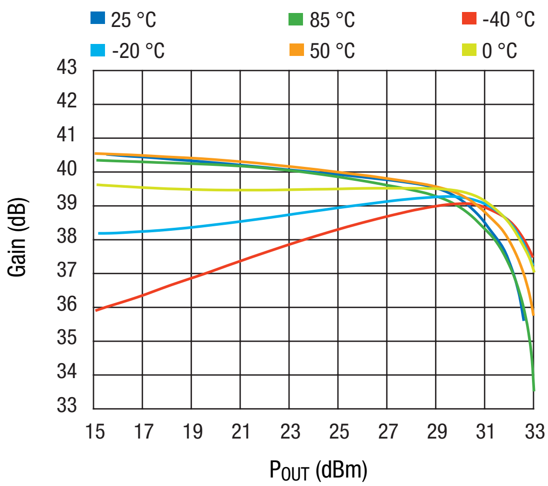
Gain vs. P_{OUT} and Frequency
V_{CC} = 3.5, T = 25 °C, $V_{APC}1,2$ = 2.7 V



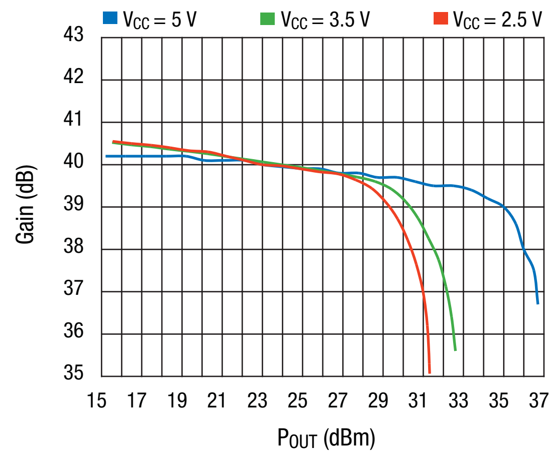
Gain vs. P_{OUT} and Frequency
V_{CC} = 3.5, T = 25 °C, $V_{APC}1,2$ = 2.8 V



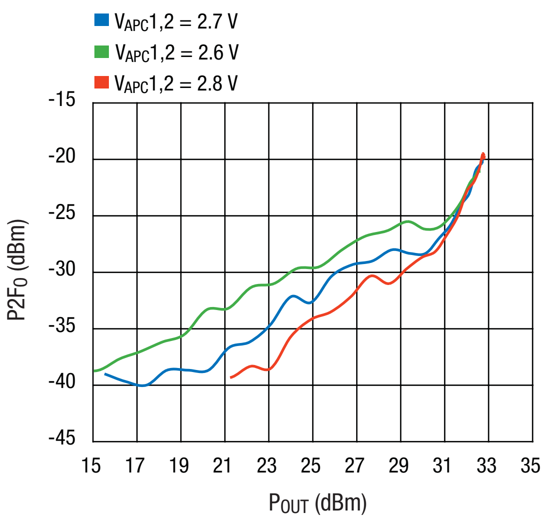
Gain vs. P_{OUT} and Frequency
V_{CC} = 3.5, T = 25 °C, $V_{APC}1,2$ = 2.6 V



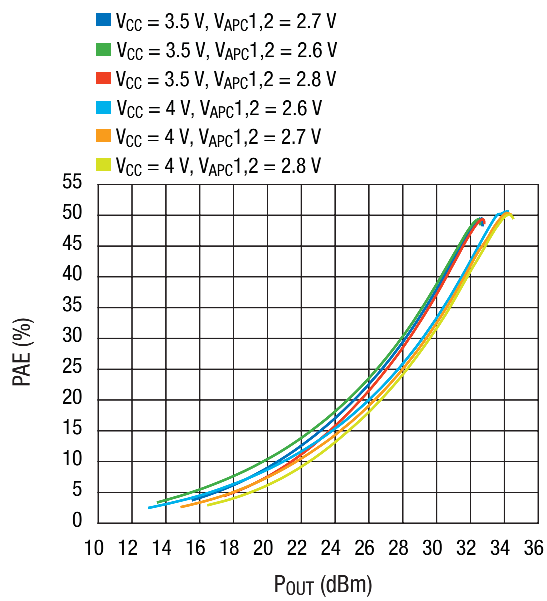
Gain vs. P_{OUT}, V_{CC} = 3.5, V_{APC}1, 2 = 2.7 V, 915 MHz



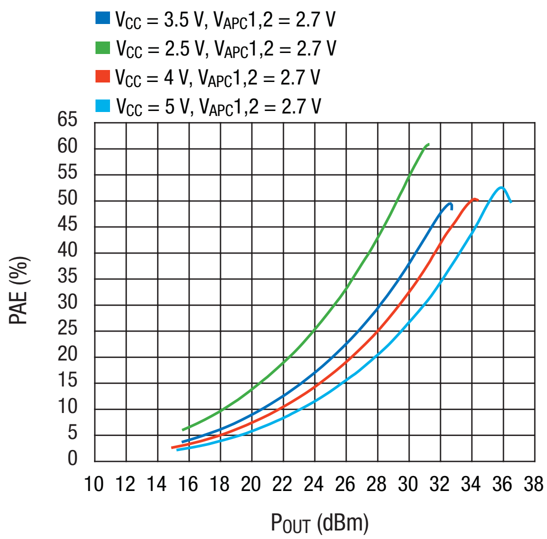
Gain vs. P_{OUT}, V_{APC}1, 2 = 2.7 V, 915 MHz @ 25 °C



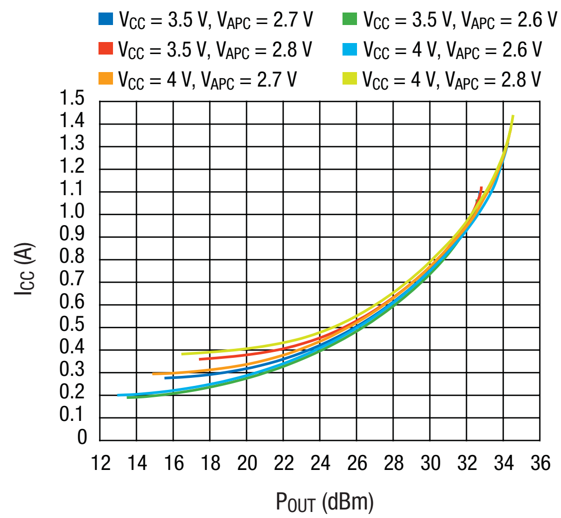
$2F_0$ vs. P_{OUT}, 915 MHz Fundamental, V_{CC} = 3.5 V 25 °C



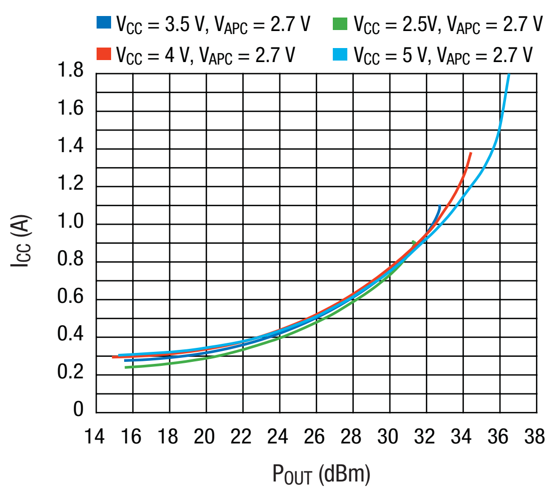
% PAE vs. V_{APC}1, 2, and V_{CC} 915 MHz @ 25 °C



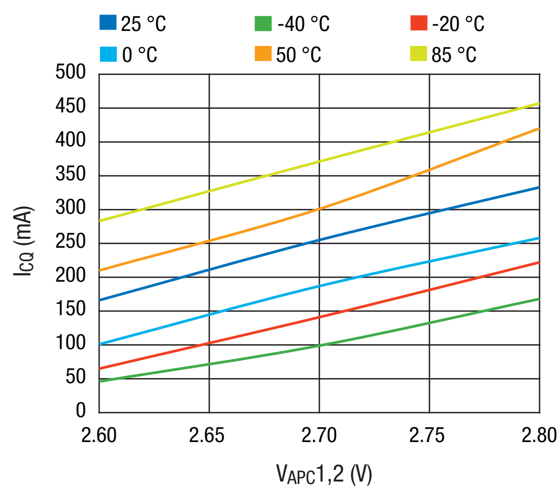
% PAE vs. P_{OUT} and V_{CC}, V_{APC}1,2 = 2.7, 915 MHz @ 25 °C



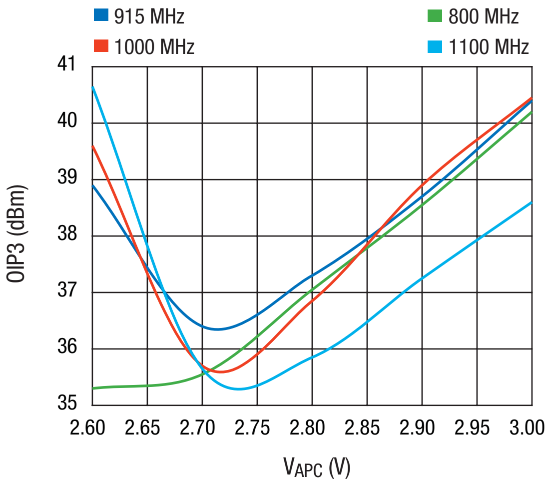
I_{CC} vs. P_{OUT}, V_{CC} and V_{APC}1,2 915 MHz, 25 °C



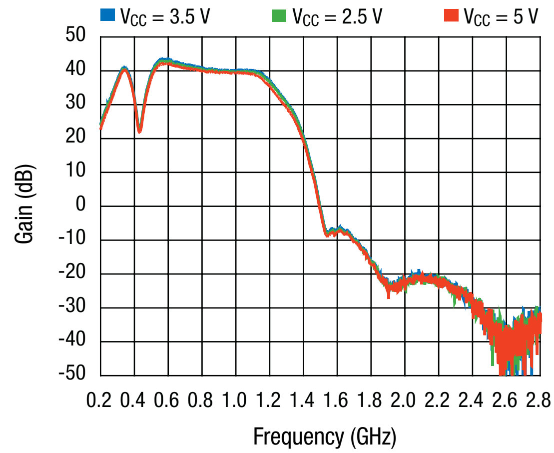
I_{CC} vs. P_{OUT} and V_{CC}, V_{APC}1,2 = 2.7 V, 915 MHz @ 25 °C



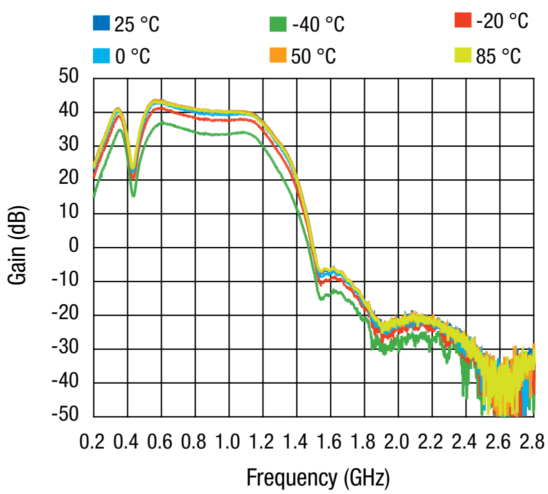
I_{CQ} vs V_{APC}1, 2, V_{CC} = 3.5 V RF Off @ 25 °C



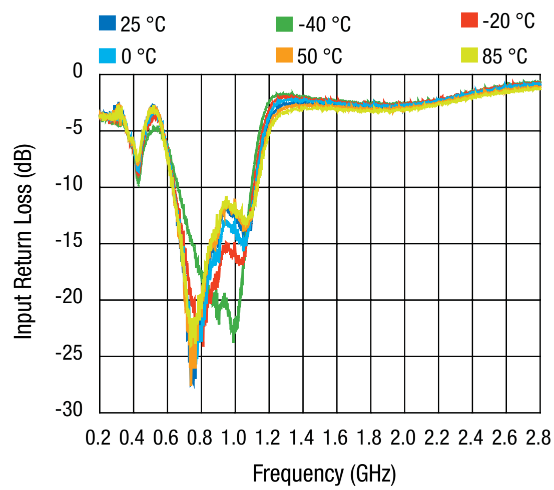
OIP3 vs. V_{APC}1,2, Tone Spacing 1 MHz
V_{CC} = 3.5 V P_{OUT} = 20 dBm @ 25 °C



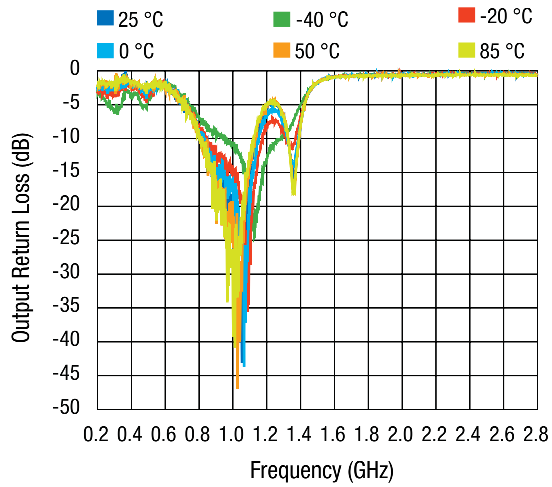
Gain vs. Frequency, V_{APC}1, 2 = 2.7 V
P_{IN} = -30 dBm, 25 °C



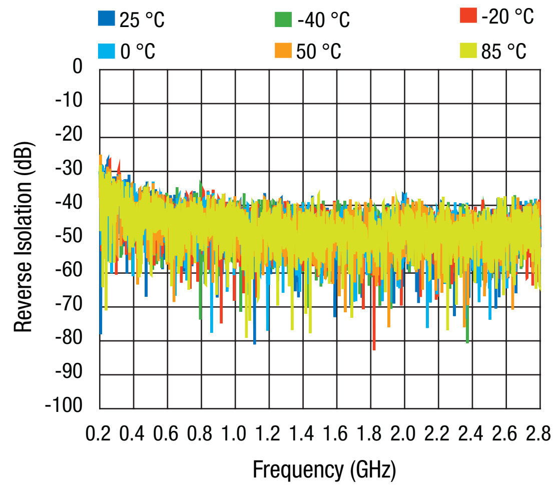
Gain vs. Frequency, V_{CC} = 3.5 V,
P_{IN} = -30 dBm, V_{APC}1,2 = 2.7 V



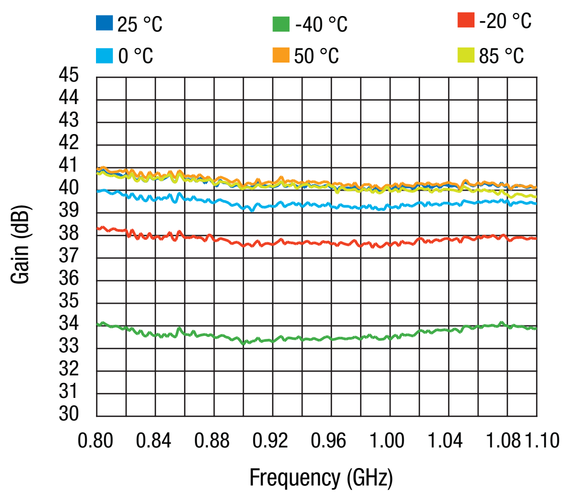
Input Return Loss vs. Frequenc
V_{CC} = 3.5 V, P_{IN} = -30 dBm, V_{APC}1,2 = 2.7 V



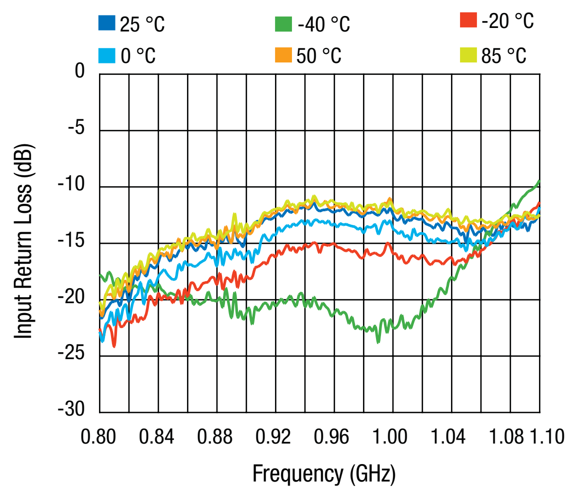
Output Return Loss vs. Frequency, V_{CC} = 3.5 V
P_{IN} = -30 dBm, V_{APC}1,2 = 2.7 V



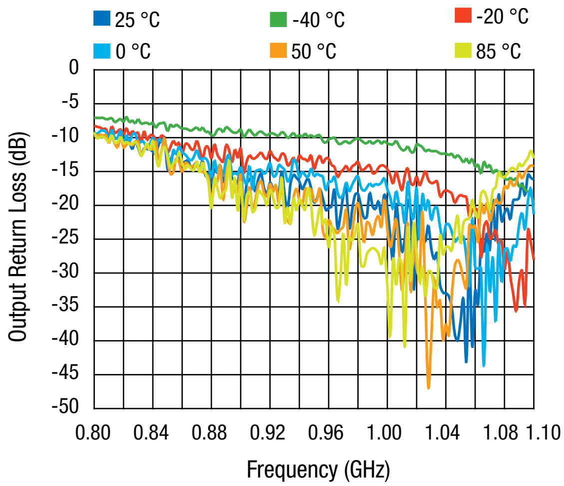
Reverse Isolation vs. Frequency, V_{CC} = 3.5 V
P_{IN} = -30 dBm, V_{APC}1,2 = 2.7 V



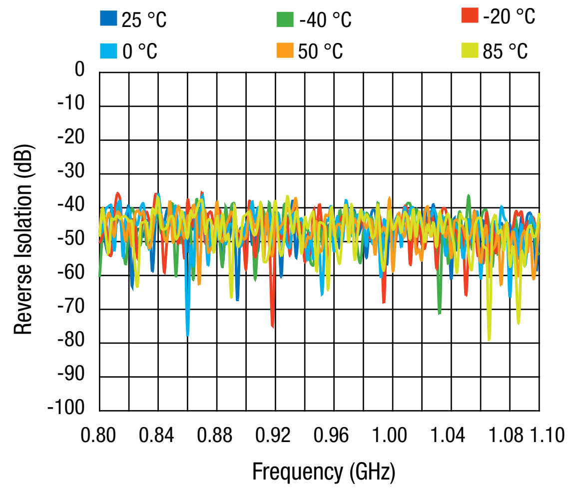
Gain vs. Frequency, V_{CC} = 3.5 V
P_{IN} = -30 dBm, V_{APC}1,2 = 2.7 V



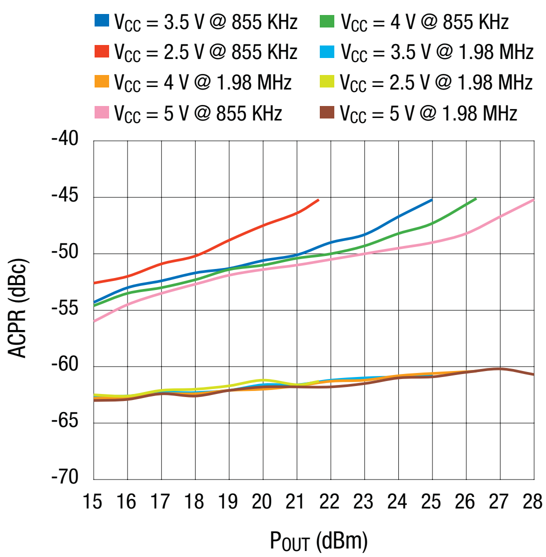
Input Return Loss vs. Frequency, V_{CC} = 3.5 V
P_{IN} = -30 dBm, V_{APC}1,2 = 2.7 V



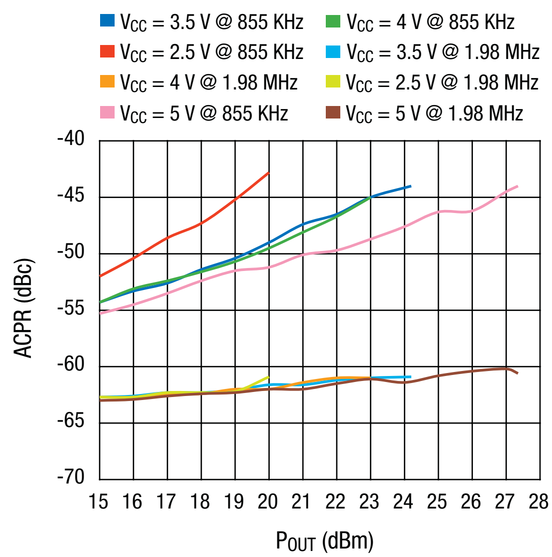
Output Return Loss vs. Frequency, V_{CC} = 3.5 V
P_{IN} = -30 dBm, V_{APC}1,2 = 2.7 V



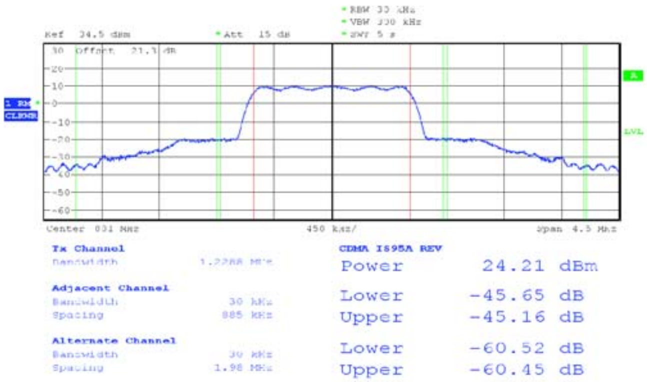
Reverse Isolation vs. Frequency, V_{CC} = 3.5 V
P_{IN} = -30 dBm, V_{APC}1,2 = 2.7 V



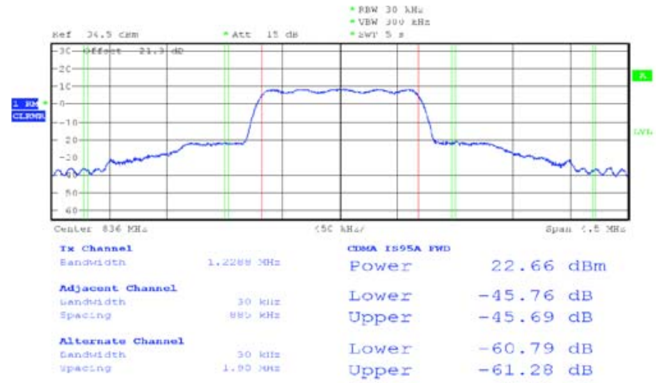
ACPR vs, P_{OUT} and Frequency
IS-95, V_{APC}1,2 = 2.7 V, 881 MHz @ 25 °C



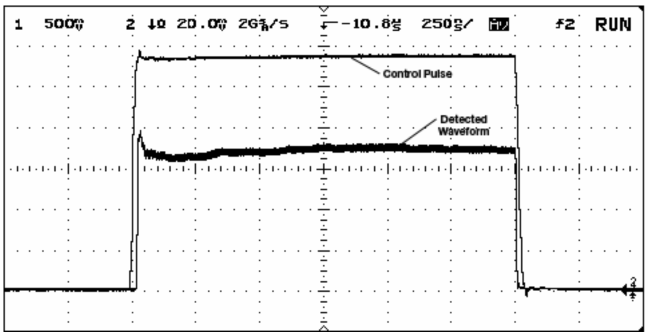
ACPR vs, P_{OUT} and Frequency
IS-95, V_{APC}1,2 = 2.7 V, 836 MHz @ 25 °C



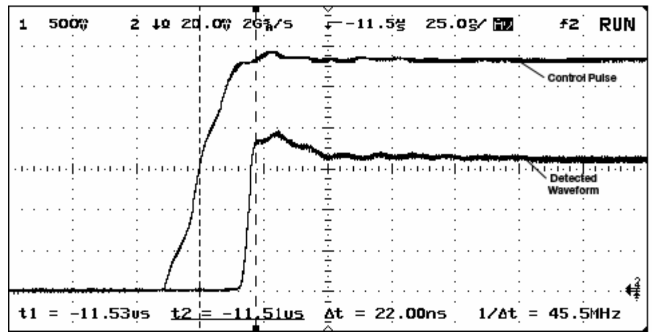
ACPR, IS-95 REV, V_{CC} 3.5 V, V_{APC}1, 2 = 2.7 V
881 MHz @ 25 °C



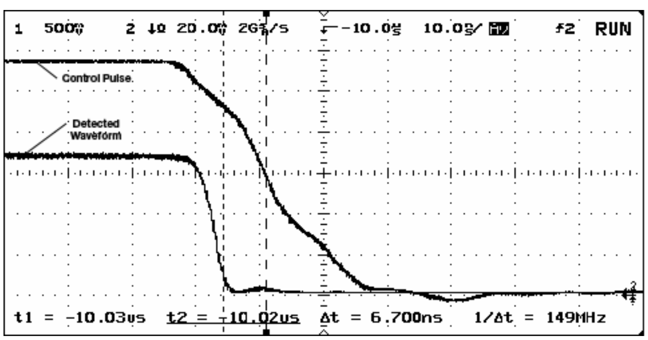
ACPR, IS-95 FWD, V_{CC} 3.5 V, V_{APC}1, 2 = 2.7 V
836 MHz @ 25 °C



Response Time, P_{IN} = -15 dBm, 915 MHz, V_{CC} = 3.5 V, V_{APC}1, 2 = 2.7 V @ 25 °C



Response Time, Rise Time, 50% Ctrl, 90% RF
V_{APC}1, 2 = 2.7 V/0 V @ 25 °C



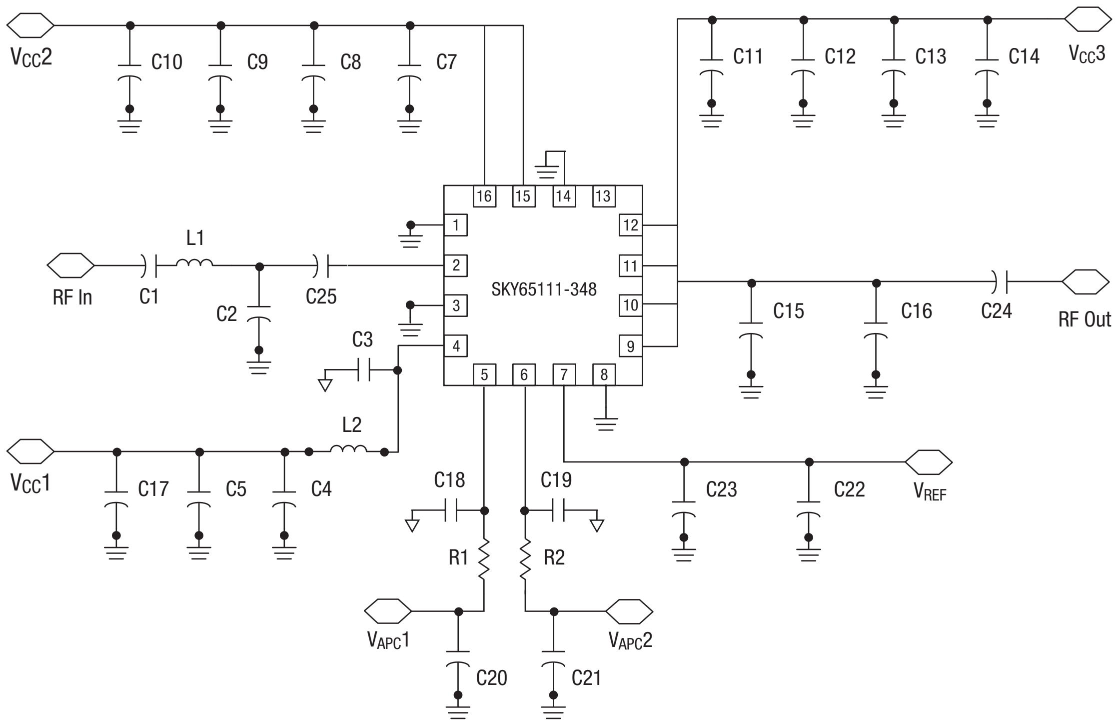
Response Time, Fall Time 90% RF, 50% Ctrl
V_{APC}1, 2 = 2.7 V/0 V @ 25 °C

Bill of Material for Evaluation Board

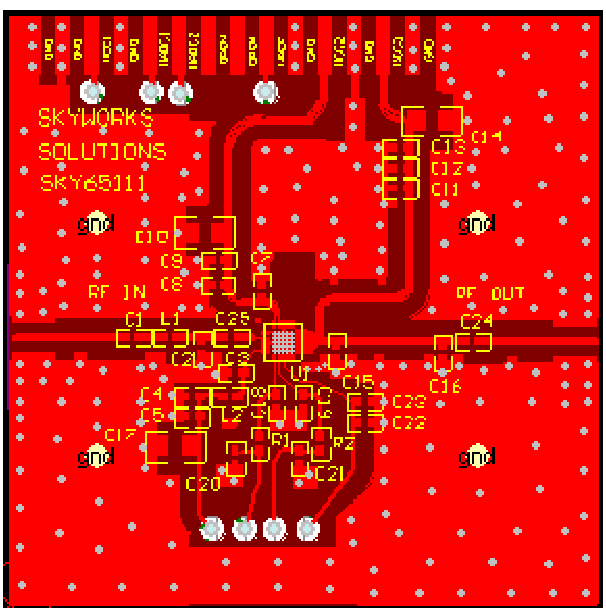
Designator	Value	Size	Manufacturer	Part Number	Notes
C1	100 pF	0402	Murata	GRM1555C1H101JD83E	
C2	2.2 pF	0402	Murata	GRM1555C1H2R2JZ35E	
C3	4.7 pF	0402	Murata	GRM1555C1H4R7JZ35E	
C4	100 pF	0402	Murata	GRM1555C1H101JD83E	
C5	1000 pF	0402	Murata	GRM155R71H102KA01	1
C7	DNP				2
C8	100 pF	0402	Murata	GRM1555C1H101JD83E	
C9	1000 pF	0402	Murata	GRM155R71H102KA01	1
C10	10 µF	0402	AVX	TAJA106M006R	
C11	100 pF	0402	Murata	GRM1555C1H101JD83E	1
C12	1000 pF	0402	Murata	GRM155R71H102KA01	1
C13	10 nF	0402	Murata	GRM155R71E103KA01	1
C14	10 µF	1206	AVX	TAJA106M006R	
C15	12 pF	0402	Murata	GJM1555C1H120JB01E	
C16	5.6 pF	0402	Murata	GJM1555C1H5R6CB01E	
C17	10 µF	1206	AVX	TAJA106M006R	
C18	DNP				2
C19	DNP				2
C20	DNP				2
C21	DNP				2
C22	1000 pF	0402	Murata	GRM155R71H102KA01	
C23	100 pF	0402	Murata	GRM1555C1H101JD83E	
C24	100 pF	0402	Murata	GRM1555C1H101JD83E	
C25	18 pF	0402	Murata	GRM1555C180JZ35E	
L1	1.8 nH	0402	Johanson	L-07C1N8ST	
L2	1 nH	0402	Johanson	L-07C1N0ST	
R1	0 W	0402	Panasonic	ERJ2BJ00X	1
R2	0 W	0402	Panasonic	ERJ2BJ00X	1

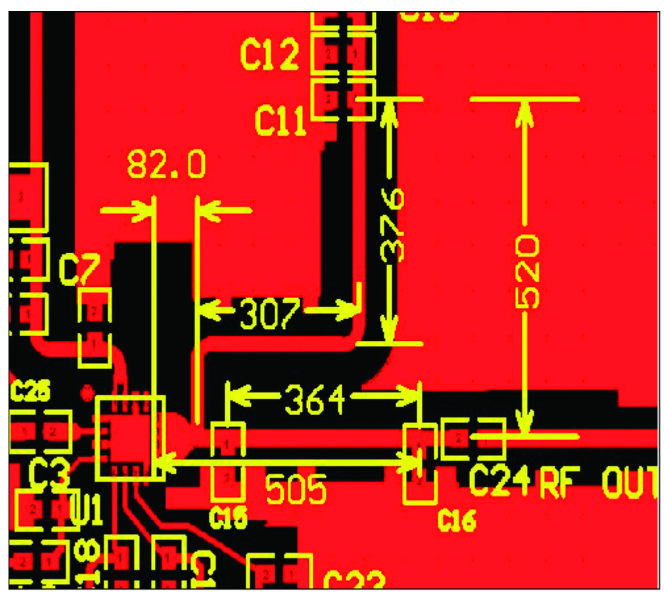
1. Panasonic and Murata are Skyworks preferred vendors. However, any suitable equivalent part is acceptable for this component.
2. "DNP" = Do not place.

Application Circuit



Component Placement Diagram





Transmission line width: 0.027 inches.
Gerber files available upon request.

Incorrect soldering of the device paddle to grounding pad may lead to parasitic oscillations, reduced performance and increased device temperature rise. Uniform coverage over the entire bottom ground paddle must be maintained to avoid these conditions.

Application Circuit Notes

Ground, (Pins 1, 3, 8, 14). Attach all ground pins to the RF ground plane with the largest diameter and lowest inductance via that the layout will allow. Multiple small vias are also acceptable and will work well under the device if solder migration is an issue. It is extremely important that the device paddle be sufficiently grounded for both thermal and stability reasons. Please refer to the enclosed Package Footprint.

RF input (Pin 2). A lumped element matching structure for good in-band return loss has been realized on the RF input, Pin 2. This structure is comprised of a DC blocking capacitor (C1), low pass LC filter (L1, C1) and at the device input, a series capacitor (C25). This combination of devices will yield a return loss better than -11 dB over the entire 800–1100 MHz band of interest. The placement of C1 is not critical; it can be moved as close to L1, C2 and C25 as desired. C25 should be placed as close to the device pin as possible to replicate performance as measured on the applications board.

V_{CC}1 (Pin 4). V_{CC}1 is the collector bias for the first amplifier stage in the SKY65111. Multiple bypass capacitors, C3-C5, C17 and a series inductor, L2, have been utilized to ensure stability both in and out of the useable bandwidth of the device. The length of transmission line between L2 and Pin 4 is not critical; L2 can be placed as close to the pin as possible if desired. However, placement of L2 farther away from Pin 4 than shown on the Applications Circuit is not recommended. C3 should also be placed in the approximate location shown on the Applications Circuit, but placement is not critical.

V_{APC}1 (Pin 5). V_{APC}1 is the bias control voltage input for amplifier stages 1 and 2. Nominal operating range is between 2.6 V_{DC} and 2.8 V_{DC}, with 3 V_{DC} producing the minimum attenuation point. V_{APC}1 may also be set to 0 V_{DC}, to force stages 1 and 2 into standby mode.

V_{APC}2 (Pin 6). V_{APC}2 is the bias control voltage for amplifier stage 3. Nominal operating range is between 2.6 V_{DC} and 2.8 V_{DC}, with 3 V_{DC} producing the minimum attenuation point. A 100 pF capacitor (C19) may be used for bypassing at high frequencies. The value of this capacitor may also be made large, greater than 1000 pF, if longer response time is acceptable. V_{APC}2 may also be set to 0 V_{DC}, to place amplifier stage 3 into standby status.

NOTE: *In most applications V_{APC}1 and V_{APC}2 pins are directly tied together and biased from the same control voltage. V_{APC}1 and V_{APC}2 may also be split if independent control is desired.*

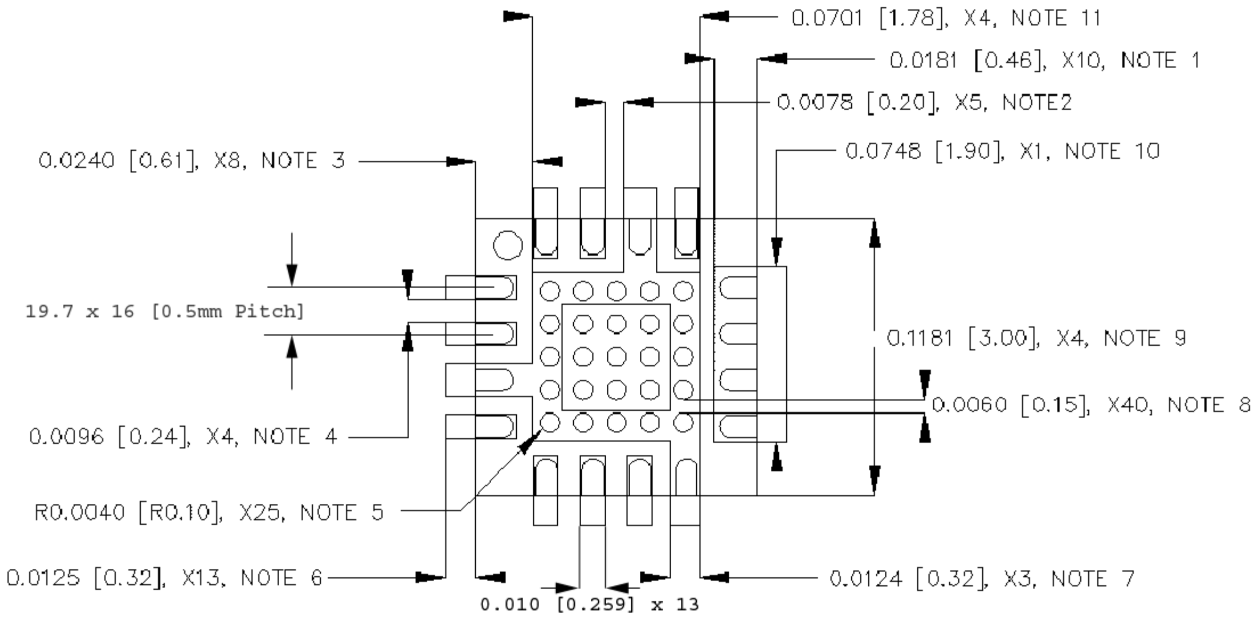
V_{REF} (Pin 7). V_{REF} is the bias reference voltage for amplifier stages 2 and 3. V_{REF} should be operated over the same voltage range as V_{CC}, with a nominal voltage of 3.5 V_{DC}. Bypassing of V_{REF} is accomplished with C22 and C23 which should be placed as close to the device pin as possible.

RF_{OUT}, V_{CC}3 (Pins 9-12). RF_{OUT} and V_{CC}3 are the biasing input of the stage 3 collectors. Bias is applied to the RF output through a length of transmission line that is approximately 827 mils (21 mm) long. Capacitors C11-C14 provide proper RF bypassing and should be placed as shown in the Applications Circuit. Output matching for optimal power gain is accomplished with capacitors C15 and C16. Spacing between these capacitors with respect to the RF output and each other is critical and is shown on the Component Placement Diagram. Special care must be taken when placing these devices; their locations should not deviate significantly from the locations as shown. If these capacitors are not located properly, large decreases in output power and efficiency will occur.

Pin 13. Pin 13 has no connection and should be left open circuit.

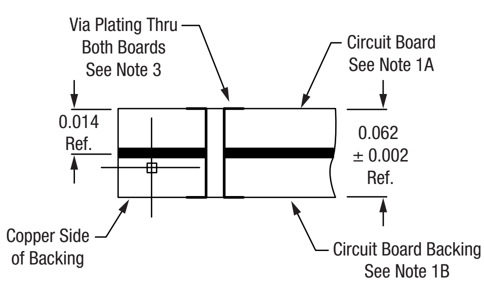
V_{CC}2 (Pins 15-16). V_{CC}2 is the collector bias input for the second amplifier stage in the SKY65111. Multiple bypass capacitors, C8-C10 have been utilized to ensure stability both in and out of the useable bandwidth of the device. Capacitor C7 is not populated with the normal tuning configuration described above.

Package Footprint



NOTE: All units in inches [mm].
NOTE 1: Length of all non–grounded lands underneath the package.
NOTE 2: Width between grounded lands and non–grounded lands.
NOTE 3: Length of from ground pad to edge of package.
NOTE 4: Width between non–grounded lands.
NOTE 5: Radius of the vias.
NOTE 6: Length of all lands from the edge of the package.
NOTE 7: Width of the ground lands.
NOTE 8: Distance betwwen all vias.
NOTE 9: X and Y dimension of the package.
NOTE 10: Width of the land for RFOUT.
NOTE 11: Width of the land for the ground pad.

Evaluation Board Stack-Up



Detail A

Application Board Bias Procedure

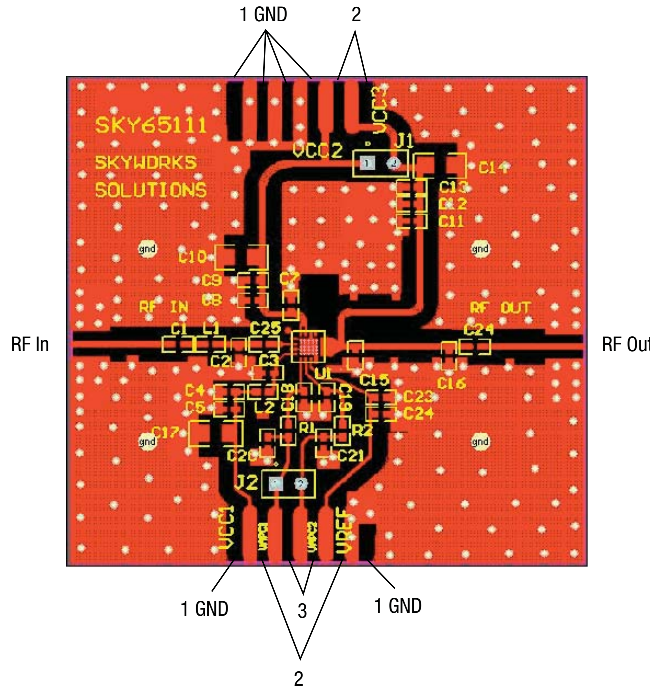
Step 1. Connect DC ground.

Step 2. Connect all V_{CC} and V_{REF} lines to 3.5 V supply, labeled 2.

Step 3. With the RF off, apply 2.7 V_{DC} to V_{APC}1, 2 control pins. Verify the I_{CQ} current is approximately 250 mA, labeled 3.

Step 4. Apply RF signal data -30 dBm level and observe that the output level is approximately 10 dBm or the gain of the device is approximately 40 dB.

NOTE: *It is important that the V_{CC}1, V_{CC}2, V_{CC}3, and V_{REF} voltage source be adjusted such that 3.5 V is measured at the board. The high collector currents will drop the collector voltage significantly if long leads are used. Adjust the bias voltage to compensate.*



Recommended Solder Reflow Profiles

Refer to the *"Recommended Solder Reflow Profile"* Application Note.

Tape and Reel Information

Refer to the *"Discrete Devices and IC Switch/Attenuators Tape and Reel Package Orientation"* Application Note.

Branding Specifications