8 bit 串入并出移位寄存器

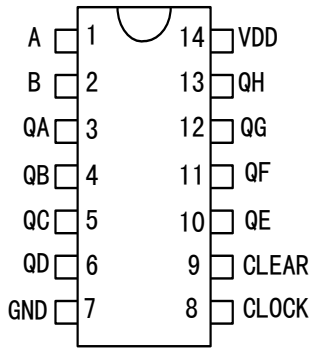
- AND-Gated (Enable/Disable) Serial Inputs
- Fully Buffered Clock and Serial Inputs
- Direct Clear
- Package Options Include Plastic
  Small-Outline (D) and Ceramic Flat (W)
  Packages, Ceramic Chip Carriers (FK), and
  Standard Plastic (N) and Ceramic (J)
  300-mil DIPS

DESCRIPTION

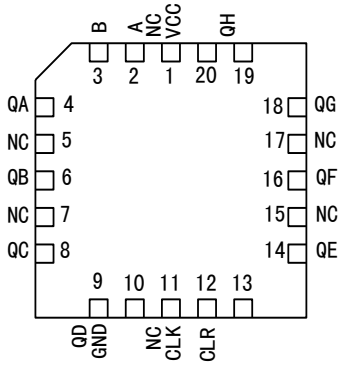
These 8-bit shift registers feature AND-gated serial inputs and an asynchronous clear (CLR) input. The gated serial (A and B) inputs permit complete control over incoming data; a low at either input inhibits entry of the new data and resets the first flip-flop to the low level at the next clock (CLK) pulse. A high-level input enables the other input, which then determines the state of the first flip-flop. Data at the serial inputs can be changed while CLK is high or low, provided the minimum setup time requirements are met. Clocking occurs on the low-to-high-level transition of CLK.

The 54HC164 is characterized for operation over the full military temperature range of –55℃ to 125℃. The 74HC164 is characterized for operation from -40℃ to 85℃.

54HC164…J OR W PACKAGE
74HC164…D OR N PACKAGE



54HC164…FK PACKAGE (TOP VIEW)



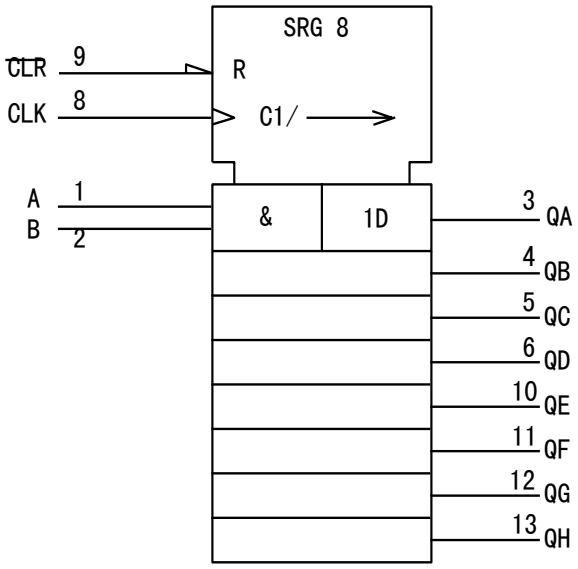
NC–NO internal connection

FUNCTION TABLE

INPUTS				OUTPUTS		
CLR	CLK	A	B	QA	QB...QH	
L	X	X	X	L	L	L
H	L	X	X	QA0	QB0	QH0
H	↑	H	H	H	QAn	QGn
H	↑	L	X	L	QAn	QGn
H	↑	X	L	L	QAn	QGn

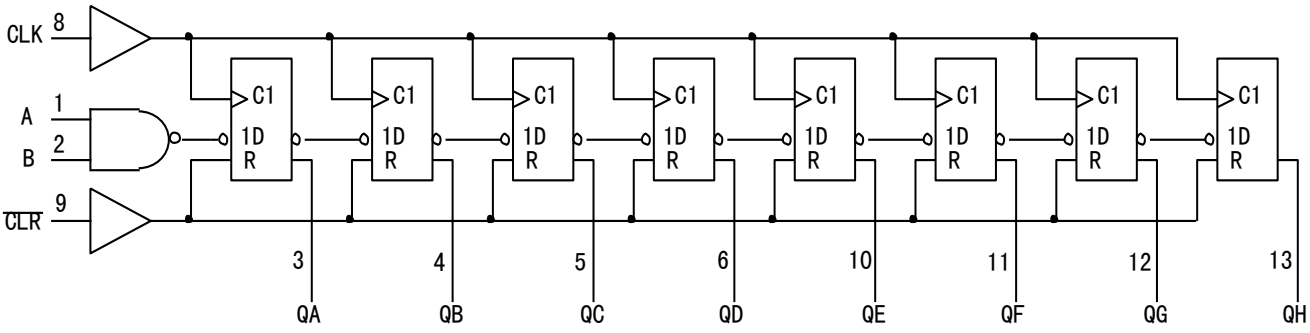
QA0, QB0, QH0=the level of QA, QB, or QH, respectively, before the indicated steady-state input conditions were established
QAn, QGn=the level of QA or QG before the most recent ↑ transition of CLK; indicates a 1-bit shift

LOGIC SYMBOLT



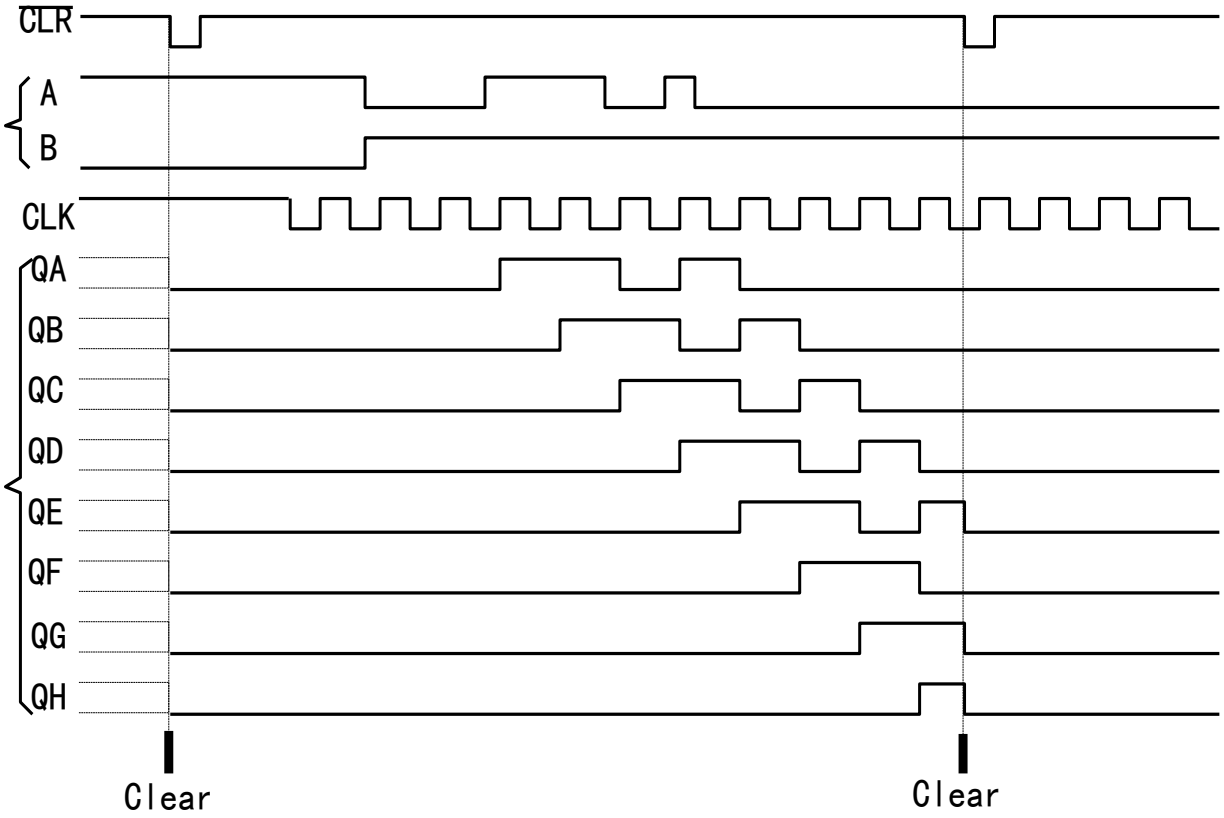
- This symbol is in accordance with ANS/IEEE Std 91-1984 and IEC publication 617-12.
- Pin numbers shown are for the D, J, N, and W packages.

LOGIC DIAGRAM (positive logic)



Pin numbers shown are for the D, J, N and W packages.

TYPICAL CLEAR, SHIFT, AND CLEAR SEQUENCE



Absolute maximum ratings over operating free-air temperature rangeT

Supply voltage range, Vcc……..-0.5V to 7V

Input clamp current, I_{IK} (V_I<0 or VI>Vcc)(see Note 1)……±20mA

Output clamp current, IOK (VO<) or VO>Vcc)(see Note 1)……±20mA

Continuous output current, IO (VO=0 to Vcc)……±25mA

Continuous current through Vcc or GND……±50mA

Packaged thermal impedance, θ JA (see Note 2): D packaged……127℃/W

N package…….. 78℃/W

Storage temperature range, Tstg……-65℃ to 150℃

T Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hale packages, which use a trace length of zero.

RECOMMENDED OPERATING CONDITIONS

		54HC164			74HC164			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Vcc Supply voltage		2	5	6	2	5	6	
V_{IH} High-level input voltage	VCC=2V	1.5	-	-	1.5	-		
	VCC=4.5V	3.15	-	-	3.15	-		
	VCC=6V	4.2	-	-	4.2	-		
V_{IL} Low-level input voltage	VCC=2V	0	-	0.5	0	-	0.5	
	VCC=4.5V	0	-	1.35	0	-	1.35	
	VCC=6V	0	-	1.8	0	-	1.8	
V_I Input voltage		0	-	VCC		0	VCC	V
V_O Output voltage		0	-	VCC		0	VCC	V
t_{tT} Input transition (rise and fall) time	VCC=2V	0	-	1000	0	-	1000	ns
	VCC=4.5V	0	-	500	0	-	500	
	VCC=6V	0	-	400	0	-	400	
T_A Operating free-air temperature		-55	-	125	-40	-	85	℃

T If this device is used in the threshold region (from V_{IL} max=0.5V to V_{IH}min=1.5V), there is a potential to go into the wrong state from induced grounding, causing double clocking. Operating with the inputs at tt=1000ns and VCC=2V does not damage the device; however, functionally, the CLK inputs are not ensured while in the shift, count, or toggle operating modes.

Electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		VCC	T_A=25℃			54HC164		74HC164		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I=V_{IH} or V_{IL}	I_{OH}=-20uA	2V	1.9	1.998	-	1.9	-	1.9	-	V
			4.5V	4.4	4.499	-	4.4	-	4.4	-	
			6V	5.9	5.999	-	5.9	-	5.9	-	
		I_{OH}=-4mA	4.5V	3.98	4.3	-	3.7	-	3.84	-	
		I_{OH}=-5.2mA	6V	5.48	5.8	-	5.2	-	5.34	-	
V_{OL}	V_I=V_{IH} or V_{IL}	I_{OL}=20uA	2V	-	0.002	0.1	-	0.1	-	0.1	V
			4.5V	-	0.001	0.1	-	0.1	-	0.1	
			6V	-	0.001	0.1	-	0.1	-	0.1	
		I_{OL}=4mA	4.5V	-	0.17	0.26	-	0.4	-	0.33	
		I_{OL}=5.2mA	6V	-	0.15	0.26	-	0.4	-	0.33	
I_I	V_I=V_{CC} or 0		6V	-	±0.1	±100	-	±1000	-	±1000	nA
I_{CC}	V_I=V_{CC} or 0, I_O=0		6V	-	-	8	-	160	-	80	uA
C_I			2V to 6V	-	3	10	-	10	-	10	pF

Timing requirements over recommended operating free-air temperature range (unless otherwise noted)

		VCC	T_A=25℃		54HC164		74HC164		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock} Clock frequency		2V	0	6	0	4.2	0	5	MHz
		4.5V	0	31	0	21	0	25	
		6V	0	36	0	25	0	28	
t_W Pulse duration	$\overline{CLR}$ low	2V	100	-	150	-	125	-	ns
		4.5V	20	-	30	-	25	-	
		6V	17	-	25	-	21	-	
	CLK high or low	2V	80	-	120	-	100	-	
		4.5V	16	-	24	-	20	-	
		6V	14	-	20	-	18	-	
t_{su} Setup time before CLK ↑	Date	2V	100	-	150	-	125	-	ns
		4.5V	20	-	30	-	25	-	
		6V	17	-	25	-	21	-	
	CLR inactive	2V	100	-	150	-	125	-	
		4.5V	20	-	30	-	25	-	
		6V	17	-	25	-	21	-	
t_h Hold time, data after CLK ↑		2V	5	-	5	-	5	-	ns
		4.5V	5	-	5	-	5	-	
		6V	5	-	5	-	5	-	

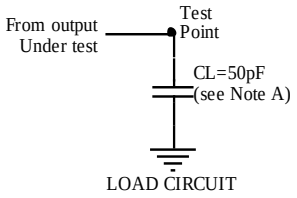
Switching characteristics over recommended operating free-air temperature rang, C_L=50pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	VCC	T_A=25℃			54HC164		74HC164		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			2V	6	10	-	4.2	-	5	-	MHz
			4.5V	31	54	-	21	-	25	-	
			6V	36	62	-	25	-	28	-	
t_{PHL}	CLR	Any Q	2V	-	140	205	-	295	-	255	ns
			4.5V	-	28	41	-	59	-	51	
			6V	-	24	35	-	51	-	46	
t_{pd}	CLK	Any Q	2V	-	115	175	-	265	-	220	
			4.5V	-	23	35	-	53	-	44	
			6V	-	20	30	-	45	-	38	
t_t			2V	-	38	75	-	110	-	95	ns
			4.5V	-	8	15	-	22	-	19	
			6V	-	6	13	-	19	-	16	

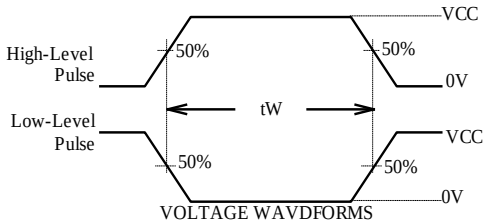
Operating characteristics, T_A=25℃

PARAMETER	TEST CONDITIONS	TYP	UNIT
Cpd Power dissipation capacitance	No load	135	pF

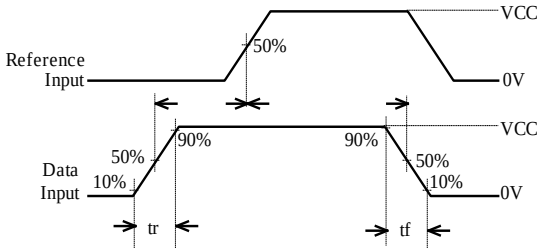
PARAMETER MEASUREMENT INFORMATION



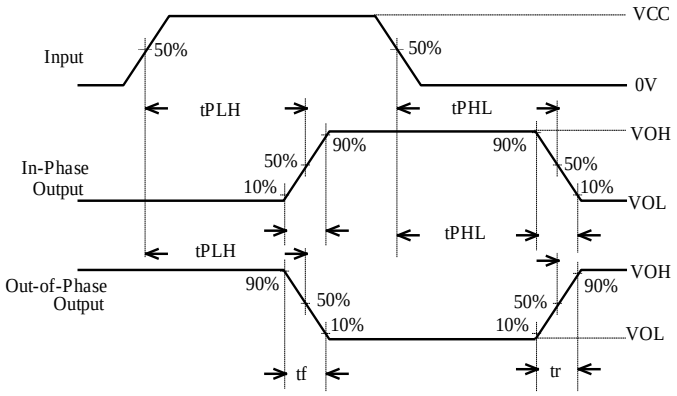
LOAD CIRCUIT



VOLTAGE WAVDFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
SETUP AND HOLD AND INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES

NOTES: A. C_L includes probe and test-fixture capacitance.

B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR≤1MHz, Z_O=50Ω, t_r=6ns, t_f=6ns.

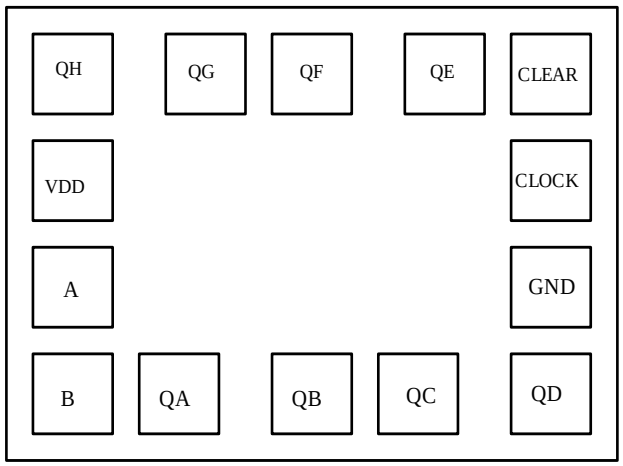
C. For clock inputs, f_{max} is measured when the input duty cycle is 50%

D. The outputs are measured one at a time with one input transition per measurement.

E. t_{PLH} and t_{PHL} are the same as t_{pd}.

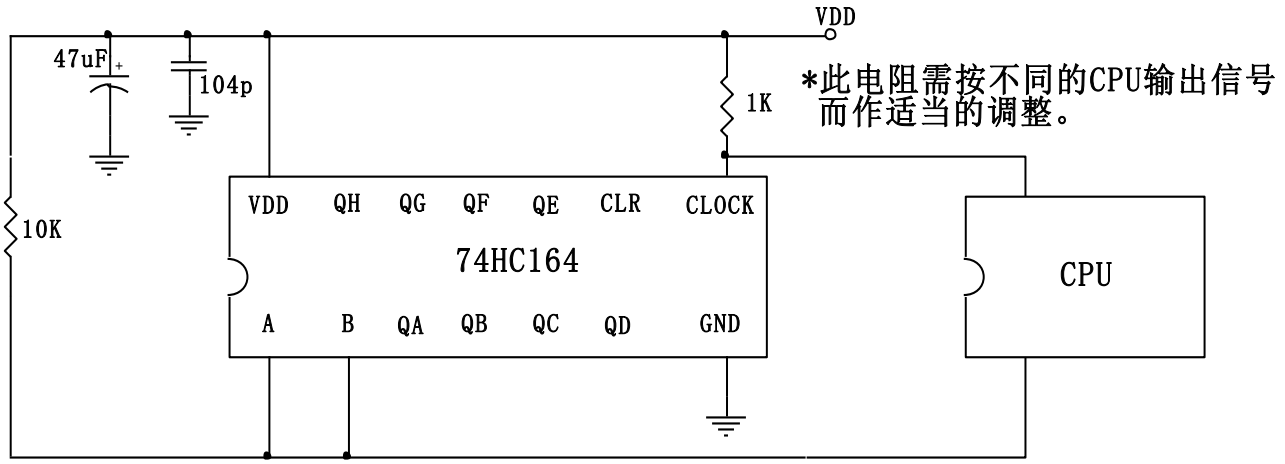
Figure 1. Load Circuit and Voltage Waveforms

PAD ASSIGNMENT



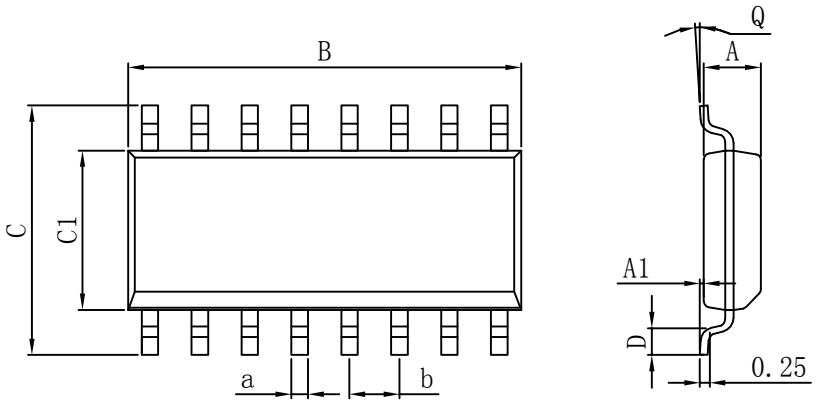
Pad No	Pad Name	X	Y
1	A	-242.00	-53.50
2	B	-250.00	252.00
3	QA	-135.00	-188.50
4	QB	0.00	-188.50
5	QC	115.00	-188.50
6	QD	252.00	-188.50
7	GND	252.00	-73.50
8	CLOCK	241.85	41.50
9	CLEAR	252.00	180.50
10	QE	137.00	190.50
11	QF	2.00	190.50
12	QG	-113.00	190.50
13	QH	-250.00	190.50
14	VDD	-250.00	61.50

附图：



封装外形

SOP14



Dimensions In Millimeters					
Symbol :	Min :	Max :	Symbol :	Min :	Max :
A	4.520	4.620	D	0.400	0.950
A1	0.100	0.250	Q	0°	8°
B	8.500	9.000	a	0.420TYP	
C	5.800	6.250	b	1.270 TYP	
C1	3.800	4.000			

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