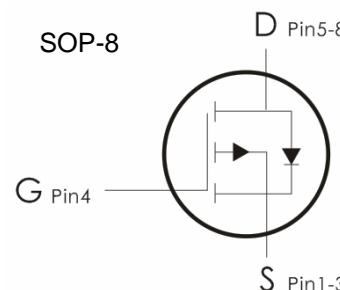
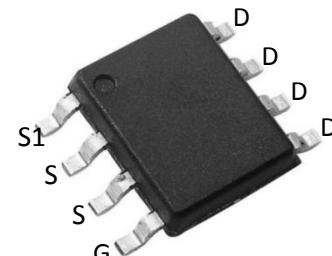


P-Channel 30 V (D-S) MOSFET

Description:

This P-Channel MOSFET uses advanced trench technology and design to provide excellent $R_{DS(on)}$ with low gate charge. It can be used in a wide variety of applications.



Features:

- 1) $V_{DS}=-30V, I_D=-15A, R_{DS(on)}<9.5m\Omega @V_{GS}=-10V$
- 2) Low gate charge.
- 3) Green device available.
- 4) Advanced high cell density trench technology for ultra $R_{DS(on)}$.
- 5) Excellent package for good heat dissipation.

Absolute Maximum Ratings: ($T_c=25^\circ C$ unless otherwise noted)

Symbol	Parameter	Ratings	Units
V_{DS}	Drain-Source Voltage	-30	V
V_{GS}	Gate-Source Voltage	± 20	V
I_D	Continuous Drain Current- $T_C=25^\circ C$	-15	A
	Continuous Drain Current- $T_C=100^\circ C$	-7.8	
	Pulsed Drain Current ¹	-52	
E_{AS}	Single Pulse Avalanche Energy	---	mJ
P_D	Power Dissipation	4.2	W
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	°C

Thermal Characteristics:

Symbol	Parameter	Max	Units
R_{eJC}	Thermal Resistance,Junction to Case	30	°C/W
R_{eJA}	Thermal Resistance,Junction to Ambient	60	

Electrical Characteristics: ($T_C=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{\text{GS}}=0\text{V}, I_D=250 \mu\text{A}$	-30	---	---	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{\text{GS}}=0\text{V}, V_{\text{DS}}=-30\text{V}, T_J=25^\circ\text{C}$	---	---	-1	μA
I_{GSS}	Gate-Source Leakage Current	$V_{\text{GS}}=\pm 20\text{V}, V_{\text{DS}}=0\text{A}$	---	---	± 100	nA
On Characteristics						
$V_{\text{GS}(\text{th})}$	GATE-Source Threshold Voltage	$V_{\text{GS}}=V_{\text{DS}}, I_D=250 \mu\text{A}$	-1.0	-1.6	-2.5	V
$R_{\text{DS}(\text{ON})}$	Drain-Source On Resistance ²	$V_{\text{GS}}=-10\text{V}, I_D=-10\text{A}$	---	8	9.5	$\text{m}\Omega$
		$V_{\text{GS}}=-4.5\text{V}, I_D=-8\text{A}$	---	12.4	15	
G_{FS}	Forward Transconductance	$V_{\text{DS}}=-10\text{V}, I_D=-10\text{A}$	---	13	---	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{\text{DS}}=-15\text{V}, V_{\text{GS}}=0\text{V}, f=1\text{MHz}$	---	3300	4800	pF
C_{oss}	Output Capacitance		---	410	700	
C_{rss}	Reverse Transfer Capacitance		---	280	500	
Switching Characteristics						
$t_{\text{d}(\text{on})}$	Turn-On Delay Time ^{2,3}	$V_{\text{DS}}=-15\text{V}, V_{\text{GS}}=-10\text{V}$ $I_D=-1\text{A}, R_{\text{GEN}}=6\Omega$	---	24.5	38	ns
t_r	Rise Time ^{2,3}		---	10.5	16	ns
$t_{\text{d}(\text{off})}$	Turn-Off Delay Time ^{2,3}		---	156.8	230	ns
t_f	Fall Time ^{2,3}		---	50	75	ns
Q_g	Total Gate Charge ^{2,3}	$V_{\text{DS}}=-15\text{V}, V_{\text{GS}}=-4.5\text{V},$ $I_D=-10\text{A}$	---	35	56	nC
Q_{gs}	Gate-Source Charge ^{2,3}		---	10.8	16	nC
Q_{gd}	Gate-Drain "Miller" Charge ^{2,3}		---	10.6	18	nC
Drain-Source Diode Characteristics						
V_{SD}	Source-Drain Diode Forward Voltage ²	$V_{\text{GS}}=0\text{V}, I_S=-1\text{A}, T_J=25^\circ\text{C}$	---	---	-1	V

Notes:

1. Repetitive Rating : Pulsed width limited by maximum junction temperature.
2. The data tested by pulsed , pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$.
3. Essentially independent of operating temperature.

Typical Characteristics: ($T_c=25^\circ C$ unless otherwise noted)

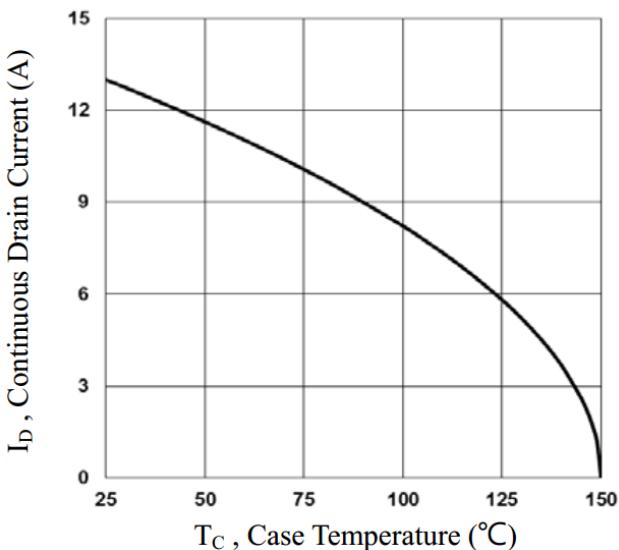


Fig.1 Continuous Drain Current vs. T_c

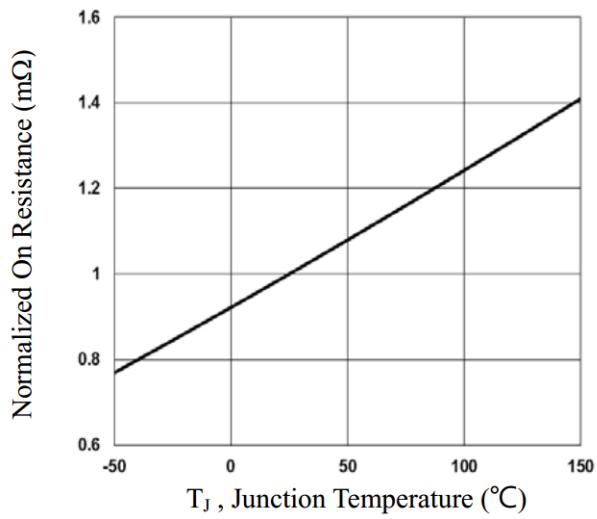


Fig.2 Normalized RDS(on) vs. T_j

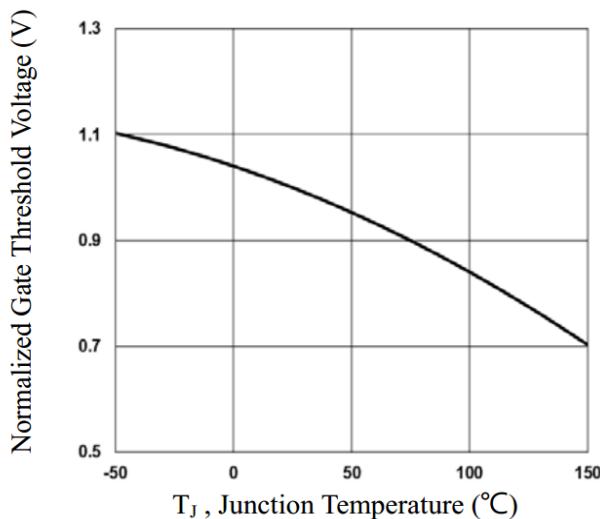


Fig.3 Normalized V_{th} vs. T_j

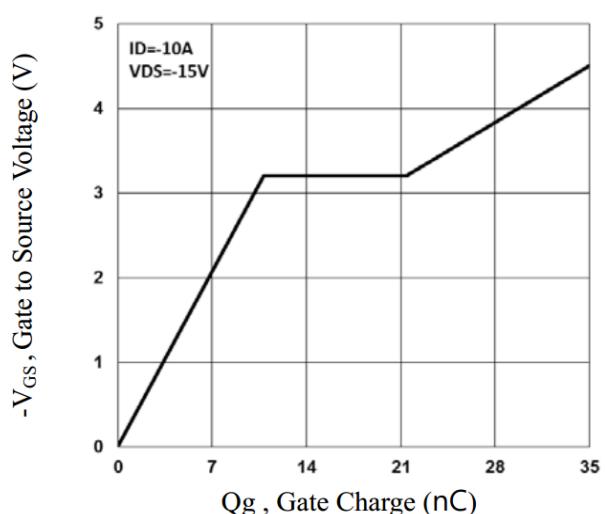


Fig.4 Gate Charge Waveform

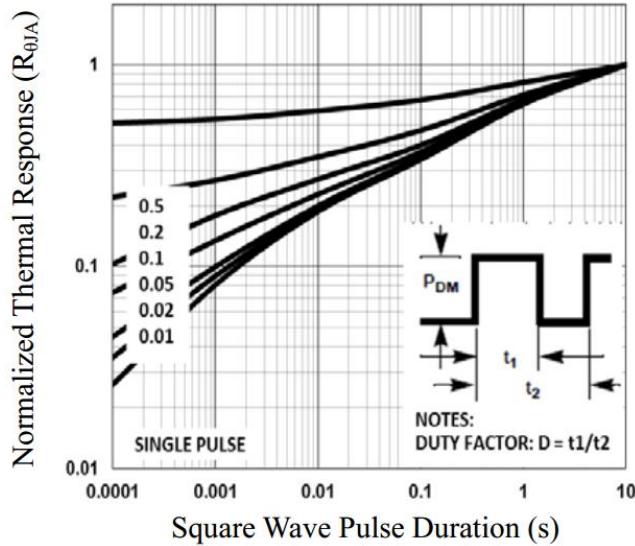


Fig.5 Normalized Transient Impedance

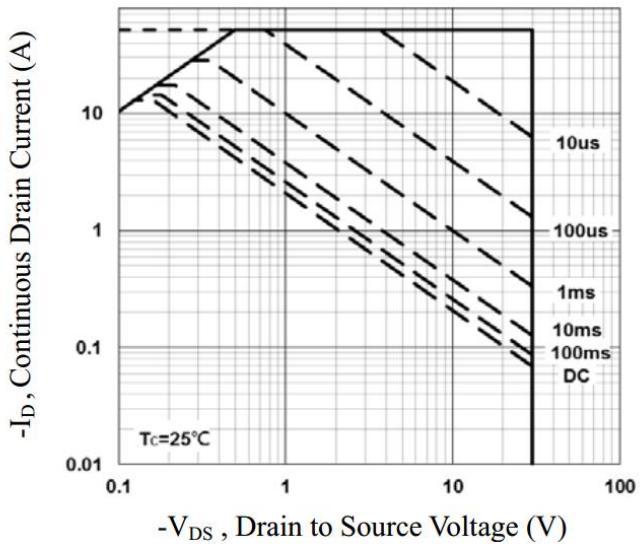


Fig.6 Maximum Safe Operation Area

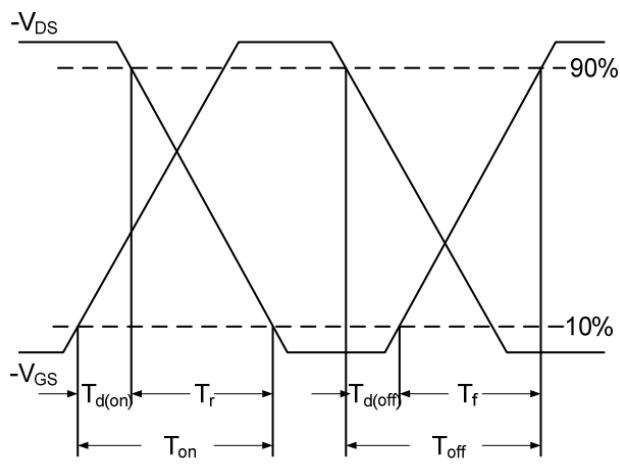


Fig.7 Switching Time Waveform

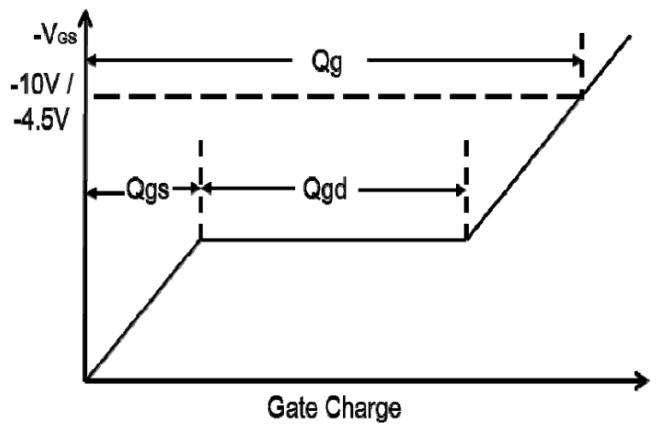
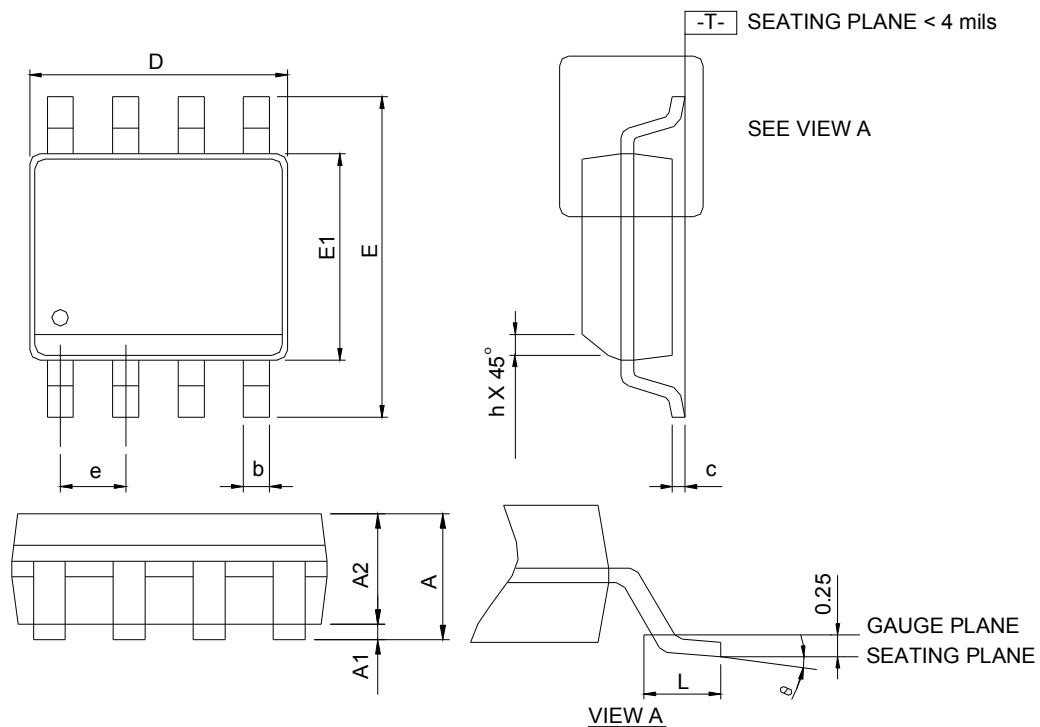


Fig.8 Gate Charge Waveform

Package Information

SOP-8



SYMBOL	SOP-8			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	-	1.75	-	0.069
A1	0.10	0.25	0.004	0.010
A2	1.25	-	0.049	-
b	0.31	0.51	0.012	0.020
c	0.17	0.25	0.007	0.010
D	4.80	5.00	0.189	0.197
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
h	0.25	0.50	0.010	0.020
L	0.40	1.27	0.016	0.050
θ	0°	8°	0°	8°

Note: 1. Follow JEDEC MS-012 AA.

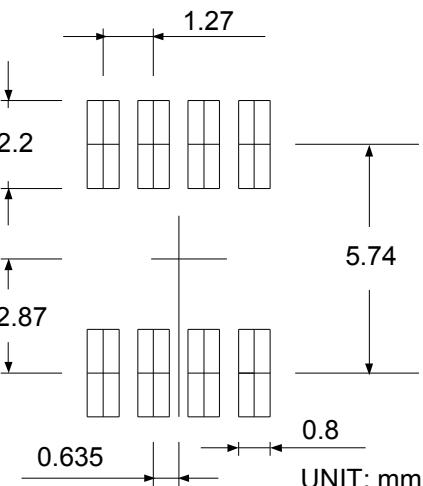
2. Dimension "D" does not include mold flash, protrusions or gate burrs.

Mold flash, protrusion or gate burrs shall not exceed 6 mil per side.

3. Dimension "E" does not include inter-lead flash or protrusions.

Inter-lead flash and protrusions shall not exceed 10 mil per side.

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