High speed CAN transceiver

FEATURES

- High speed (up to 1 MBaud)
- Very low-current standby mode with remote wake-up capability via the bus
- Very low ElectroMagnetic Emission (EME)
- Differential receiver with high common-mode range for ElectroMagnetic Immunity (EMI)
- Transceiver in unpowered state disengages from the bus (zero load)
- Input levels compatible with 3.3 V and 5 V devices
- Voltage source for stabilizing the recessive bus level if split termination is used (further improvement of EME)
- At least 110 nodes can be connected
- Transmit Data (TXD) dominant time-out function
- Bus pins protected against transients in automotive environments
- Bus pins and pin SPLIT short-circuit proof to battery and ground
- Thermally protected.

GENERAL DESCRIPTION

The SL1040 is the interface between the Controller Area Network (CAN) protocol controller and the physical bus. It is primarily intended for high speed applications, up to 1 MBaud, in passenger cars. The device provides differential transmit capability to the bus and differential receive capability to the CAN controller.

The SL1040 is the next step up from the SL1050 high speed CAN transceiver. Being pin compatible and offering the same excellent EMC performance, the SL1040 also features:

- An ideal passive behaviour when supply voltage is off
- A very low-current standby mode with remote wake-up capability via the bus.

This makes the SL1040 an excellent choice in nodes which can be in power-down or standby mode in partially powered networks.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage	operating range	4.75	5.25	V
I_{CC}	supply current	standby mode	5	15	µA
V_{CANH}	DC voltage on pin CANH	$0 < V_{CC} < 5.25$ V; no time limit	–27	+40	V
V_{CANL}	DC voltage on pin CANL	$0 < V_{CC} < 5.25$ V; no time limit	–27	+40	V
V_{SPLIT}	DC voltage on pin SPLIT	$0 < V_{CC} < 5.25$ V; no time limit	–27	+40	V
V_{esd}	electrostatic discharge voltage	Human Body Model (HBM)			
		pins CANH, CANL and SPLIT	–6	+6	kV
		all other pins	–4	+4	kV
$t_{PD(TXD-RXD)}$	propagation delay TXD to RXD	$V_{STB} = 0$ V	40	255	ns
T_{vj}	virtual junction temperature		–40	+150	°C

BLOCK DIAGRAM

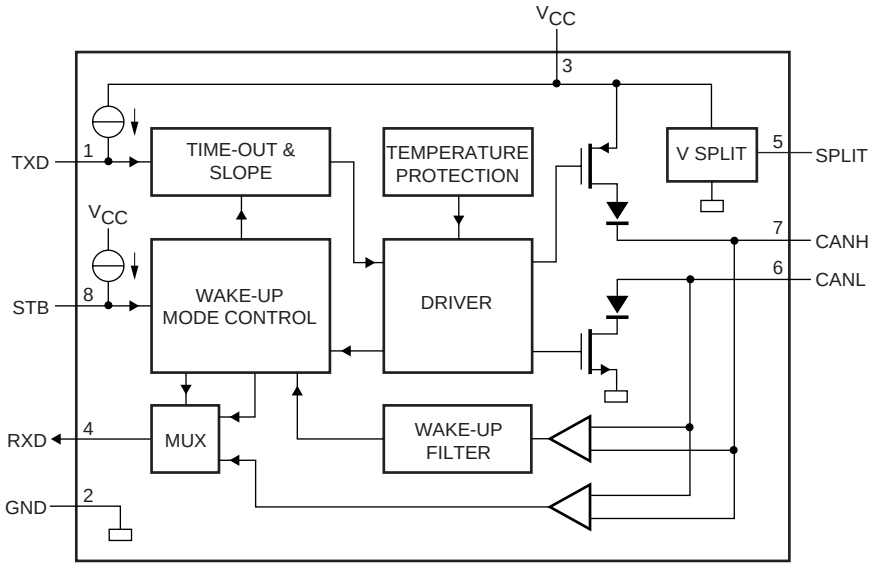


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
TXD	1	transmit data input
GND	2	ground supply
V_{CC}	3	supply voltage
RXD	4	receive data output; reads out data from the bus lines
SPLIT	5	common-mode stabilization output
CANL	6	LOW-level CAN bus line
CANH	7	HIGH-level CAN bus line
STB	8	standby mode control input

SL1040S SOP8

SL1040D DIP8

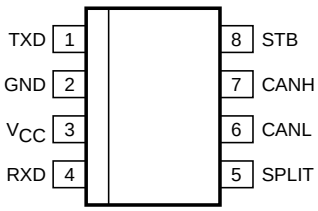


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Operating modes

The SL1040 provides two modes of operation which are selectable via pin STB.

Table 1 Operating modes

MODE	PIN STB	PIN RXD	
		LOW	HIGH
normal	LOW	bus dominant	bus recessive
standby	HIGH	wake-up request detected	no wake-up request detected

NORMAL MODE

In this mode the transceiver is able to transmit and receive data via the bus lines CANH and CANL. See Fig.1 for the block diagram. The differential receiver converts the analog data on the bus lines into digital data which is output to pin RXD via the multiplexer (MUX). The slope of the output signals on the bus lines is fixed and optimized in a way that lowest ElectroMagnetic Emission (EME) is guaranteed.

STANDBY MODE

In this mode the transmitter and receiver are switched off, and the low-power differential receiver will monitor the bus lines. A HIGH level on pin STB activates this low-power receiver and the wake-up filter, and after t_{BUS} the state of the CAN bus is reflected on pin RXD.

The supply current on V_{CC} is reduced to a minimum in such a way that ElectroMagnetic Immunity (EMI) is guaranteed and a wake-up event on the bus lines will be recognized.

In this mode the bus lines are terminated to ground to reduce the supply current (I_{CC}) to a minimum. A diode is added in series with the high-side driver of RXD to prevent a reverse current from RXD to V_{CC} in the unpowered state. In normal mode this diode is bypassed. This diode is not bypassed in standby mode to reduce current consumption.

Split circuit

Pin SPLIT provides a DC stabilized voltage of $0.5V_{CC}$. It is turned on only in normal mode. In standby mode pin SPLIT is floating. The V_{SPLIT} circuit can be used to stabilize the recessive common-mode voltage by connecting pin SPLIT to the centre tap of the split termination (see Fig.4). In case of a recessive bus voltage $<0.5V_{CC}$ due to the presence of an unsupplied transceiver in the network with a significant leakage current from the bus lines to ground, the split circuit will stabilize this recessive voltage to $0.5V_{CC}$. So a start of transmission does not cause a step in the common-mode signal which would lead to poor ElectroMagnetic Emission (EME) behaviour.

Wake-up

In the standby mode the bus lines are monitored via a low-power differential comparator. Once the low-power differential comparator has detected a dominant bus level for more than t_{BUS}, pin RXD will become LOW.

Over-temperature detection

The output drivers are protected against over-temperature conditions. If the virtual junction temperature exceeds the shutdown junction temperature $T_{j(sd)}$, the output drivers will be disabled until the virtual junction temperature becomes lower than $T_{j(sd)}$ and TXD becomes recessive again. By including the TXD condition, the occurrence of output driver oscillation due to temperature drifts is avoided.

TXD dominant time-out function

A 'TXD dominant time-out' timer circuit prevents the bus lines from being driven to a permanent dominant state (blocking all network communication) if pin TXD is forced permanently LOW by a hardware and/or software application failure. The timer is triggered by a negative edge on pin TXD.

If the duration of the LOW level on pin TXD exceeds the internal timer value (t_{dom}), the transmitter is disabled, driving the bus lines into a recessive state. The timer is reset by a positive edge on pin TXD. The TXD dominant time-out time t_{dom} defines the minimum possible bit rate of 40 kBaud.

Fail-safe features

Pin TXD provides a pull-up towards V_{CC} in order to force a recessive level in case pin TXD is unsupplied.

Pin STB provides a pull-up towards V_{CC} in order to force the transceiver into standby mode in case pin STB is unsupplied.

In the event that the V_{CC} is lost, pins TXD, STB and RXD will become floating to prevent reverse supplying conditions via these pins.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage	no time limit	–0.3	+6	V
		operating range	4.75	5.25	V
V_{TXD}	DC voltage on pin TXD		–0.3	V_{CC} + 0.3	V
V_{RXD}	DC voltage on pin RXD		–0.3	V_{CC} + 0.3	V
V_{STB}	DC voltage on pins STB		–0.3	V_{CC} + 0.3	V
V_{CANH}	DC voltage on pin CANH	$0 < V_{CC} < 5.25$ V; no time limit	–27	+40	V
V_{CANL}	DC voltage on pin CANL	$0 < V_{CC} < 5.25$ V; no time limit	–27	+40	V
V_{SPLIT}	DC voltage on pin SPLIT	$0 < V_{CC} < 5.25$ V; no time limit	–27	+40	V
V_{trt}	transient voltages on pins CANH, CANL and SPLIT	according to ISO 7637; see Fig.5	–200	+200	V
V_{esd}	electrostatic discharge voltage	Human Body Model (HBM); note 1			
		pins CANH and CANL and SPLIT	–6	+6	kV
		all other pins	–4	+4	kV
		Machine Model (MM); note 2	–200	+200	V
T_{vj}	virtual junction temperature	note 3	–40	+150	°C
T_{stg}	storage temperature		–55	+150	°C

Notes

1. Equivalent to discharging a 100 pF capacitor via a 1.5 kΩ series resistor.
2. Equivalent to discharging a 200 pF capacitor via a 0.75 µH series inductor and a 10 Ω series resistor.
3. Junction temperature in accordance with IEC 60747-1. An alternative definition of T_{vj} is: $T_{vj} = T_{amb} + P \times R_{th(vj\text{-}amb)}$, where $R_{th(vj\text{-}amb)}$ is a fixed value to be used for the calculating of T_{vj}. The rating for T_{vj} limits the allowable combinations of power dissipation (P) and ambient temperature (T_{amb}).

THERMAL CHARACTERISTICS

In accordance with IEC 60747-1.

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(vj\text{-}a)}$	thermal resistance from virtual junction to ambient in SO8 package	in free air	145	K/W
$R_{th(vj\text{-}s)}$	thermal resistance from virtual junction to substrate of bare die	in free air	50	K/W

CHARACTERISTICS

V_{CC} = 4.75 to 5.25 V, T_{vj} = –40 to +150 °C and R_L = 60 Ω unless specified otherwise; all voltages are defined with respect to ground; positive currents flow into the IC; note 1.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply (pin V_{CC})						
I_{CC}	supply current	standby mode	5	10	15	µA
		normal mode				
		recessive; $V_{TXD} = V_{CC}$	2.5	5	10	mA
		dominant; V_{TXD} = 0 V	30	50	70	mA
Transmit data input (pin TXD)						
V_{IH}	HIGH-level input voltage		2	–	V_{CC} + 0.3	V
V_{IL}	LOW-level input voltage		–0.3	–	+0.8	V
I_{IH}	HIGH-level input current	$V_{TXD} = V_{CC}$	–5	0	+5	µA
I_{IL}	LOW-level input current	normal mode; V_{TXD} = 0 V	–100	–200	–300	µA
C_i	input capacitance	not tested	–	5	10	pF
Standby mode control input (pin STB)						
V_{IH}	HIGH-level input voltage		2	–	V_{CC} + 0.3	V
V_{IL}	LOW-level input voltage		–0.3	–	+0.8	V
I_{IH}	HIGH-level input current	$V_{STB} = V_{CC}$	–	0	–	µA
I_{IL}	LOW-level input current	V_{STB} = 0 V	–1	–4	–10	µA
Receive data output (pin RXD)						
V_{OH}	HIGH-level output voltage	standby mode; I_{RXD} = –100 µA	V_{CC} – 1.1	V_{CC} – 0.7	V_{CC} – 0.4	V
I_{OH}	HIGH-level output current	normal mode; $V_{RXD} = V_{CC}$ – 0.4 V	–0.1	–0.4	–1	mA
I_{OL}	LOW-level output current	V_{RXD} = 0.4 V	2	6	12	mA
Common-mode stabilization output (pin SPLIT)						
V_O	output voltage	normal mode; –500 µA < I_O < +500 µA	$0.3V_{CC}$	$0.5V_{CC}$	$0.7V_{CC}$	V
$\lvert I_L \rvert$	leakage current	standby mode; –22 V < V_{SPLIT} < +35 V	–	0	5	µA
Bus lines (pins CANH and CANL)						
$V_{O(dom)}$	dominant output voltage	V_{TXD} = 0 V				
		pin CANH	3	3.6	4.25	V
		pin CANL	0.5	1.4	1.75	V
$V_{O(dom)(m)}$	matching of dominant output voltage (V_{CC} - V_{CANH} - V_{CANL})		–100	0	+150	mV
$V_{O(dif)(bus)}$	differential bus output voltage (V_{CANH} – V_{CANL})	V_{TXD} = 0 V; dominant; 45 Ω < R_L < 65 Ω	1.5	–	3.0	V
		$V_{TXD} = V_{CC}$; recessive; no load	–50	–	+50	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{O(reces)}$	recessive output voltage	normal mode; $V_{TXD} = V_{CC}$; no load	2	$0.5V_{CC}$	3	V
		standby mode; no load	–0.1	0	+0.1	V
$I_{O(sc)}$	short-circuit output current	V_{TXD} = 0 V				
		pin CANH; V_{CANH} = 0 V	–40	–70	–95	mA
		pin CANL; V_{CANL} = 40 V	40	70	100	mA
$I_{O(reces)}$	recessive output current	–27 V < V_{CAN} < +32 V	–2.5	–	+2.5	mA
$V_{dif(th)}$	differential receiver threshold voltage	–12 V < V_{CANL} < +12 V; –12 V < V_{CANH} < +12 V				
		normal mode (see Fig.6)	0.5	0.7	0.9	V
		standby mode	0.4	0.7	1.15	V
$V_{hys(dif)}$	differential receiver hysteresis voltage	normal mode; –12 V < V_{CANL} < +12 V; –12 V < V_{CANH} < +12 V	50	70	100	mV
I_{LI}	input leakage current	V_{CC} = 0 V; $V_{CANH} = V_{CANL}$ = 5 V	–5	0	+5	µA
$R_{i(cm)}$	common-mode input resistance	standby or normal mode	15	25	35	kΩ
$R_{i(cm)(m)}$	common-mode input resistance matching	$V_{CANH} = V_{CANL}$	–3	0	+3	%
$R_{i(dif)}$	differential input resistance	standby or normal mode	25	50	75	kΩ
$C_{i(cm)}$	common-mode input capacitance	$V_{TXD} = V_{CC}$; not tested	–	–	20	pF
$C_{i(dif)}$	differential input capacitance	$V_{TXD} = V_{CC}$; not tested	–	–	10	pF
Timing characteristics; see Fig.8						
$t_{d(TXD-BUSon)}$	delay TXD to bus active	normal mode	25	70	110	ns
$t_{d(TXD-BUSoff)}$	delay TXD to bus inactive		10	50	95	ns
$t_{d(BUSon-RXD)}$	delay bus active to RXD		15	65	115	ns
$t_{d(BUSoff-RXD)}$	delay bus inactive to RXD		35	100	160	ns
$t_{PD(TXD-RXD)}$	propagation delay TXD to RXD	V_{STB} = 0 V	40	–	255	ns
$t_{dom(TXD)}$	TXD dominant time-out	V_{TXD} = 0 V	300	600	1000	µs
t_{BUS}	dominant time for wake-up via bus	standby mode	0.75	1.75	5	µs
$t_{d(stb-norm)}$	delay standby mode to normal mode	normal mode	5	7.5	10	µs
Thermal shutdown						
$T_{j(sd)}$	shutdown junction temperature		155	165	180	°C

Note

1. All parameters are guaranteed over the virtual junction temperature range by design, but only 100% tested at 125 °C ambient temperature for dies on wafer level, and in addition to this 100% tested at 25 °C ambient temperature for cased products; unless specified otherwise. For bare dies, all parameters are only guaranteed with the backside of the die connected to ground.

APPLICATION AND TEST INFORMATION

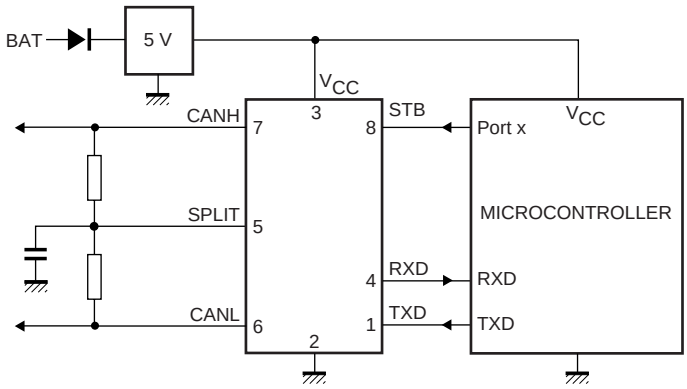


Fig.3 Typical application for 5 V microcontroller.

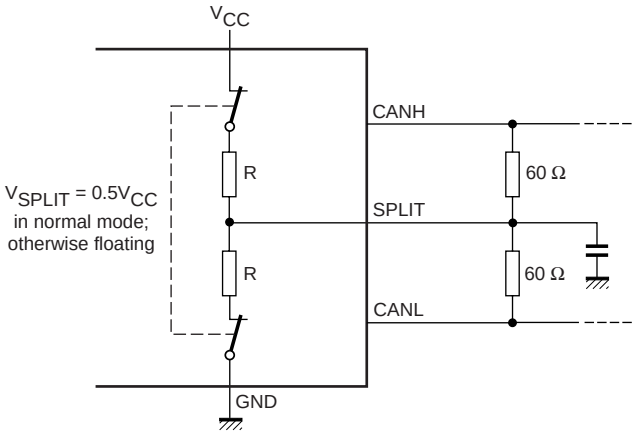


Fig.4 Stabilization circuitry and application.

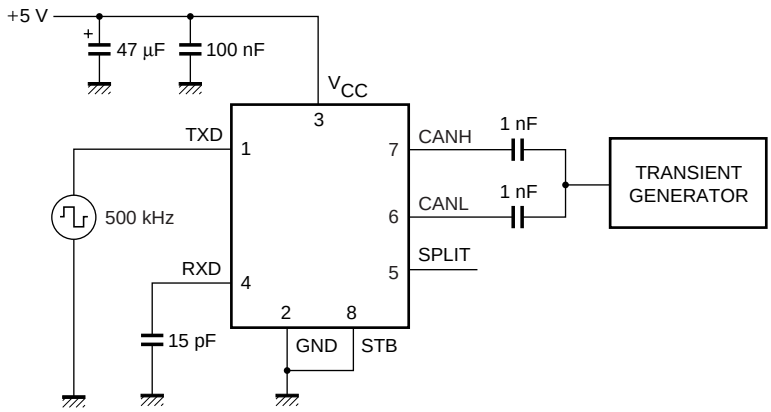


Fig.5 Test circuit for automotive transients.

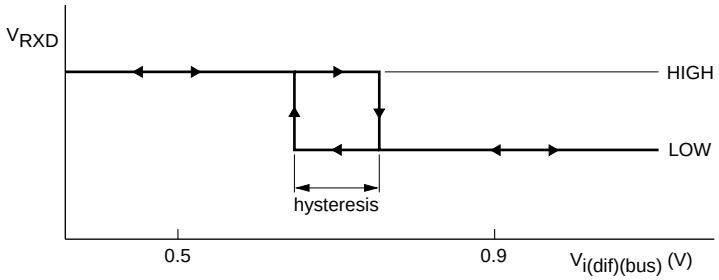


Fig.6 Hysteresis of the receiver.

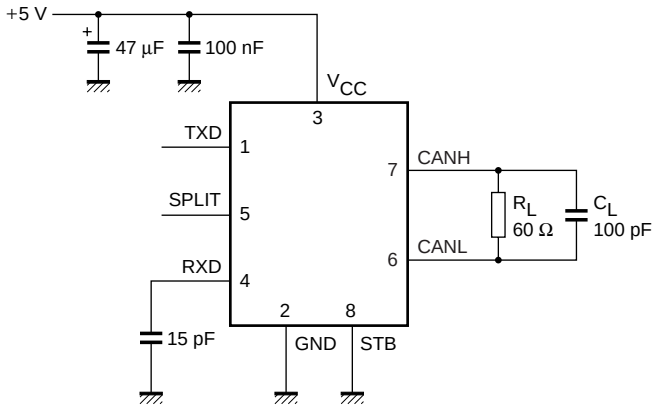
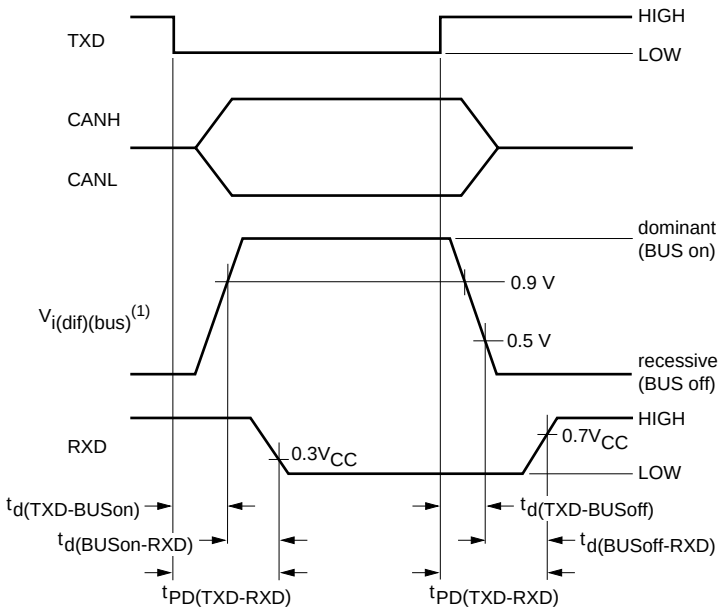


Fig.7 Test circuit for timing characteristics.

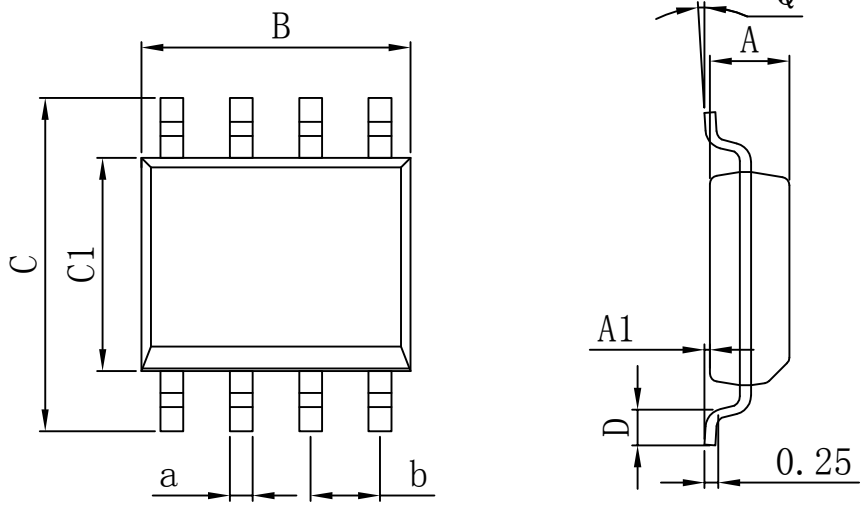


(1) $V_{i(dif)(bus)} = V_{CANH} - V_{CANL}$.

Fig.8 Timing diagram.

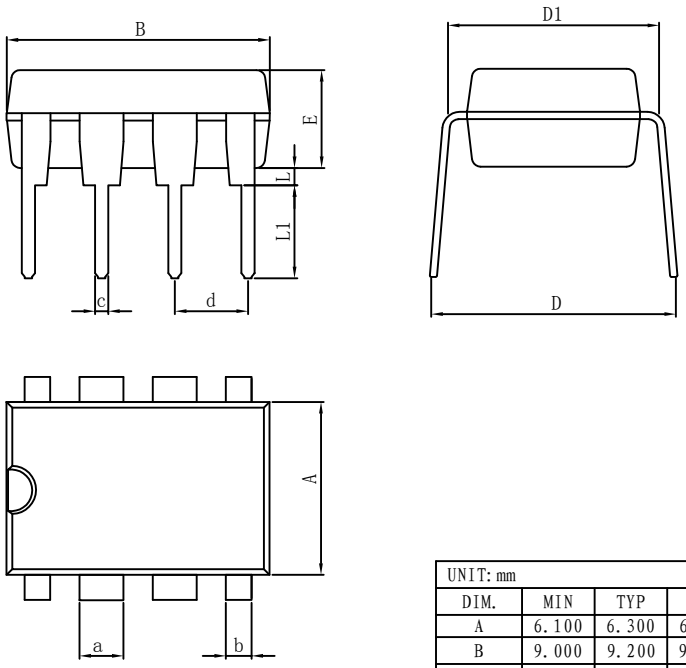
PACKAGE

SOP8



UNIT: mm							
DIM.	MIN	TYP	MAX	DIM.	MIN	TYP	MAX
A	4.520	4.570	4.620	a	0.400	0.420	0.440
A1	0.100	–	0.250	b	1.260	1.270	1.280
B	4.800	4.920	5.100	Q	0°	–	8°
C	5.800	6.100	6.250				
C1	3.800	3.900	4.000				
D	0.400	–	0.950				

DIP8



UNIT: mm							
DIM.	MIN	TYP	MAX	DIM.	MIN	TYP	MAX
A	6.100	6.300	6.680	a	1.504	1.524	1.544
B	9.000	9.200	9.500	b	–	0.889	–
D	8.400	8.700	9.000	c	0.437	0.457	0.477
D1	7.42	7.62	7.82	d	2.530	2.540	2.550
E	3.100	3.300	3.550	L	0.500	–	0.700
				L1	3.000	3.200	3.600

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