

200V Half-Bridge Driver

PRODUCT SUMMARY

- V_{OFFSET} 200 V max.
- $I_{O+/-} \text{ (min.)}$ 130 mA/270 mA
- V_{OUT} 10 V - 20 V
- $t_{on/off} \text{ (typ.)}$ 680 ns/180 ns
- **Deadtime (typ.)** 520 ns

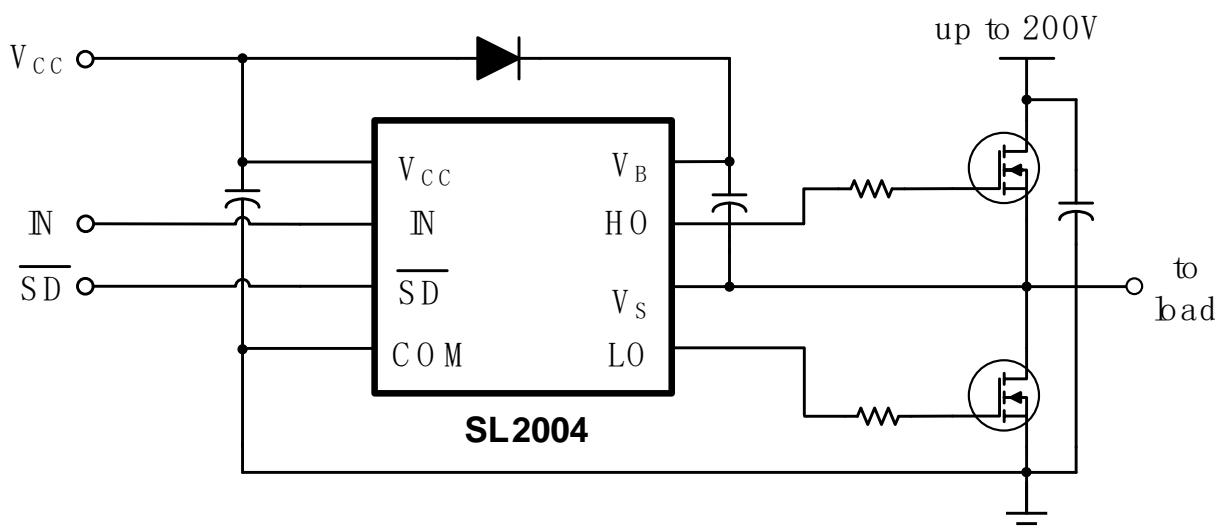
GENERAL DESCRIPTION

The SL2004 is a high voltage, high speed power MOSFET and IGBT drivers with dependent high- and low-side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output, down to 3.3 V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high-side configuration which operates up to 200 V.

FEATURES

- Floating channel designed for bootstrap operation
- Fully operational to +200 V
- Tolerant to negative transient voltage, dV/dt immune
- Gate drive supply range from 10 V to 20 V
- Undervoltage lockout
- 3.3 V, 5 V, and 15 V logic compatible
- Cross-conduction prevention logic
- Matched propagation delay for both channels
- Internal set deadtime
- Shutdown input turns off both channels
- RoHS compliant
- SOP8 package

TYPICAL APPLICATION CIRCUIT



PIN CONFIGURATION

| Package | Pin Configuration (Top View) |
|---------|--|
| SOP8 | <p>The diagram shows an SOP8 package with pin numbers 1 through 8. Pin 1 is labeled V_{CC}, Pin 2 is labeled IN, Pin 3 is labeled \overline{SD}, Pin 4 is labeled COM, Pin 5 is labeled LO, Pin 6 is labeled V_S, Pin 7 is labeled HO, and Pin 8 is labeled V_B.</p> |

PIN DESCRIPTION

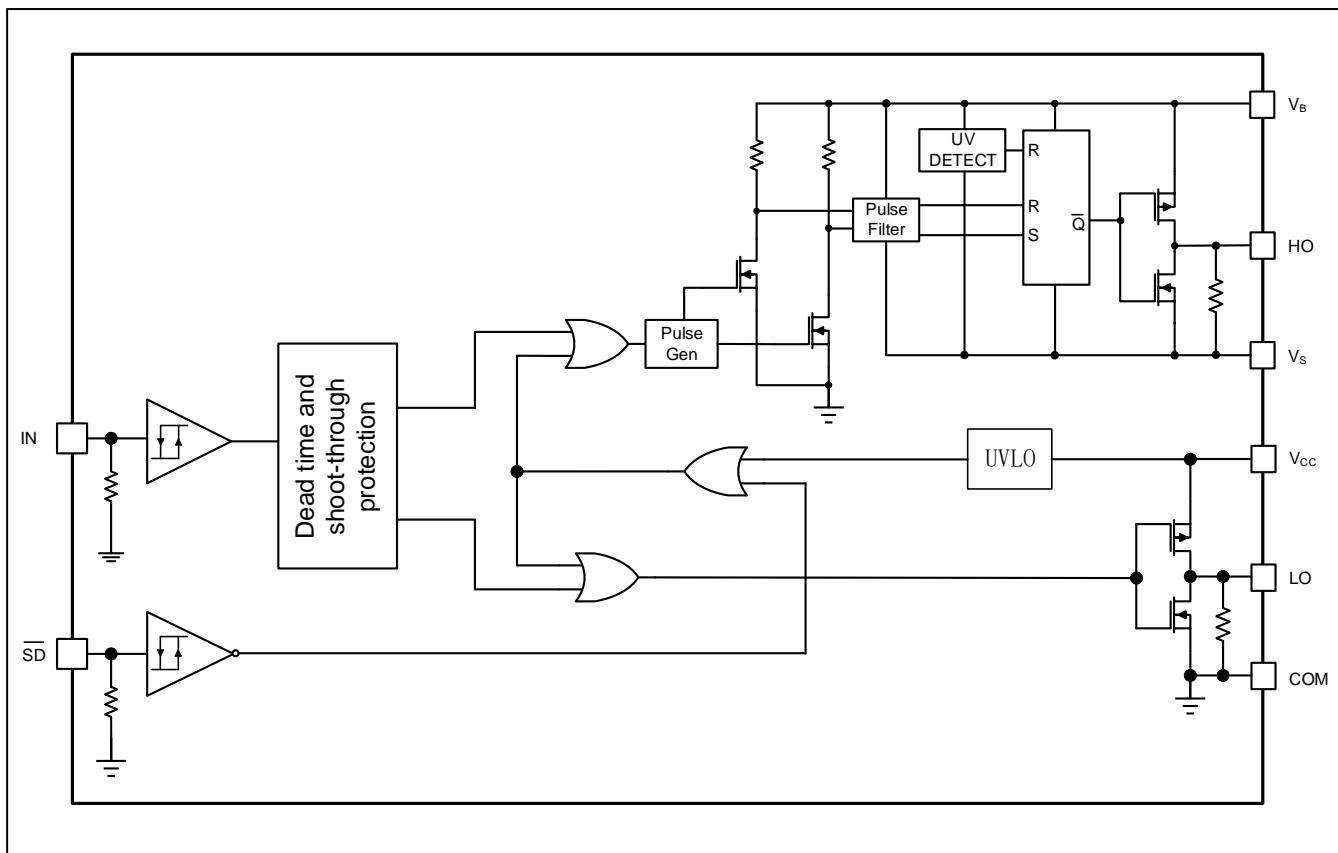
| No. | Pin | Description |
|-----|-----------------|--|
| 1 | V_{CC} | Low-side and logic fixed supply |
| 2 | IN | Logic input for high-side and low-side gate driver outputs (HO and LO), in phase with HO |
| 3 | \overline{SD} | Logic input for shutdown |
| 4 | COM | Low-side return |
| 5 | LO | Low-side gate drive output |
| 6 | V_S | High-side floating supply return |
| 7 | HO | High-side gate drive output |
| 8 | V_B | High-side floating supply |

ORDERING INFORMATION

Industrial Range: -40°C to +125°C

| Order Part No. | Package | QTY |
|----------------|---------------|-----------|
| SL2004 | SOP8, Pb-Free | 2500/Reel |

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

| Symbol | Definition | Min. | Max. | Units |
|---------------|---|-------------|----------------|---------------------------|
| V_B | High-side floating absolute voltage | -0.3 | 225 | V |
| V_s | High-side floating supply offset voltage | $V_B - 25$ | $V_B + 0.3$ | |
| V_{HO} | High-side floating output voltage | $V_s - 0.3$ | $V_B + 0.3$ | |
| V_{CC} | Low-side and logic fixed supply voltage | -0.3 | 25 | |
| V_{LO} | Low-side output voltage | -0.3 | $V_{CC} + 0.3$ | |
| V_{IN} | Logic input voltage (IN & \overline{SD}) | -0.3 | $V_{CC} + 0.3$ | |
| dV_s/dt | Allowable offset supply voltage transient | --- | 50 | V/ns |
| P_D | Package power dissipation @ $T_A \leq 25^\circ\text{C}$ | --- | 0.625 | W |
| θ_{JA} | Thermal resistance, junction to ambient | --- | 200 | $^\circ\text{C}/\text{W}$ |
| T_J | Junction temperature | --- | 150 | $^\circ\text{C}$ |
| T_S | Storage temperature | -55 | 150 | |
| T_L | Lead temperature (soldering, 10 seconds) | --- | 300 | |

Note: Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

RECOMMENDED OPERATION CONDITIONS

| Symbol | Definition | Min. | Max. | Units |
|----------|---|------------|------------|------------------|
| V_B | High-side floating absolute voltage | $V_s + 10$ | $V_s + 20$ | V |
| V_s | High-side floating supply offset voltage | | 200 | |
| V_{HO} | High-side floating output voltage | V_s | V_B | |
| V_{CC} | Low-side and logic fixed supply voltage | 10 | 20 | |
| V_{LO} | Low-side output voltage | 0 | V_{CC} | |
| V_{IN} | Logic input voltage (IN & \overline{SD}) | 0 | V_{CC} | |
| T_A | Ambient temperature | -40 | 125 | $^\circ\text{C}$ |

Note: The input/output logic timing diagram is shown in Figure 1. For proper operation the device should be used within the recommended conditions. The V_s offset rating is tested with all supplies biased at a 15 V differential.

DYNAMIC ELECTRICAL CHARACTERISTICS

V_{BIAS} (V_{CC} , V_{BS}) = 15 V, $C_L = 1000 \text{ pF}$ and $T_A = 25^\circ\text{C}$ unless otherwise specified.

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|-----------|---|---------------------|------|------|------|------|
| t_{on} | Turn-on propagation delay | $V_s = 0 \text{ V}$ | --- | 680 | 820 | ns |
| t_{off} | Turn-off propagation delay | $V_s = 0 \text{ V}$ | --- | 180 | 280 | |
| t_{sd} | Shutdown propagation delay | | --- | 220 | 300 | |
| t_r | Turn-on rise time | | --- | 70 | 170 | |
| t_f | Turn-off fall time | | --- | 25 | 90 | |
| DT | Deadtime, LS turn-off to HS turn-on & HS turn-on to LS turn-off | | 400 | 520 | 650 | |

STATIC ELECTRICAL CHARACTERISTICS

V_{BIAS} (V_{CC} , V_{BS}) = 15 V and $T_A = 25^\circ\text{C}$ unless otherwise specified. The V_{IN} , V_{TH} , and I_{IN} parameters are referenced to COM and are applicable to all logic input leads: IN and SD. The V_o and I_o parameters are referenced to COM and are applicable to the respective output leads: HO or LO.

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|----------------------------|--|--|------|------|------|---------------|
| V_{IH} | Logic "1" input voltage | $V_{CC} = 10 \text{ V to } 20 \text{ V}$ | 2.5 | --- | --- | V |
| V_{IL} | Logic "0" input voltage | | --- | --- | 0.8 | |
| $V_{SD}, TH+$ | SD input positive going threshold | | 2.5 | --- | --- | |
| $V_{SD}, TH-$ | SD input negative going threshold | | --- | --- | 0.8 | |
| V_{OH} | High level output voltage, $V_{BIAS} - V_o$ | $I_o = 20 \text{ mA}$ | --- | 0.45 | 0.6 | μA |
| V_{OL} | Low level output voltage, V_o | | --- | 0.15 | 0.2 | |
| I_{LK} | Offset supply leakage current | $V_B = V_s = 200 \text{ V}$ | --- | --- | 50 | |
| I_{QBS} | Quiescent V_{BS} supply current | $V_{IN} = 0 \text{ V}$ | --- | 60 | 78 | |
| I_{QCC} | Quiescent V_{CC} supply current | | --- | 220 | 280 | |
| I_{IN+} | Logic "1" input bias current | $V_{IN} = 5 \text{ V}$ | --- | 8 | 15 | |
| I_{IN-} | Logic "0" input bias current | $V_{IN} = 0 \text{ V}$ | --- | --- | 5 | |
| V_{CCUV+} V_{BSUV+} | V_{CC} and V_{BS} supply undervoltage positive going threshold | | 8 | 8.9 | 9.8 | V |
| V_{CCUV-} V_{BSUV-} | V_{CC} and V_{BS} supply undervoltage negative going threshold | | 7.4 | 8.2 | 9 | V |

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|----------|--|---|------|------|------|------|
| I_{O+} | Output high short circuit pulsed current | $V_O = 0 \text{ V}, V_{IN} = V_{IH}$ $PW \leq 10 \mu\text{s}$ | 130 | 290 | | mA |
| I_{O-} | Output low short circuit pulsed current | $V_O = 15 \text{ V}, V_{IN} = V_{IL}$ $PW \leq 10 \mu\text{s}$ | 270 | 600 | | |

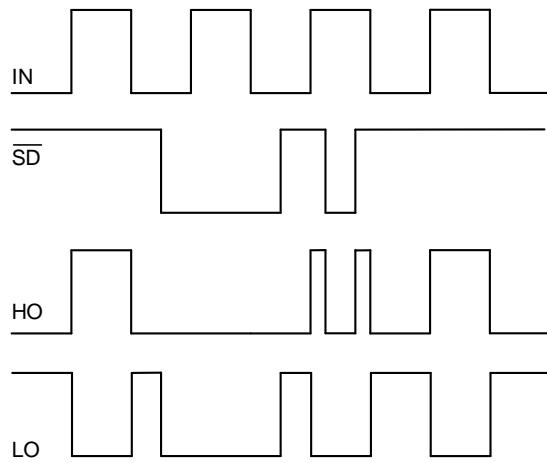


Figure 1. Input/Output Timing Diagram

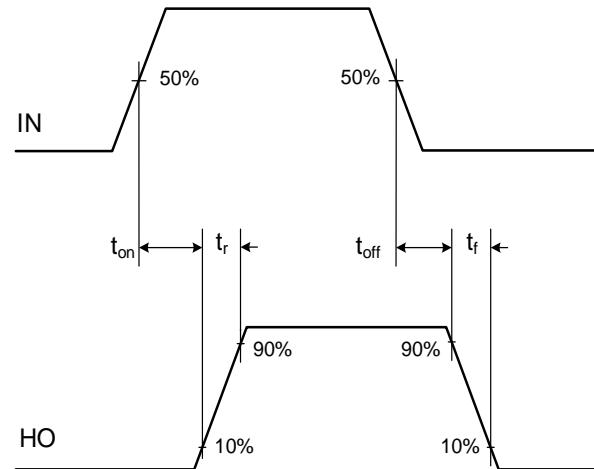


Figure 2. High Side Switching Time Waveform

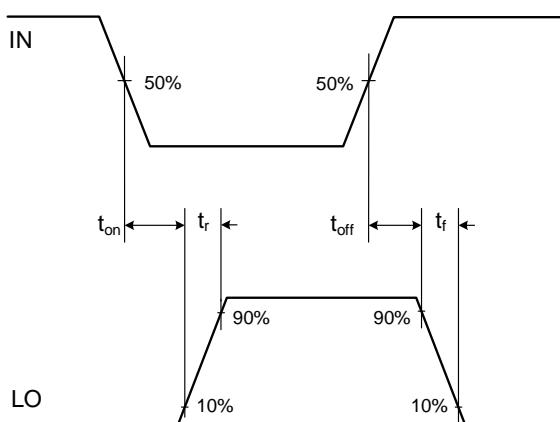


Figure 3. Low Side Switching Time Waveform

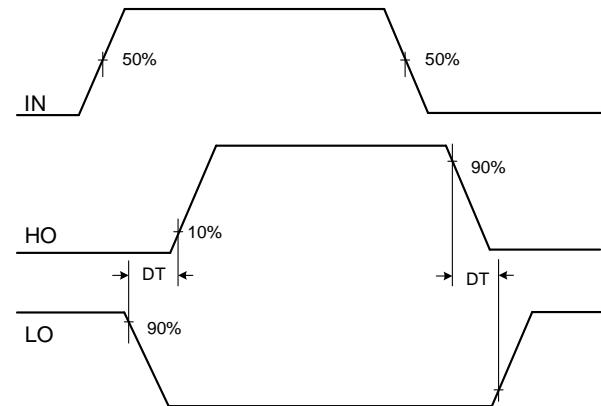


Figure 4. Dead Time Waveform

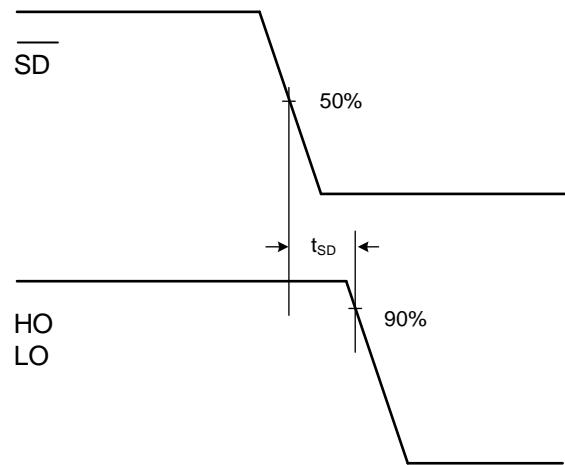


Figure 5. Shutdown Time Waveform

PACKAGE CASE OUTLINES

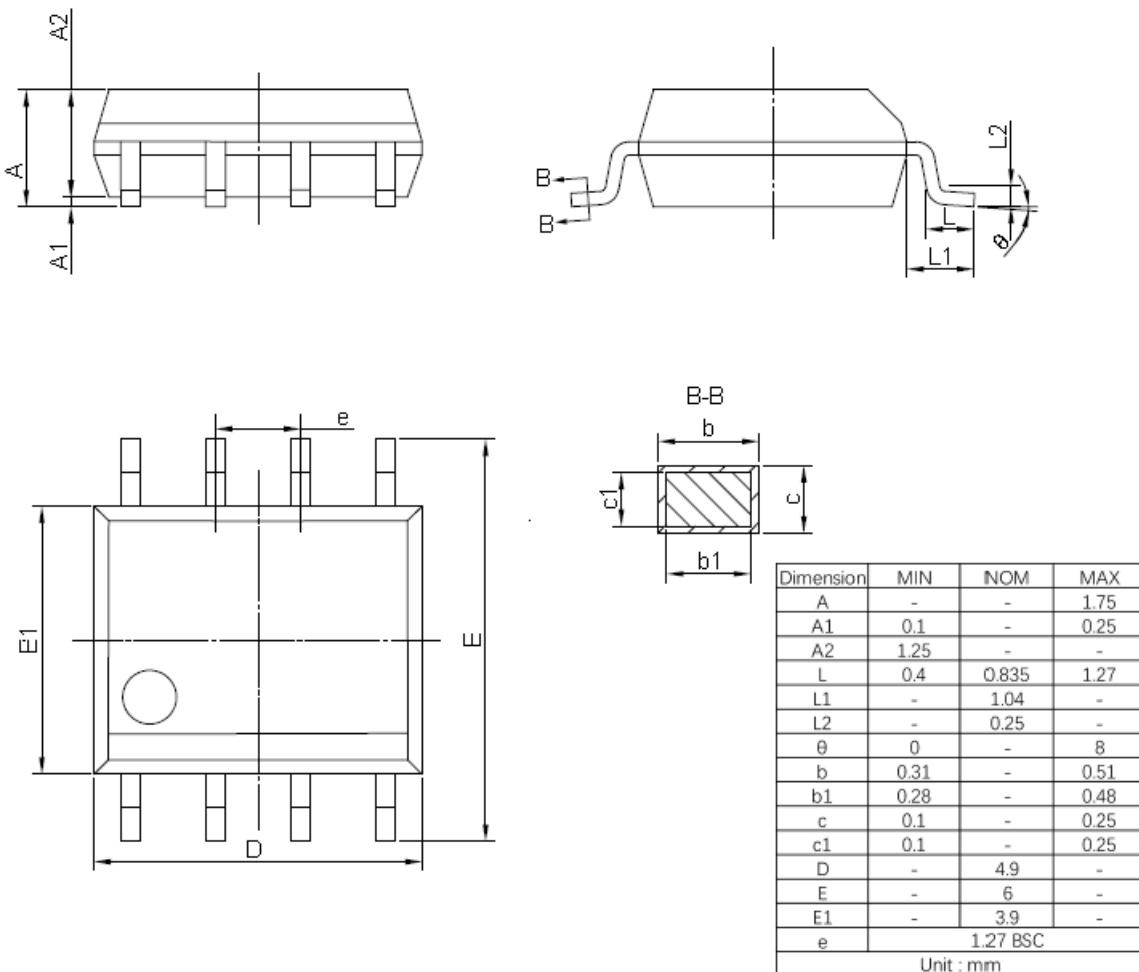


Figure 6. SOP8 Outline Dimensions

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