

# 600V Half-Bridge Driver

## PRODUCT SUMMARY

- $V_{\text{OFFSET}}$  600 V max.
- $I_{\text{O+/-}}$  130 mA/270 mA
- $V_{\text{OUT}}$  10 V - 20 V
- $t_{\text{on/off (typ.)}}$  680 ns/150 ns
- **Deadtime (typ.)** 520 ns

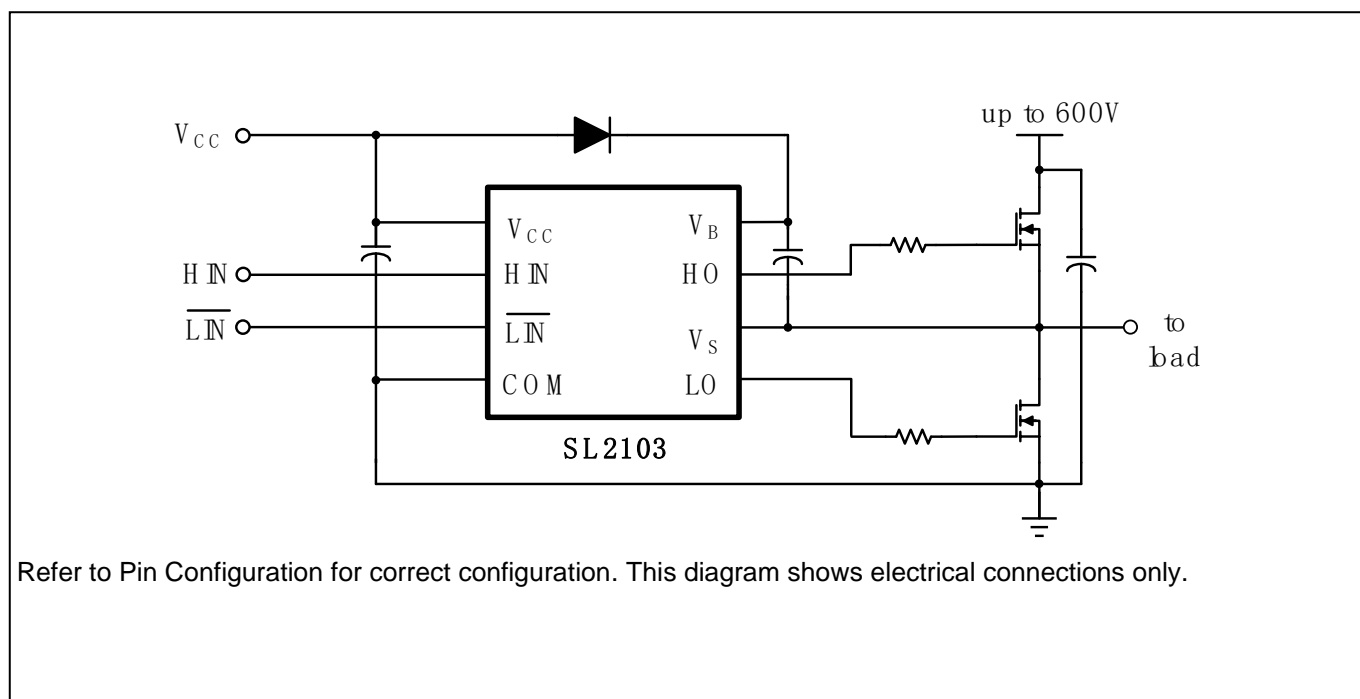
## GENERAL DESCRIPTION

The SL2103 is a high voltage, high speed power MOSFET and IGBT drivers with dependent high- and low-side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output, down to 3.3 V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high-side configuration which operates up to 600 V.

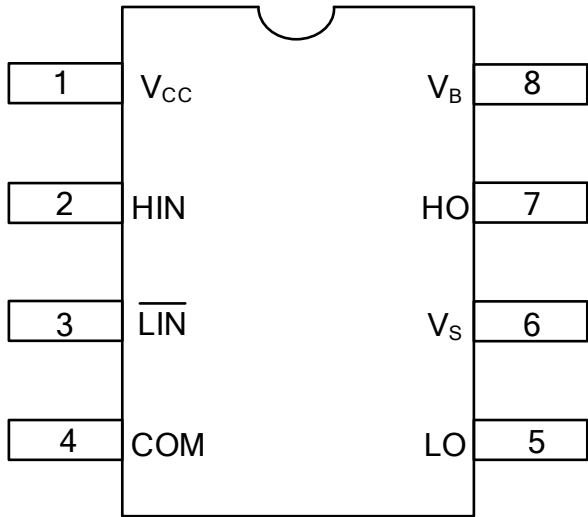
## FEATURES

- Floating channel designed for bootstrap operation
- Fully operational to +600 V
- Tolerant to negative transient voltage,  $dV/dt$  immune
- Gate drive supply range from 10 V to 20 V
- Undervoltage lockout
- 3.3 V, 5 V, and 15 V logic compatible
- Cross-conduction prevention logic
- Matched propagation delay for both channels
- Internal set deadtime
- High-side output in phase with  $\overline{\text{HIN}}$  input
- Low-side output out of phase with  $\overline{\text{LIN}}$  input
- RoHS compliant
- SOP8 package

## TYPICAL APPLICATION CIRCUIT



## PIN CONFIGURATION

Package	Pin Configuration (Top View)
SOP8	

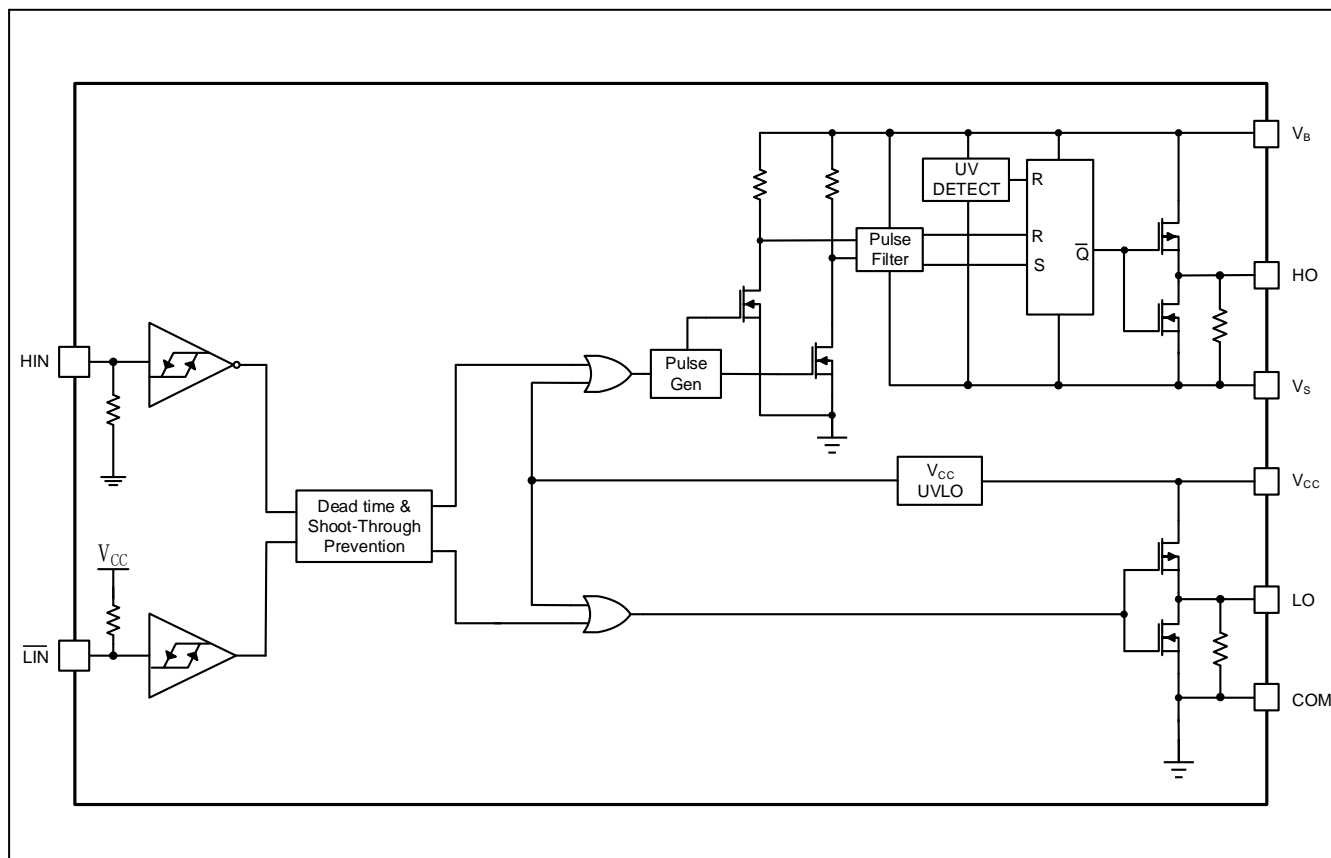
## PIN DESCRIPTION

No.	Pin	Description
1	V <sub>CC</sub>	Low-side and logic fixed supply
2	HIN	Logic input for high-side gate driver output (HO), in phase
3	$\overline{\text{LIN}}$	Logic input for low-side gate driver output (LO), out of phase
4	COM	Low-side return
5	LO	Low-side gate drive output
6	V <sub>S</sub>	High-side floating supply return
7	HO	High-side gate drive output
8	V <sub>B</sub>	High-side floating supply

## ORDERING INFORMATION

Industrial Range: -40°C to +125°C

Order Part No.	Package	QTY
SL2103	SOP8, Pb-Free	2500/Reel

**FUNCTIONAL BLOCK DIAGRAM**


## ABSOLUTE MAXIMUM RATINGS

Symbol	Definition	Min.	Max.	Units
V <sub>B</sub>	High-side floating absolute voltage	-0.3	625	V
V <sub>S</sub>	High-side floating supply offset voltage	V <sub>B</sub> - 25	V <sub>B</sub> + 0.3	
V <sub>HO</sub>	High-side floating output voltage	V <sub>S</sub> - 0.3	V <sub>B</sub> + 0.3	
V <sub>CC</sub>	Low-side and logic fixed supply voltage	-0.3	25	
V <sub>LO</sub>	Low-side output voltage	-0.3	V <sub>CC</sub> + 0.3	
V <sub>IN</sub>	Logic input voltage (HIN & $\overline{\text{LIN}}$ )	-0.3	V <sub>CC</sub> + 0.3	
dV <sub>S</sub> /dt	Allowable offset supply voltage transient	---	50	V/ns
P <sub>D</sub>	Package power dissipation @ T <sub>A</sub> ≤ +25°C	---	0.625	W
θ <sub>JA</sub>	Thermal resistance, junction to ambient	---	200	°C/W
T <sub>J</sub>	Junction temperature	---	150	°C
T <sub>S</sub>	Storage temperature	-55	150	
T <sub>L</sub>	Lead temperature (soldering, 10 seconds)	---	300	

Note: Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

## RECOMMENDED OPERATION CONDITIONS

Symbol	Definition	Min.	Max.	Units
V <sub>B</sub>	High-side floating absolute voltage	V <sub>S</sub> + 10	V <sub>S</sub> + 20	V
V <sub>S</sub>	High-side floating supply offset voltage		600	
V <sub>HO</sub>	High-side floating output voltage	V <sub>S</sub>	V <sub>B</sub>	
V <sub>CC</sub>	Low-side and logic fixed supply voltage	10	20	
V <sub>LO</sub>	Low-side output voltage	0	V <sub>CC</sub>	
V <sub>IN</sub>	Logic input voltage (HIN & $\overline{\text{LIN}}$ )	0	V <sub>CC</sub>	
T <sub>A</sub>	Ambient temperature	- 40	125	°C

Note: The input/output logic timing diagram is shown in Figure 1. For proper operation the device should be used within the recommended conditions. The V<sub>S</sub> offset rating is tested with all supplies biased at a 15 V differential.

## DYNAMIC ELECTRICAL CHARACTERISTICS

$V_{BIAS}$  ( $V_{CC}$ ,  $V_{BS}$ ) = 15 V,  $C_L$  = 1000 pF and  $T_A$  = 25°C unless otherwise specified.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
$t_{on}$	Turn-on propagation delay	$V_S = 0$ V	---	680	820	ns
$t_{off}$	Turn-off propagation delay	$V_S = 0$ V	---	150	220	
$t_r$	Turn-on rise time		---	70	170	
$t_f$	Turn-off fall time		---	35	90	
DT	Deadtime, LS turn-off to HS turn-on & HS turn-on to LS turn-off		400	520	750	
MT	Delay matching, HS & LS turn-on/off		---	---	60	

## STATIC ELECTRICAL CHARACTERISTICS

$V_{BIAS}$  ( $V_{CC}$ ,  $V_{BS}$ ) = 15 V and  $T_A$  = 25°C unless otherwise specified. The  $V_{IN}$ ,  $V_{TH}$ , and  $I_{IN}$  parameters are referenced to COM. The  $V_O$  and  $I_O$  parameters are referenced to COM and are applicable to the respective output leads: HO or LO.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
$V_{IH}$	Logic "1" (HIN) & Logic "0" ( $\overline{LIN}$ ) input voltage	$V_{CC} = 10$ V to 20V	2.5	---	---	V
$V_{IL}$	Logic "0" (HIN) & Logic "1" ( $\overline{LIN}$ ) input voltage		---	---	0.8	
$V_{OH}$	High level output voltage, $V_{BIAS} - V_O$	$I_O = 2$ mA	---	0.05	0.2	
$V_{OL}$	Low level output voltage, $V_O$		---	0.02	0.1	
$I_{LK}$	Offset supply leakage current	$V_B = V_S = 600$ V	---	---	50	$\mu$ A
$I_{QBS}$	Quiescent $V_{BS}$ supply current	$V_{IN} = 0$ V	---	60	75	
$I_{QCC}$	Quiescent $V_{CC}$ supply current		---	220	280	
$I_{IN+}$	Logic "1" input bias current	$HIN = 5$ V, $\overline{LIN} = 0$ V	---	8	15	
$I_{IN-}$	Logic "0" input bias current	$HIN = 0$ V, $\overline{LIN} = 5$ V	---	---	5	
$V_{CCUV+}$ $V_{BSUV+}$	$V_{CC}$ and $V_{BS}$ supply undervoltage positive going threshold		8	8.9	9.8	V
$V_{CCUV-}$ $V_{BSUV-}$	$V_{CC}$ and $V_{BS}$ supply undervoltage negative going threshold		7.4	8.2	9	

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
$I_{O+}$	Output high short circuit pulsed current	$V_O = 0\text{ V}, V_{IN} = V_{IH}$ $PW \leq 10\ \mu\text{s}$	130	290		mA
$I_{O-}$	Output low short circuit pulsed current	$V_O = 15\text{ V}, V_{IN} = V_{IL}$ $PW \leq 10\ \mu\text{s}$	270	600		

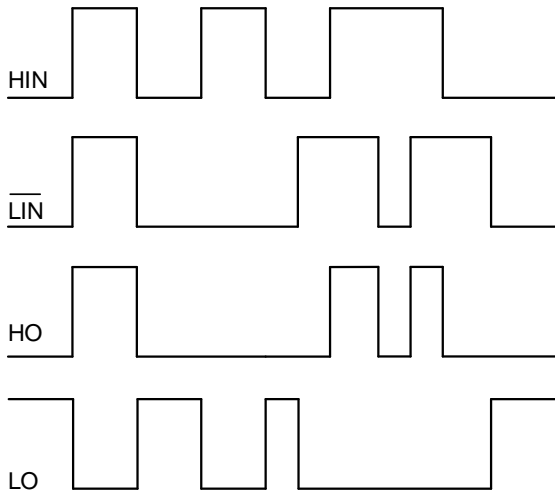


Figure 1. Input/Output Timing Diagram

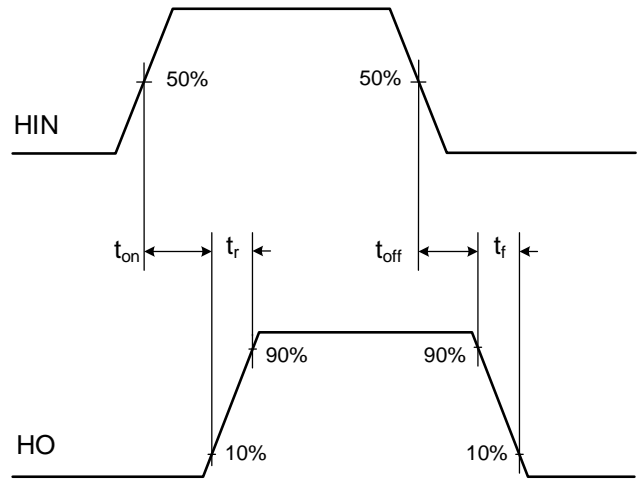


Figure 2. High Side Switching Time Waveform

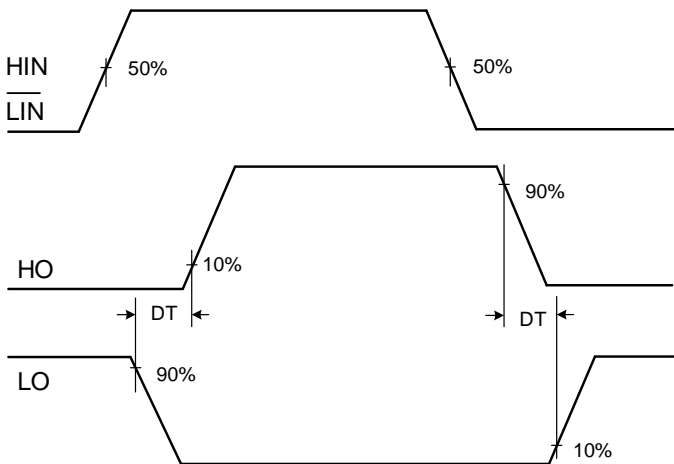


Figure 3. Dead Time Waveform

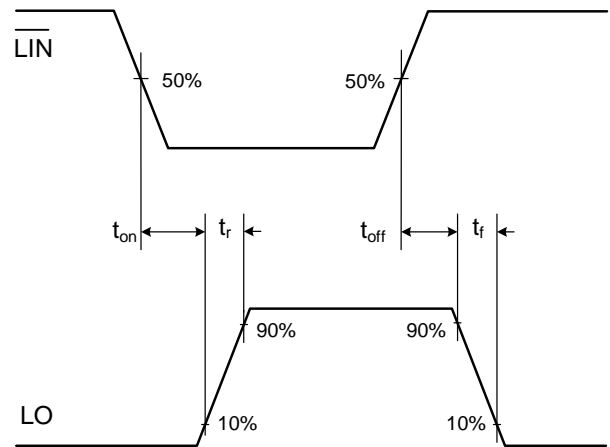


Figure 4. Low Side Switching Time Waveform

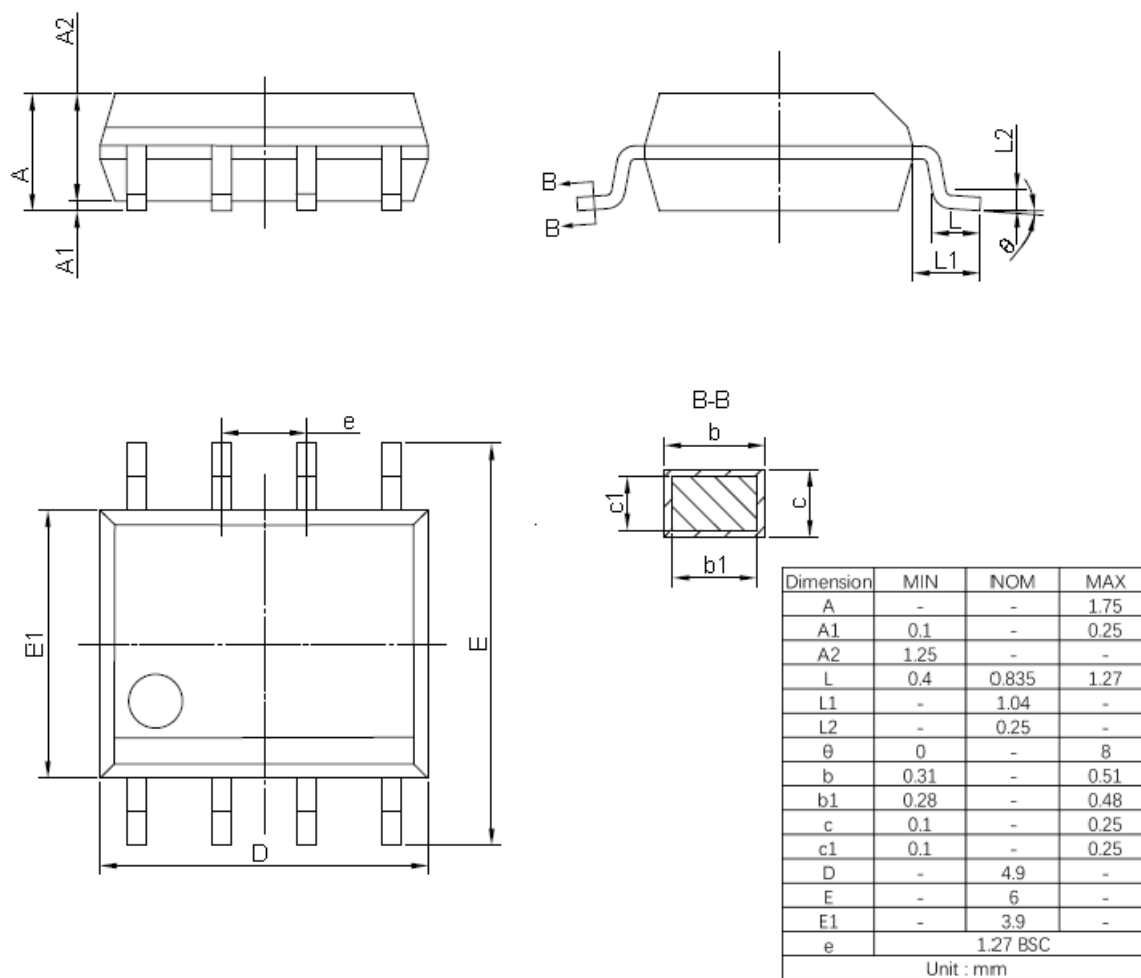
**PACKAGE CASE OUTLINES**


Figure 5. SOP8 Outline Dimensions

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