

20V N-Channel Enhancement Mode MOSFET

■ DESCRIPTION

The SL2314 is the N-Channel logic enhancement mode power field effect transistor is produced using high cell density advanced trench technology..

This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application, and low in-line power loss are needed in a very small outline surface mount package.

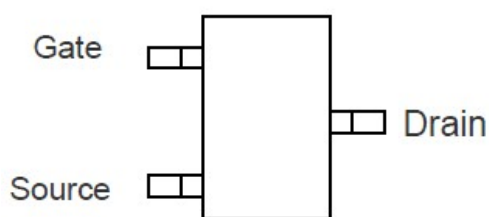
■ FEATURE

- ◆ 20V/4.5A, $R_{DS(ON)}=25m\Omega$ (typ.)@ $V_{GS}=4.5V$
- ◆ 20V/2.5A, $R_{DS(ON)}=55m\Omega$ (typ.)@ $V_{GS}=2.5V$
- ◆ 20V/2.0A, $R_{DS(ON)}=80m\Omega$ (typ.)@ $V_{GS}=1.8V$
- ◆ Super high design for extremely low $R_{DS(ON)}$
- ◆ Exceptional on-resistance and Maximum DC current capability
- ◆ Full RoHS compliance
- ◆ SOT23-3L package design

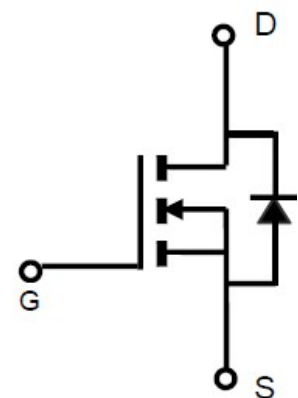
■ APPLICATIONS

- ◆ Power Management
- ◆ Portable Equipment
- ◆ DC/DC Converter
- ◆ Load Switch
- ◆ DSC
- ◆ LCD Display inverter

■ PIN CONFIGURATION



TOP VIEW
SOT-23-3L



N-Channel

■ **ABSOLUTE MAXIMUM RATINGS** ($T_A = 25^\circ\text{C}$ Unless otherwise noted)

Symbol	Parameter	Typical	Unit
V_{DSS}	Drain-Source Voltage	20	V
V_{GSS}	Gate-Source Voltage	± 10	V
I_D	Continuous Drain Current ($T_C=25^\circ\text{C}$)	4.5	A
	Continuous Drain Current ($T_C=70^\circ\text{C}$)		
I_{DM}	Pulsed Drain Current	20	A
I_S	Continuous Source Current (Diode Conduction)	1.5	A
P_D	Power Dissipation	$T_A=25^\circ\text{C}$	W
		$T_A=70^\circ\text{C}$	
T_J	Operation Junction Temperature	150	$^\circ\text{C}$
T_{STG}	Storage Temperature Range	-55~+150	$^\circ\text{C}$
$R_{\theta JA}$	Thermal Resistance Junction to Ambient	90	$^\circ\text{C/W}$

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress rating only and functional device operation is not implied

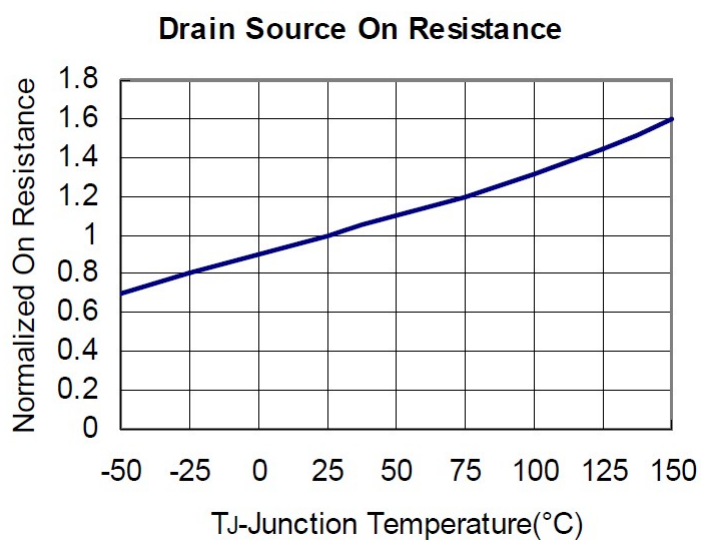
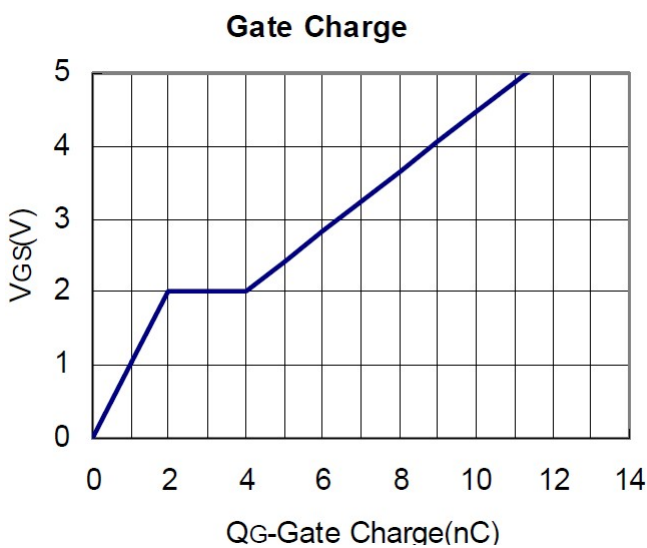
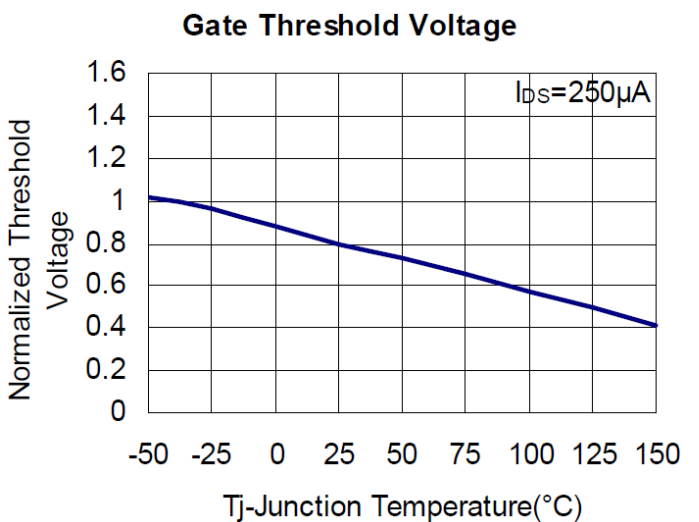
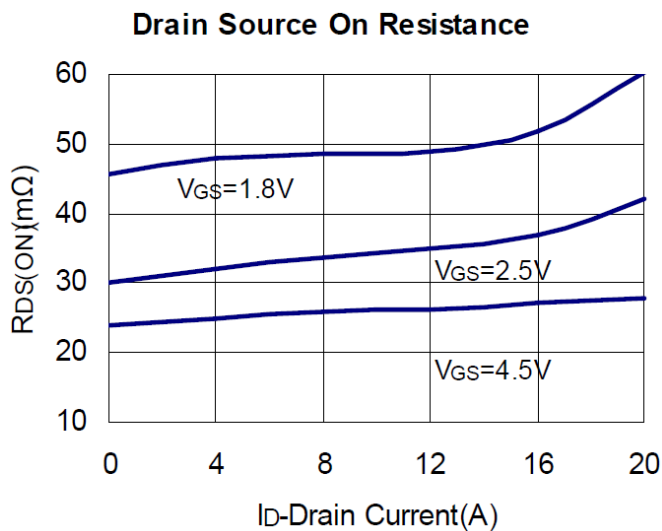
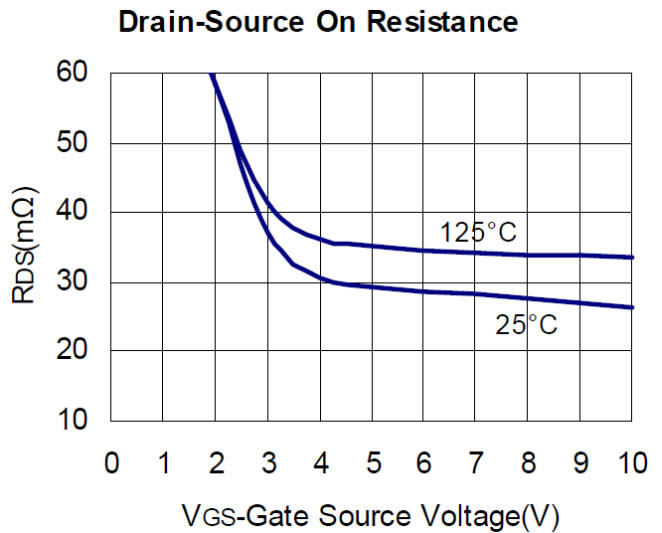
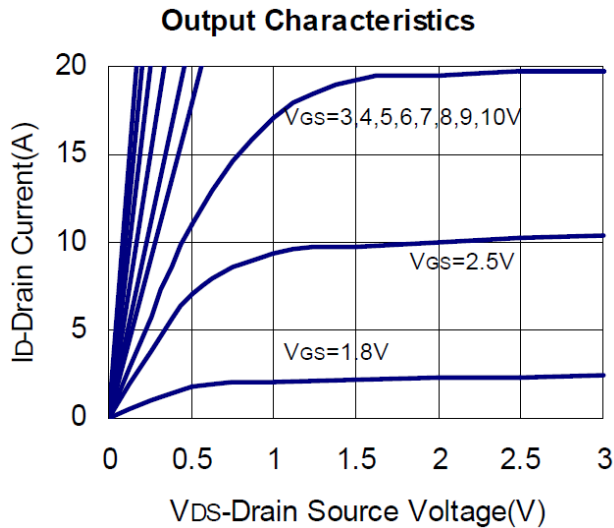
■ ELECTRICAL CHARACTERISTICS ($T_A=25^\circ\text{C}$ Unless otherwise noted)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Static Parameters						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	20			V
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	0.5		1.0	V
I_{GSS}	Gate Leakage Current	$V_{DS}=0V, V_{GS}=\pm 12V$			± 100	nA
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=20V, V_{GS}=0$			1	uA
		$V_{DS}=20V, V_{GS}=0$ $T_J=55^\circ\text{C}$			5	
$R_{DS(ON)}$	Drain-Source On-Resistance	$V_{GS}=4.5V, I_D=3.0A$		25	45	m Ω
		$V_{GS}=2.5V, I_D=2.5A$		40	60	
		$V_{GS}=1.8V, I_D=2.0A$		65	90	
Source-Drain Diode						
V_{SD}	Diode Forward Voltage	$I_S=1.7A, V_{GS}=0V$		0.78	1.2	V
Dynamic Parameters						
Q_g	Total Gate Charge	$V_{DS}=10V$ $V_{GS}=4.5V$ $I_D=5.0A$		11	13	nC
Q_{gs}	Gate-Source Charge			1.45		
Q_{gd}	Gate-Drain Charge			2.3		
C_{iss}	Input Capacitance	$V_{DS}=10V$ $V_{GS}=0V$ $f=1\text{MHz}$		578		pF
C_{oss}	Output Capacitance			116		
C_{rss}	Reverse Transfer Capacitance			96		
$T_{d(on)}$	Turn-On Time	$V_{DS}=10V$ $I_D=1.0A$ $V_{GEN}=4.5V$ $R_G=6\Omega$		14.5	25	nS
T_r				42	62	
$T_{d(off)}$	Turn-Off Time			46	67	
T_f				34	43	

Note: 1. Pulse test: pulse width \leq 300uS, duty cycle \leq 2%

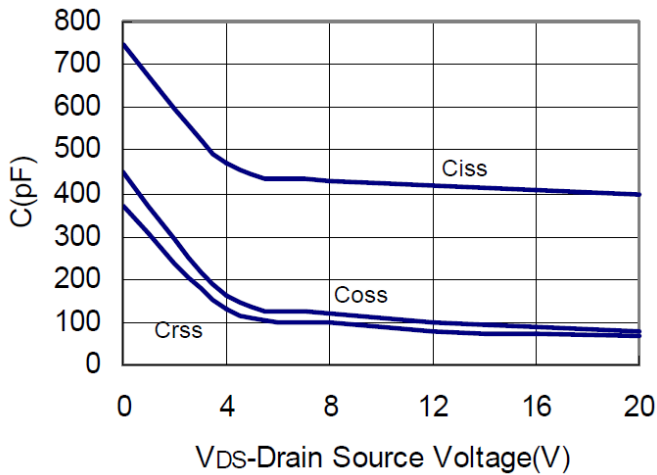
2.Static parameters are based on package level with recommended wire bonding

■ TYPICAL CHARACTERISTICS (25°C Unless Note)

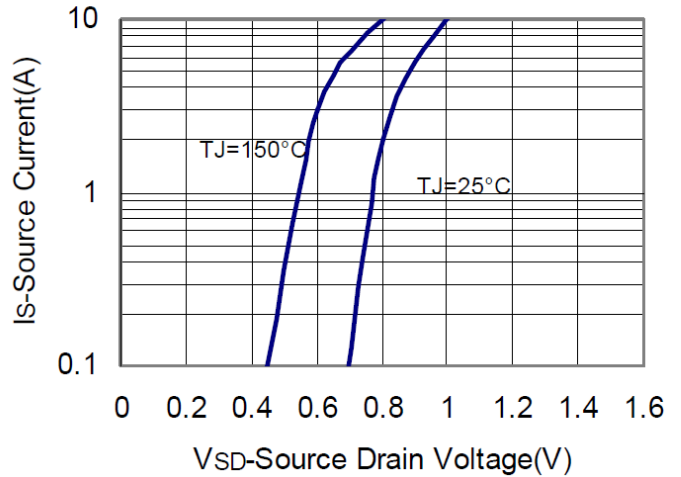


■ TYPICAL CHARACTERISTICS (continuous)

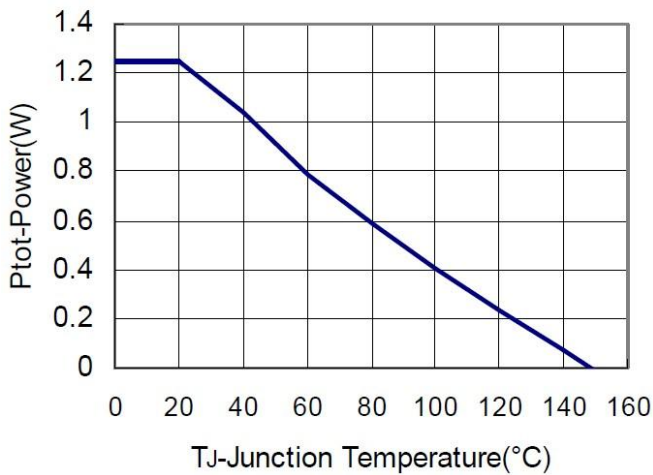
Capacitance



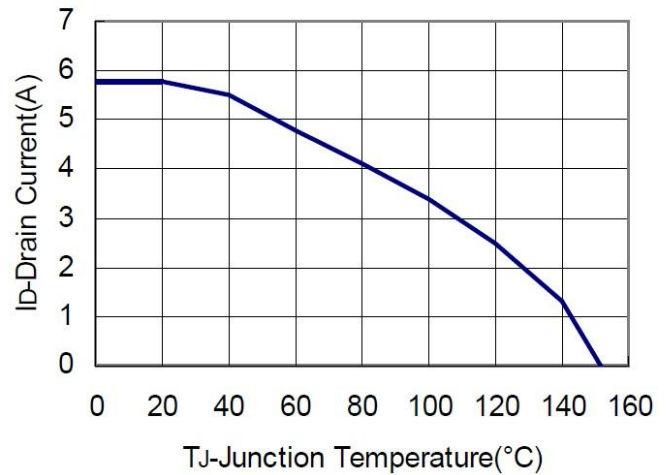
Source Drain Diode Forward



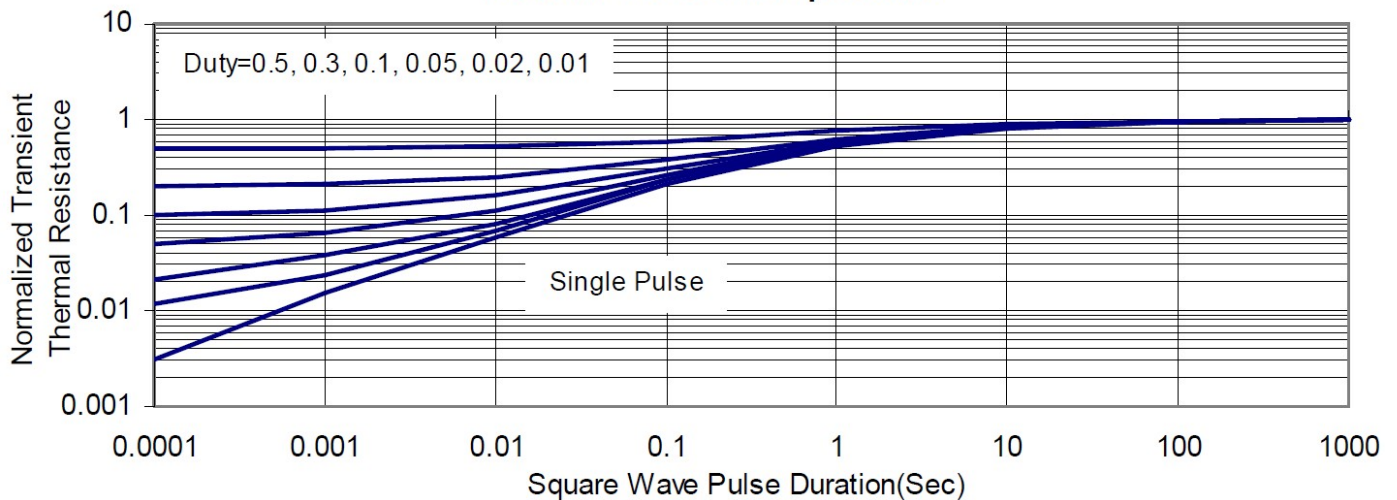
Power Dissipation

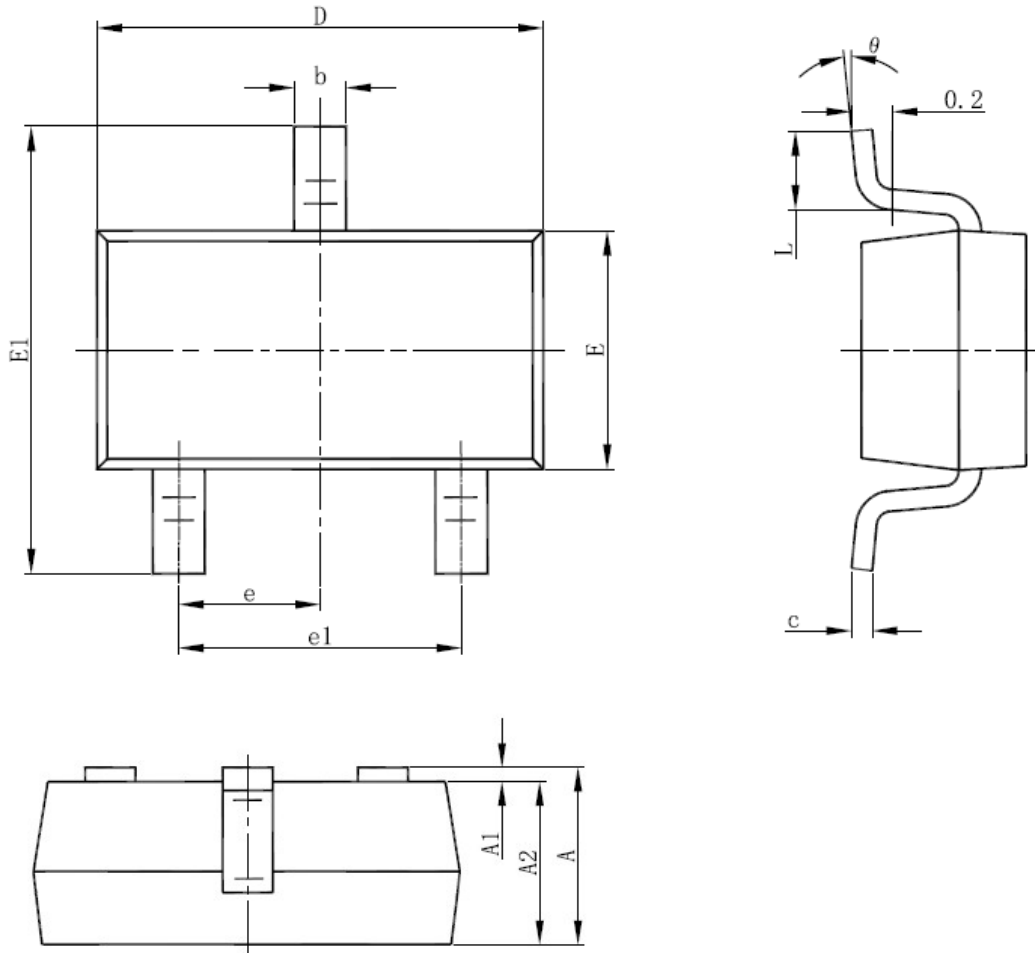


Drain Current



Thermal Transient Impedance



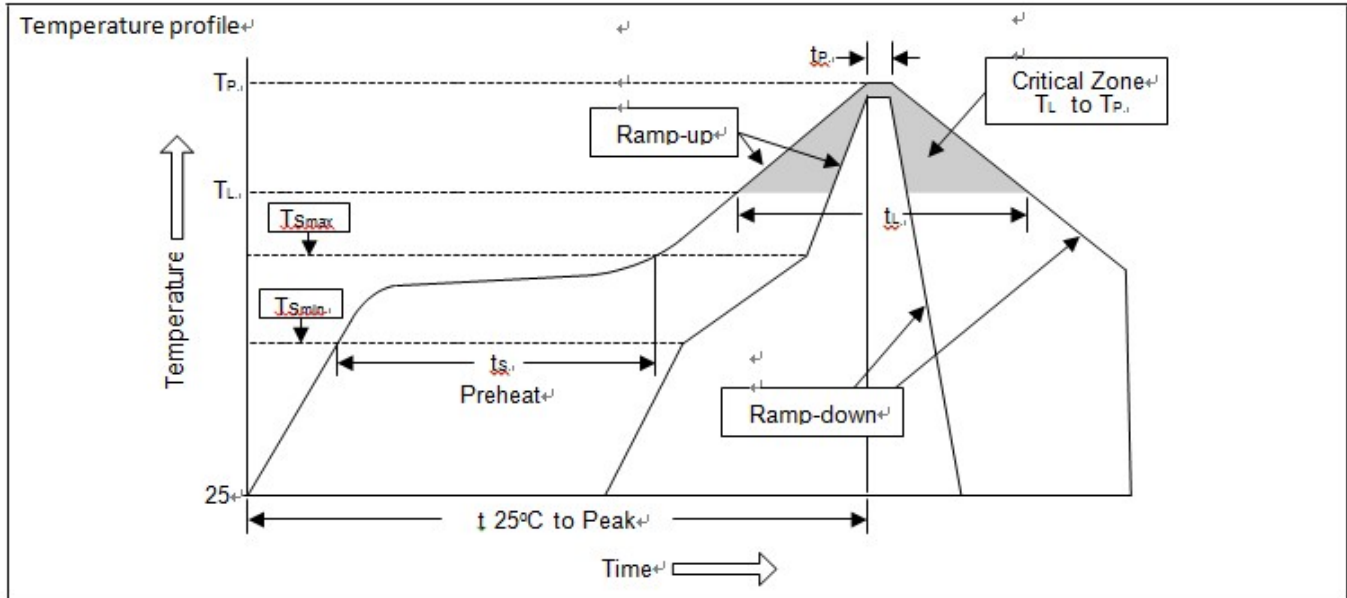
■ SOT23-3L PACKAGE OUTLINE DIMENSIONS


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950(BSC)		0.037(BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

■ SOLDERING METHODS FOR UNIVERCHIP

Storage environment Temperature=10°C~35°C Humidity=65%±15%

Reflow soldering of surface mount device



Profile Feature	Sn-Pb Eutectic Assembly	Pb free Assembly
Average ramp-up rate (T_L to T_P)	<3°C/sec	<3°C/sec
Preheat		
-Temperature Min (T_{Smin})	100°C	150°C
-Temperature Max (T_{Smax})	150°C	200°C
-Time (min to max) (t_s)	60~120 sec	60~180 sec
T_{Smax} to T_L		
-Ramp-up Rate	<3°C/sec	<3°C/sec
Time maintained above		
-Temperature (T_L)	183°C	217°C
-Time (t_L)	60~150 sec	60~150 sec
Peak Temperature (T_P)	240°C+0/-5°C	260°C+0/-5°C
Time within 5°C of actual Peak Temperature (t_p)	10~30 sec	20~40 sec
Ramp-down Rate	<6°C/sec	<6°C/sec
Time 25°C to Peak Temperature	<6 minutes	<6 minutes

Flow (wave) soldering (solder dipping)

Product	Peak Temperature	Dipping Time
Pb device	245°C±5°C	5sec±1sec
Pb-Free device	260°C+0/-5°C	5sec±1sec



This integrated circuit can be damaged by ESD. UniverChip Corporation recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedure can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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