

Dual Enhancement Mode MOSFET (N-and P-Channel)

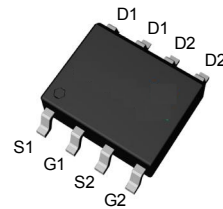
Features

- N Channel**
 40V/7.5A,
 $R_{DS(ON)} = 21m\Omega$ (max.) @ $V_{GS} = 10V$
 $R_{DS(ON)} = 25m\Omega$ (max.) @ $V_{GS} = 4.5V$
- P Channel**
 -40V/-5.5A,
 $R_{DS(ON)} = 38m\Omega$ (max.) @ $V_{GS} = -10V$
 $R_{DS(ON)} = 62m\Omega$ (max.) @ $V_{GS} = -4.5V$
- 100% UIS + R_g Tested
- Reliable and Rugged
- Lead Free Available (RoHS Compliant)

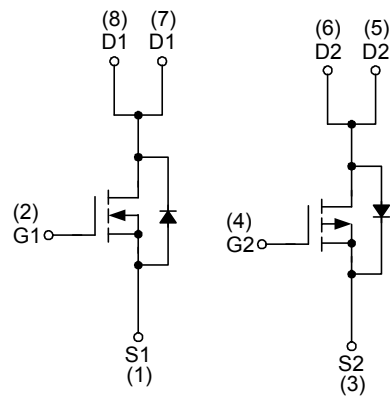
Applications

- Synchronous Rectification
- Motor Control
- Fan Pre-driver H-bridge

Pin Description



Top View of SOP-8



N-Channel MOSFET

P-Channel MOSFET

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	N Channel	P Channel	Unit	
Common Ratings					
V_{DSS}	Drain-Source Voltage	40	-40	V	
V_{GSS}	Gate-Source Voltage	± 20	± 20	V	
T_J	Maximum Junction Temperature	150		$^\circ\text{C}$	
T_{STG}	Storage Temperature Range	-55 to 150		$^\circ\text{C}$	
I_S	Diode Continuous Forward Current	2	-2	A	
I_{DP}	Pulse Drain Current Tested	$V_{GS}=10\text{V(N)}, V_{GS}=-10\text{V(P)}$		A	
I_D	Continuous Drain Current	$T_A=25^\circ\text{C}$	7.5	-5.5	A
		$T_A=70^\circ\text{C}$	6	-4.5	
P_D	Maximum Power Dissipation	$T_A=25^\circ\text{C}$	2	2	W
		$T_A=70^\circ\text{C}$	1.3	1.3	
$R_{\theta JL}$	Thermal Resistance-Junction to Lead	Steady State	50	50	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance-Junction to Ambient	$t \leq 10\text{s}$	62.5	62.5	$^\circ\text{C/W}$
		Steady State ^b	110	110	
I_{AS}^a	Avalanche Current, Single pulse	$L=0.5\text{mH}$	10	10	A
E_{AS}^a	Avalanche Energy, Single pulse	$L=0.5\text{mH}$	25	25	mJ

Note a : UIS tested and pulse width limited by maximum junction temperature 150°C (initial temperature $T_J=25^\circ\text{C}$).

Note b : Surface Mounted on 1in^2 pad area, $t=999\text{sec}$.

N Channel Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Conditions	N Channel			Unit
			Min.	Typ.	Max.	
Static Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_{DS}=250\mu A$	40	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=32V, V_{GS}=0V$	-	-	1	μA
		$T_J=85^\circ C$	-	-	30	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_{DS}=250\mu A$	1.5	2	2.5	V
I_{GSS}	Gate Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA
$R_{DS(ON)}^c$	Drain-Source On-state Resistance	$V_{GS}=10V, I_{DS}=6A$	-	16	21	m Ω
		$V_{GS}=4.5V, I_{DS}=5A$	-	18	25	
Diode Characteristics						
V_{SD}^c	Diode Forward Voltage	$I_{SD}=1A, V_{GS}=0V$	-	0.75	1.1	V
t_{rr}	Reverse Recovery Time	$I_{DS}=6A, dI_{SD}/dt=100A/\mu s$	-	13	-	ns
Q_{rr}	Reverse Recovery Charge		-	8.7	-	nC
Dynamic Characteristics^d						
R_G	Gate Resistance	$V_{GS}=0V, V_{DS}=0V, F=1MHz$	-	2.5	-	Ω
C_{iss}	Input Capacitance	$V_{GS}=0V, V_{DS}=20V, Frequency=1.0MHz$	-	815	-	pF
C_{oss}	Output Capacitance		-	95	-	
C_{rss}	Reverse Transfer Capacitance		-	60	-	
$t_{d(ON)}$	Turn-on Delay Time		$V_{DD}=20V, R_L=20\Omega, I_{DS}=1A, V_{GEN}=10V, R_G=6\Omega$	-	7.8	-
t_r	Turn-on Rise Time	-		6.9	-	
$t_{d(OFF)}$	Turn-off Delay Time	-		22.4	-	
t_f	Turn-off Fall Time	-		4.8	-	
Gate Charge Characteristics^d						
Q_g	Total Gate Charge	$V_{DS}=20V, V_{GS}=10V, I_{DS}=6A$	-	15.7	22	nC
Q_g	Total Gate Charge	$V_{DS}=20V, V_{GS}=4.5V, I_{DS}=6A$	-	7.5	10.5	
Q_{gth}	Threshold Gate Charge		-	1.85	-	
Q_{gs}	Gate-Source Charge		-	3.24	-	
Q_{gd}	Gate-Drain Charge		-	2.75	-	

Note c : Pulse test ; pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$.

Note d : Guaranteed by design, not subject to production testing.

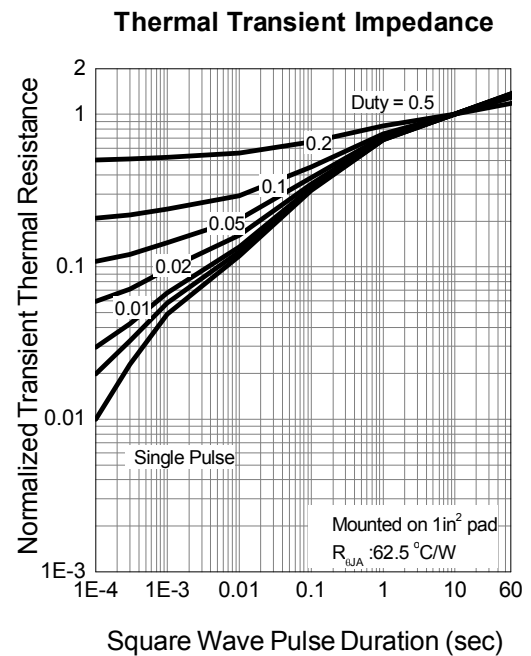
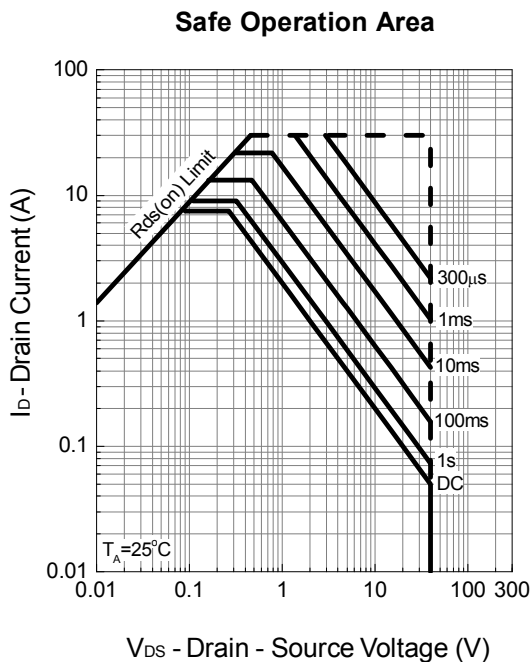
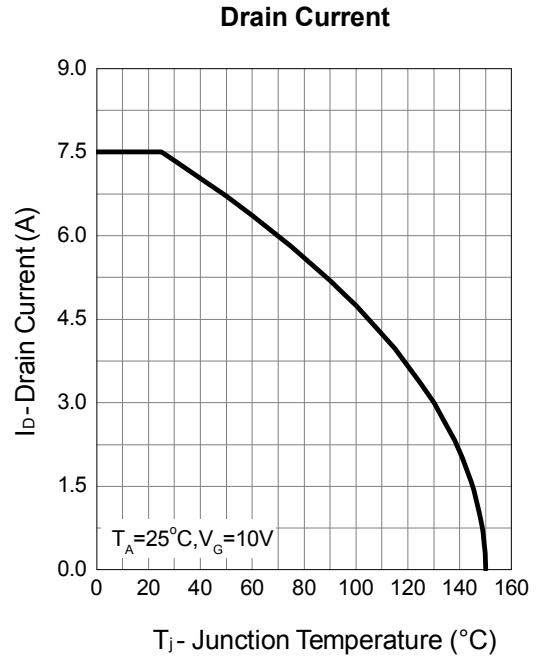
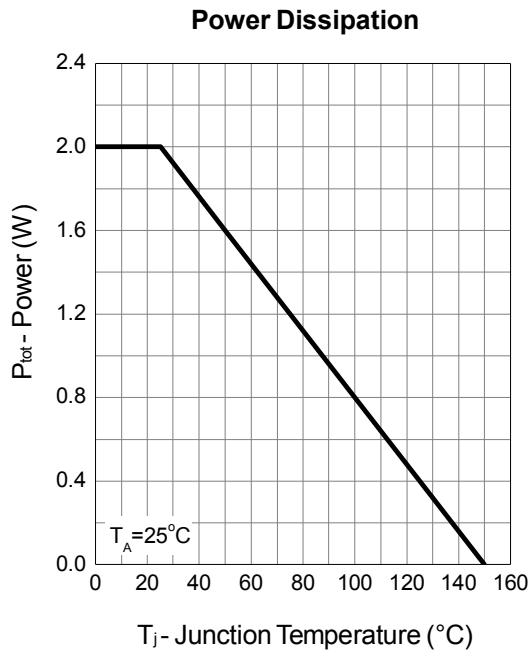
P Channel Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Conditions	P Channel			Unit
			Min.	Typ.	Max.	
Static Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_{DS}=-250\mu A$	-40	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=-32V, V_{GS}=0V$	-	-	-1	μA
		$T_J=85^\circ C$	-	-	-30	mA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_{DS}=-250\mu A$	-1.5	-2	-2.5	V
I_{GSS}	Gate Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA
$R_{DS(ON)}^c$	Drain-Source On-state Resistance	$V_{GS}=-10V, I_{DS}=-5.5A$	-	30	38	m Ω
		$V_{GS}=-4.5V, I_{DS}=-3.5A$	-	46	62	
Diode Characteristics						
V_{SD}^c	Diode Forward Voltage	$I_{SD}=-1A, V_{GS}=0V$	-	-0.75	-1	V
t_{rr}	Reverse Recovery Time	$I_{DS}=-5.5A,$ $di_{SD}/dt=100A/\mu s$	-	15	-	ns
Q_{rr}	Reverse Recovery Charge		-	8	-	nC
Dynamic Characteristics^d						
R_G	Gate Resistance	$V_{GS}=0V, V_{DS}=0V, F=1MHz$	-	8	-	Ω
C_{iss}	Input Capacitance	$V_{GS}=0V,$ $V_{DS}=-20V,$ Frequency=1.0MHz	-	668	-	pF
C_{oss}	Output Capacitance		-	98	-	
C_{rss}	Reverse Transfer Capacitance		-	72	-	
$t_{d(ON)}$	Turn-on Delay Time	$V_{DD}=-20V, R_L=20\Omega,$ $I_{DS}=-1A, V_{GEN}=-10V,$ $R_G=6\Omega$	-	8.7	-	ns
t_r	Turn-on Rise Time		-	7	-	
$t_{d(OFF)}$	Turn-off Delay Time		-	31	-	
t_f	Turn-off Fall Time		-	17	-	
Gate Charge Characteristics^d						
Q_g	Total Gate Charge	$V_{DS}=-20V, V_{GS}=-10V,$ $I_{DS}=-5.5A$	-	15	-	nC
Q_g	Total Gate Charge	$V_{DS}=-20V, V_{GS}=-4.5V,$ $I_{DS}=-5.5A$	-	7.5	-	
Q_{gth}	Threshold Gate Charge		-	1.4	-	
Q_{gs}	Gate-Source Charge		-	2.4	-	
Q_{gd}	Gate-Drain Charge		-	3.5	-	

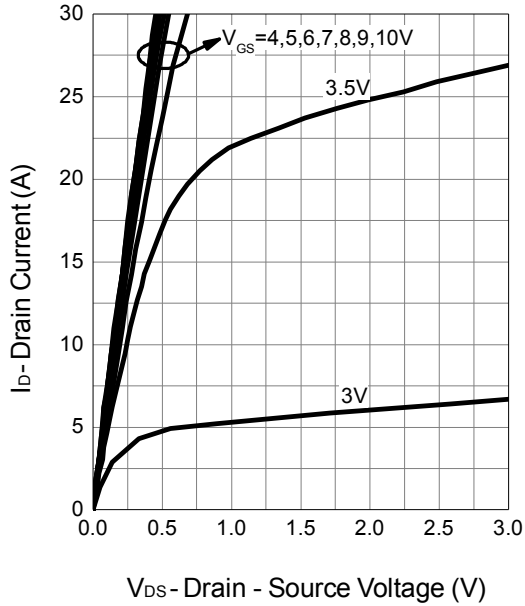
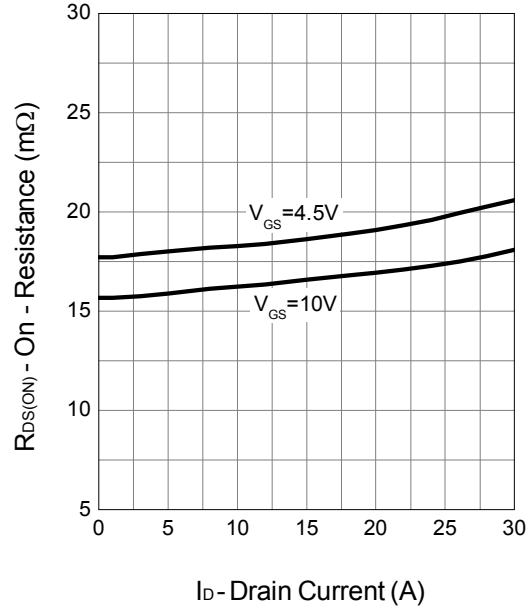
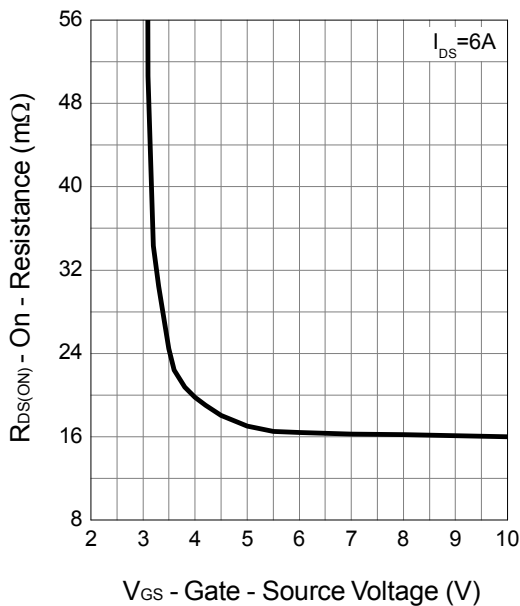
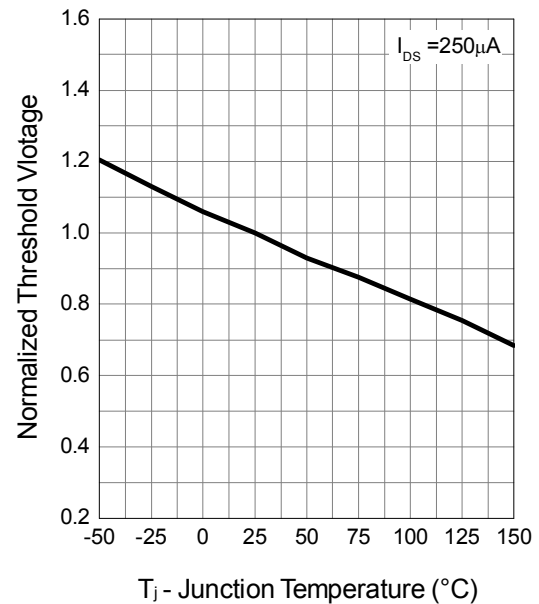
Note c : Pulse test; pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$.

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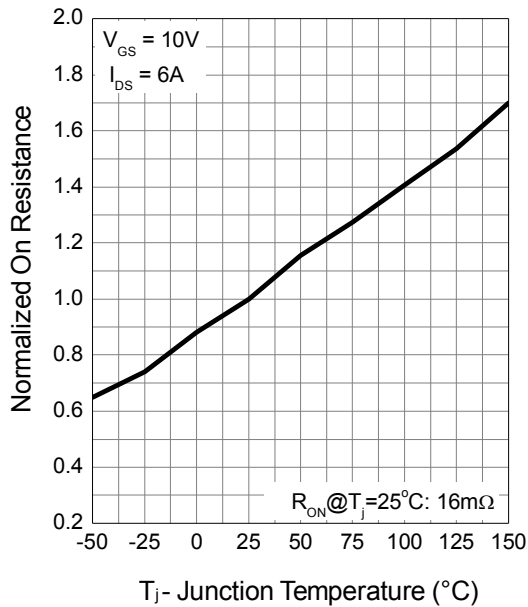
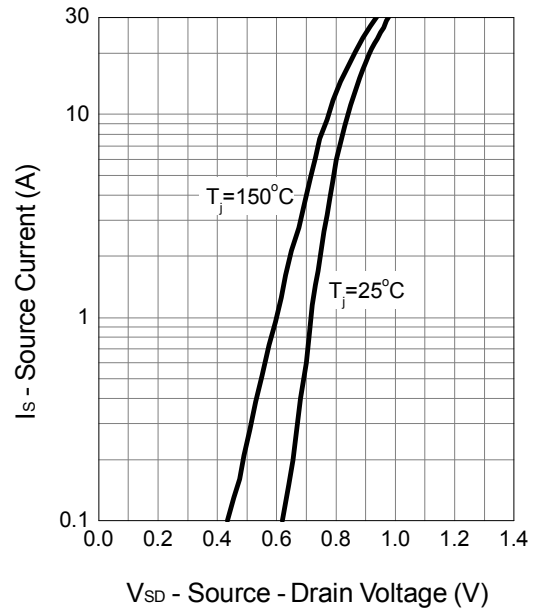
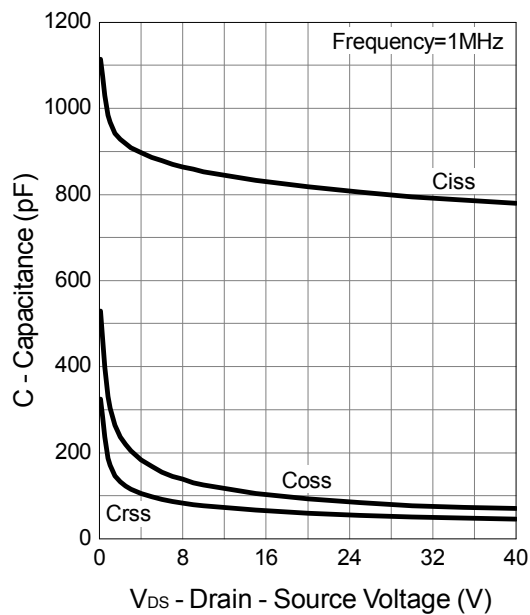
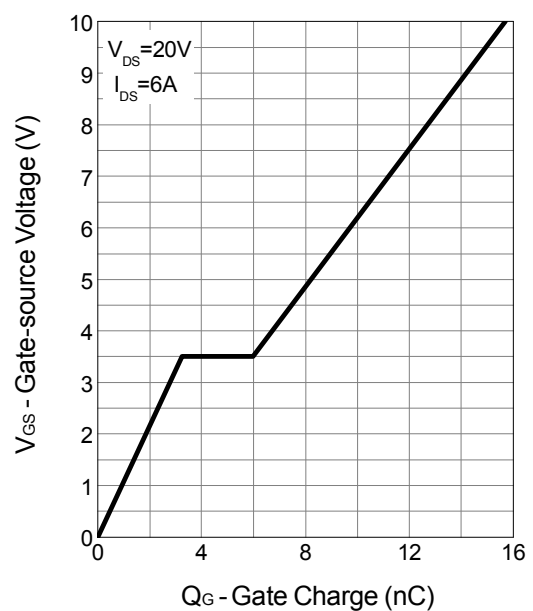
N Channel Typical Operating Characteristics



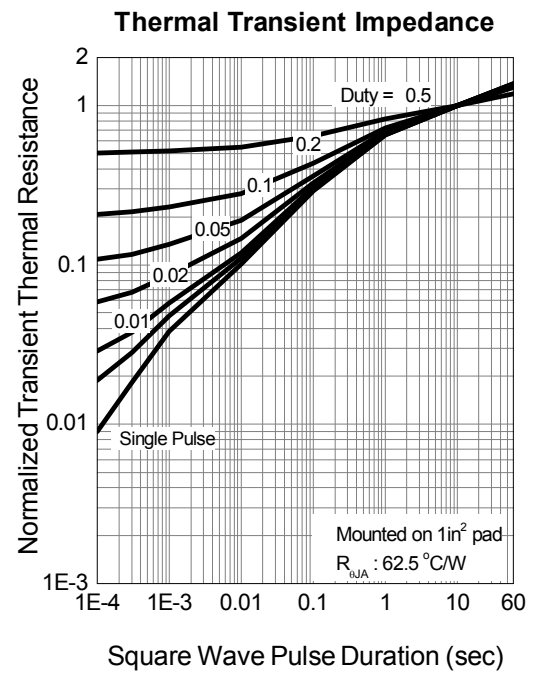
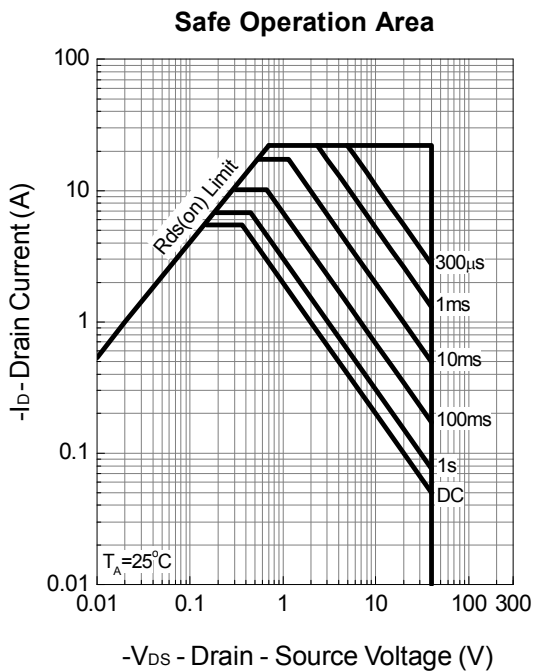
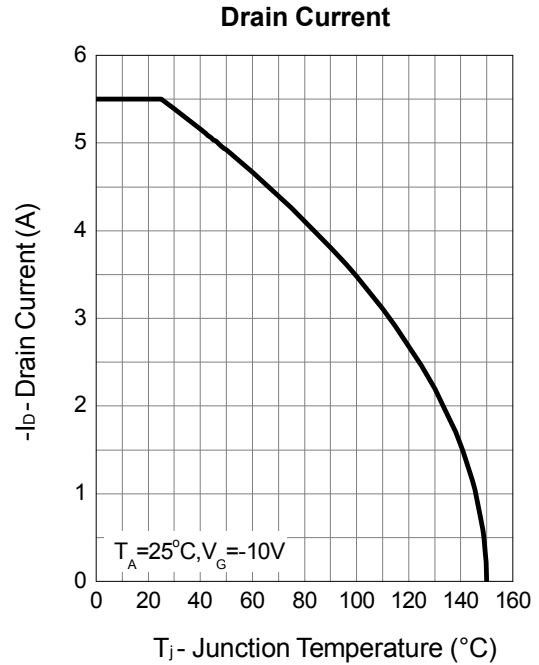
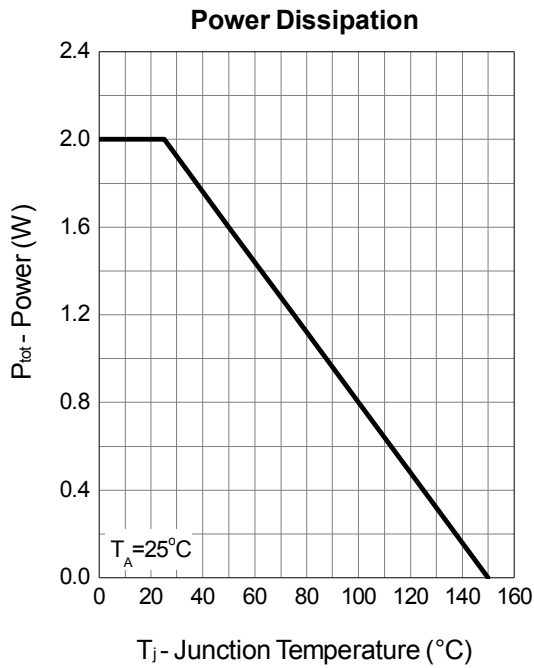
N Channel Typical Operating Characteristics (Cont.)

Output Characteristics

Drain-Source On Resistance

Gate-Source On Resistance

Gate Threshold Voltage


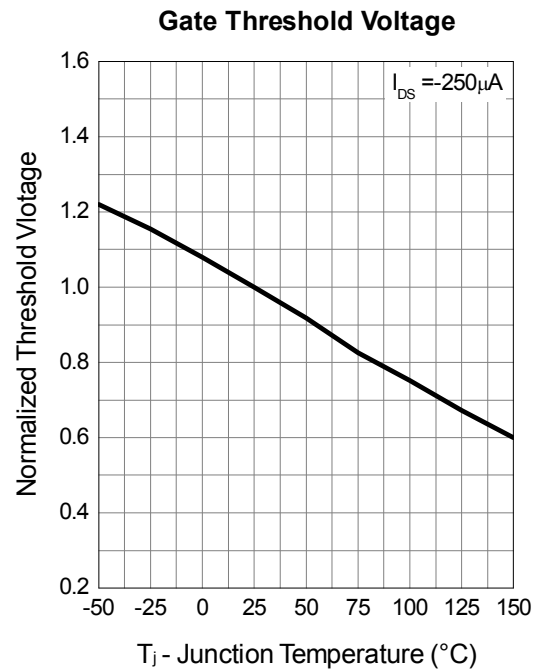
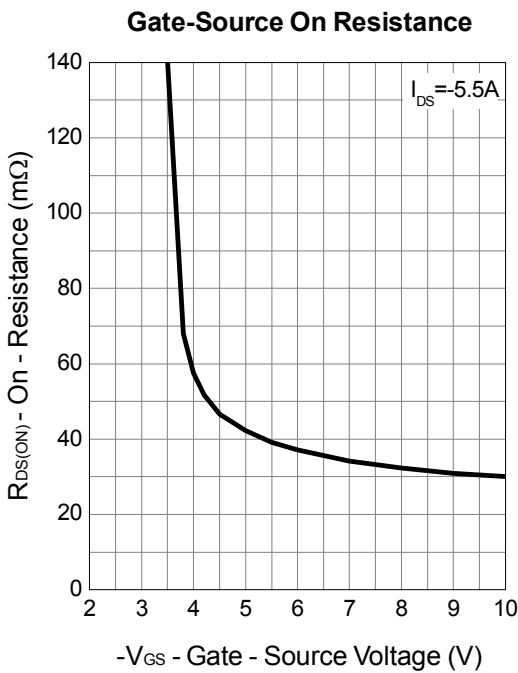
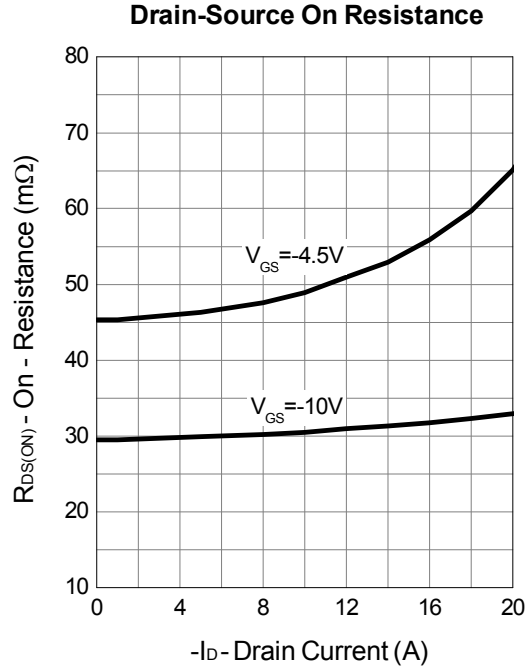
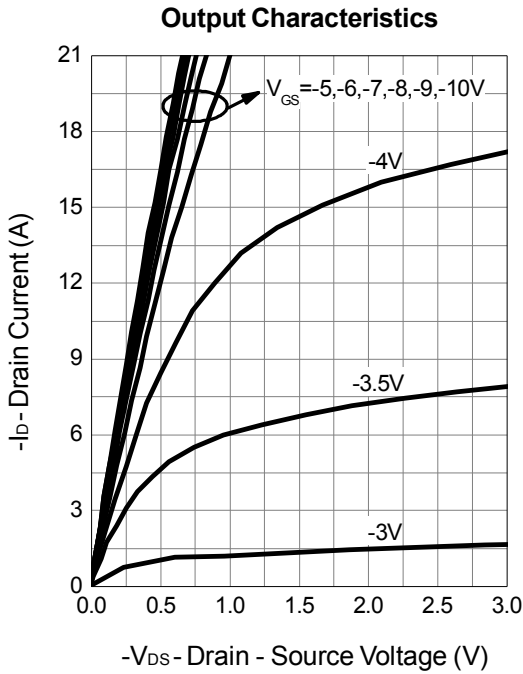
N Channel Typical Operating Characteristics (Cont.)

Drain-Source On Resistance

Source-Drain Diode Forward

Capacitance

Gate Charge


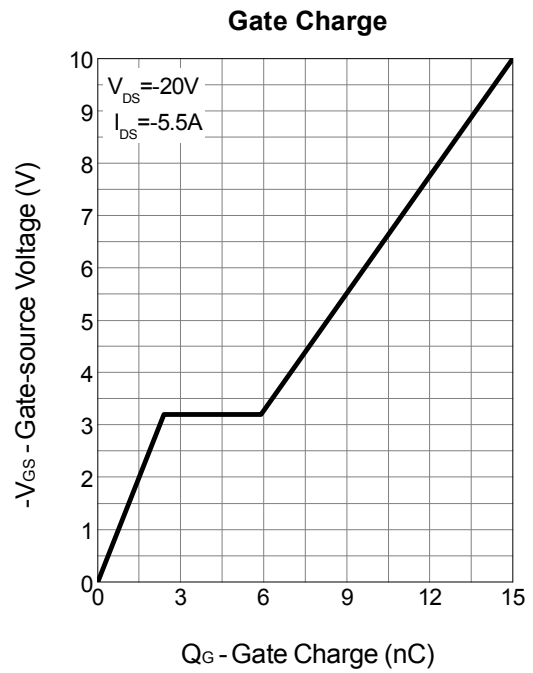
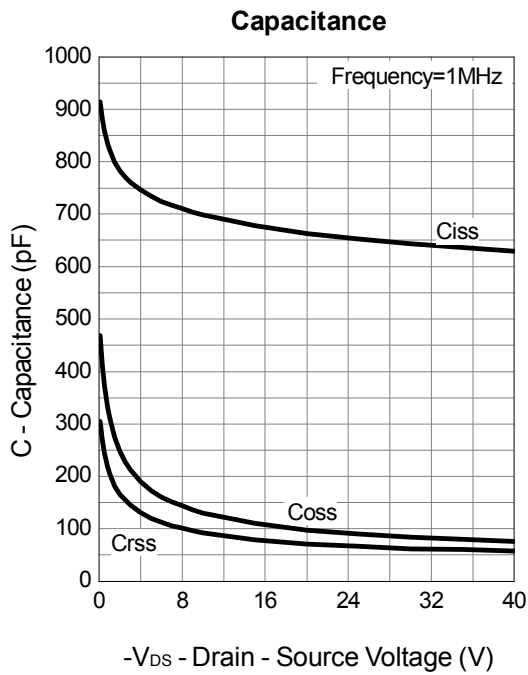
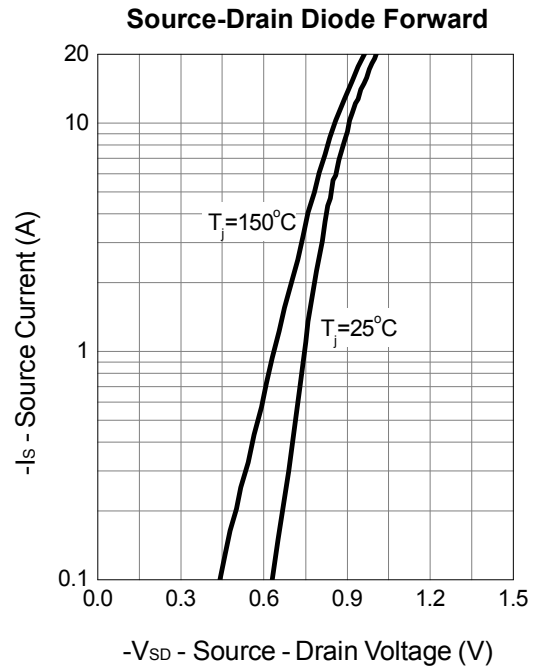
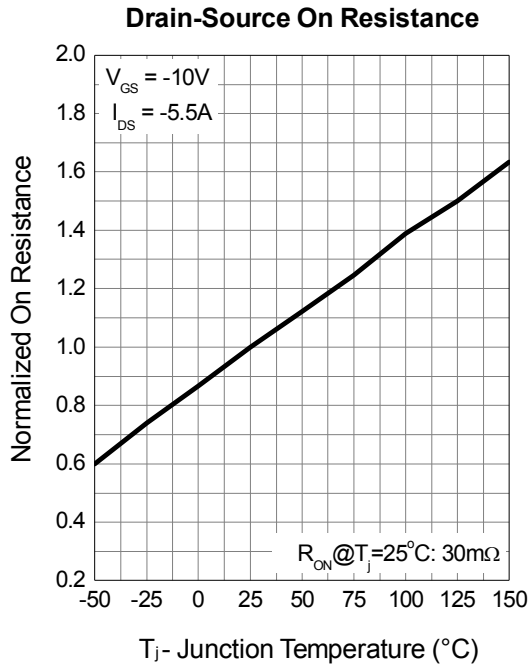
P Channel Typical Operating Characteristics



P Channel Typical Operating Characteristics (Cont.)

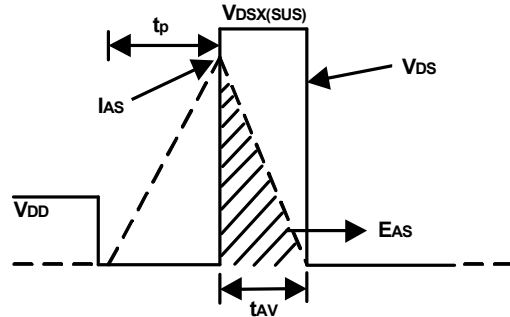
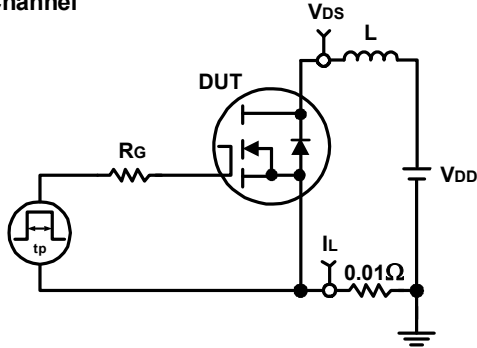


P Channel Typical Operating Characteristics (Cont.)

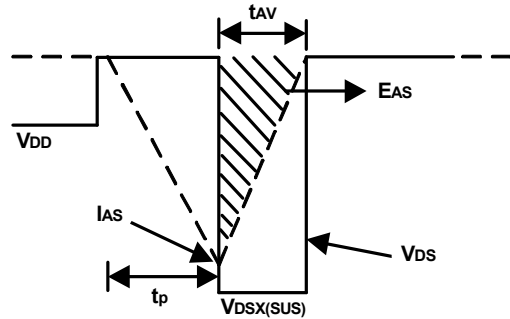
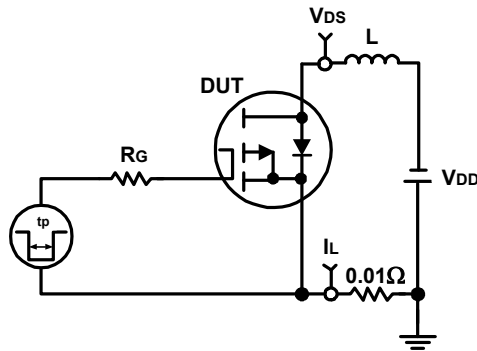


Avalanche Test Circuit and Waveforms

N Channel

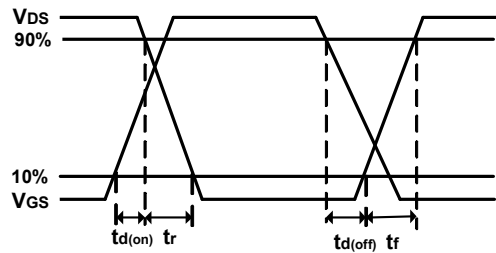
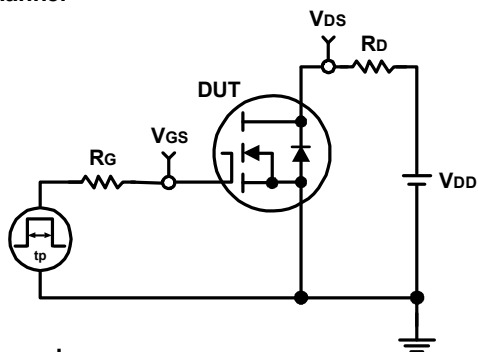


P Channel

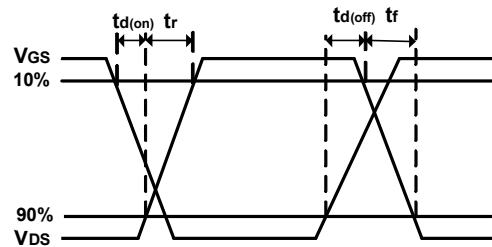
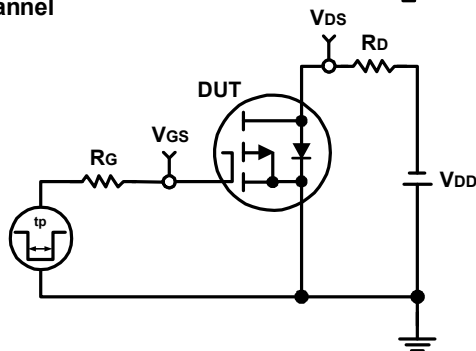


Switching Time Test Circuit and Waveforms

N Channel



P Channel



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