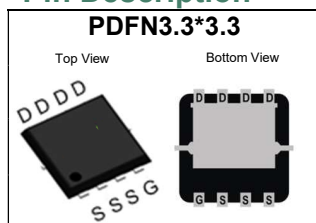
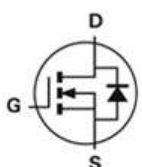


## N-Channel Enhancement Mode MOSFET

### Pin Description



### Symbol



### Product Summary

Symbol	N-Channel	Unit
$V_{DSS}$	100	V
$R_{DS(ON)-Max}$	9.2	m $\Omega$
$I_D$	49	A

### Feature

- Advanced trench cell design
- Reliable and Rugged
- ROHS Compliant & Halogen-Free
- 100% UIS and Rg Tested

### Applications

- Motor drivers
- DC-DC Converter

### Ordering Information

Orderable Part Number	Package Type	Form	Shipping	Marking
SL49N10G	PDFN3.3*3.3	Tape & Reel	5000 / Tape & Reel	

### Absolute Maximum Ratings (T<sub>J</sub>=25°C Unless Otherwise Noted)

Symbol	Parameter	N-Channel	Unit	
$V_{DSS}$	Drain-Source Voltage	100	V	
$V_{GSS}$	Gate-Source Voltage	±20		
$T_J$	Maximum Junction Temperature	150	°C	
$T_{STG}$	Storage Temperature Range	-55 to 150	°C	
$I_{DM}^{①}$	Pulse Drain Current Tested	T <sub>c</sub> =25°C	76	A
$I_D$	Continuous Drain Current	T <sub>c</sub> =25°C	49	A
		T <sub>c</sub> =100°C	31	
$P_D$	Maximum Power Dissipation	T <sub>c</sub> =25°C	36	W
		T <sub>c</sub> =100°C	14	
$I_{AS}^{②}$	Avalanche Current, Single pulse	L=0.1mH	27	A
$E_{AS}^{②}$	Avalanche Energy, Single pulse	L=0.1mH	36	mJ

### Thermal Characteristics

Symbol	Parameter	Rating	Unit	
$R_{\theta JC}$	Thermal Resistance-Junction to Case	Steady State	3.5	°C/W
$R_{\theta JA}^{③}$	Thermal Resistance-Junction to Ambient	Steady State	75	°C/W

Note ① : Max. current is limited by bonding wire

Note ② : UIS tested and pulse width are limited by maximum junction temperature 150°C

Note ③ : Surface Mounted on 1in<sup>2</sup> FR-4 board with 1oz.

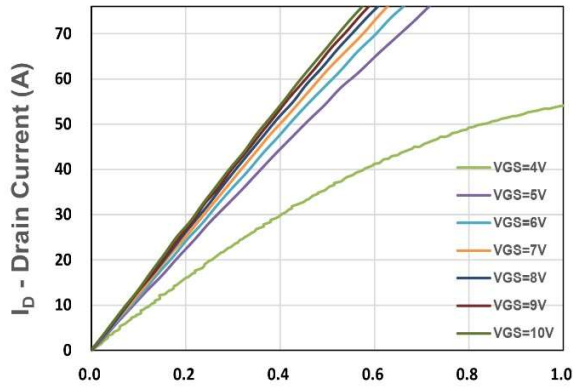
**N-Channel Electrical Characteristics** ( $T_J=25^{\circ}\text{C}$  Unless Otherwise Noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
<b>Static Electrical Characteristics</b>						
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_{DS}=250\mu A$	100	-	-	V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS}=80V, V_{GS}=0V$	-	-	1	$\mu A$
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_{DS}=250\mu A$	1	2	3	V
$I_{GSS}$	Gate Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	$\pm 100$	nA
$R_{DS(ON)}$ ●	Drain-Source On-state Resistance	$V_{GS}=10V, I_{DS}=20A$	-	7.6	9.2	m $\Omega$
		$V_{GS}=4.5V, I_{DS}=20A$	-	11	14	
<b>gfs</b>	Forward Transconductance	$V_{DS}=5V, I_{DS}=10A$	-	18.8	-	S
<b>Dynamic Characteristics</b> ●						
$R_G$	Gate Resistance	$V_{GS}=0V, V_{DS}=0V,$ Freq.=1MHz	-	1	-	$\Omega$
$C_{iss}$	Input Capacitance	$V_{GS}=0V,$ $V_{DS}=50V,$ Freq.=1MHz	-	1915	-	pF
$C_{oss}$	Output Capacitance		-	505	-	
$C_{rss}$	Reverse Transfer Capacitance		-	35	-	
$t_{d(ON)}$	Turn-on Delay Time	$V_{GS}=10V, V_{DS}=50V,$ $I_D=1A, R_{GEN}=6\Omega$	-	9.1	-	nS
$t_r$	Turn-on Rise Time		-	17.5	-	
$t_{d(OFF)}$	Turn-off Delay Time		-	32.1	-	
$t_f$	Turn-off Fall Time		-	70	-	
$Q_g$	Total Gate Charge	$V_{GS}=4.5V, V_{DS}=50V$ $I_D=20A$	-	22.1	-	nC
$Q_g$	Total Gate Charge	$V_{GS}=10V, V_{DS}=50V,$ $I_D=20A$	-	40	-	
$Q_{gs}$	Gate-Source Charge		-	8.93	-	
$Q_{gd}$	Gate-Drain Charge		-	10.5	-	
<b>Source-Drain Characteristics</b>						
$V_{SD}$ ●	Diode Forward Voltage	$I_{SD}=10A, V_{GS}=0V$	-	0.8	1.1	V
$t_{rr}$	Reverse Recovery Time	$I_F=10A, V_R=50V$	-	37.2	-	nS
$Q_{rr}$	Reverse Recovery Charge	$dI_F/dt=100A/\mu s$	-	35.1	-	nC

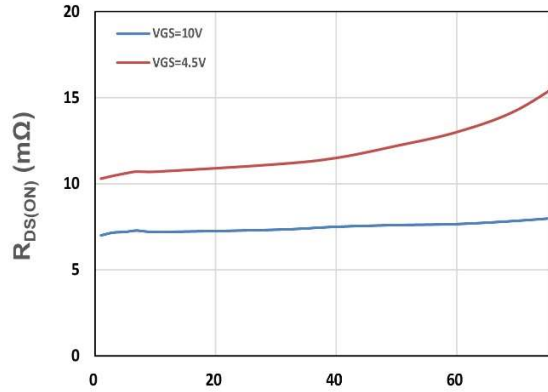
Note ④ : Pulse test (pulse width $\leq 300\mu s$ , duty cycle $\leq 2\%$ ).

Note ⑤ : Guaranteed by design, not subject to production testing.

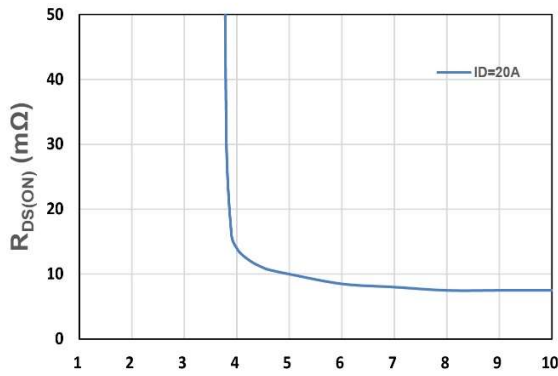
**N-Channel Typical Characteristics**



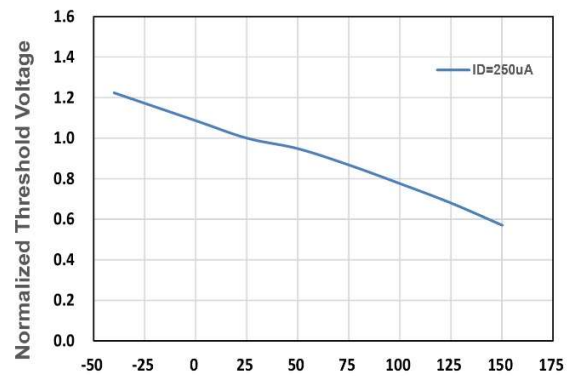
$V_{DS}$  - Drain - Source Voltage (V)  
Figure 1. Output Characteristics



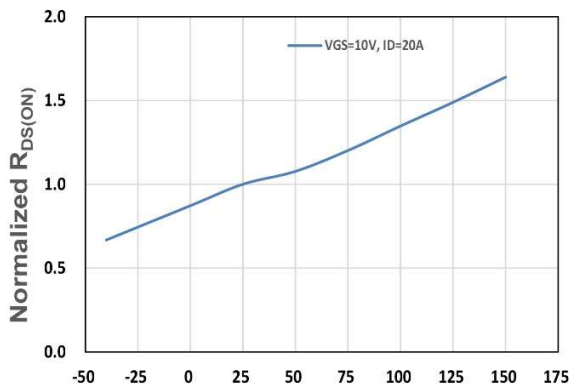
$I_D$  - Drain Current (A)  
Figure 2. On-Resistance vs. ID



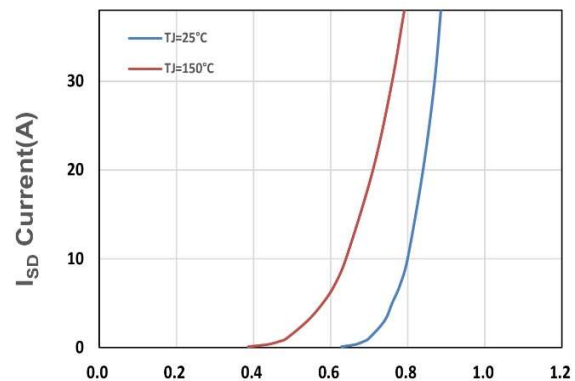
$V_{GS}$  - Gate - Source Voltage (V)  
Figure 3. On-Resistance vs. VGS



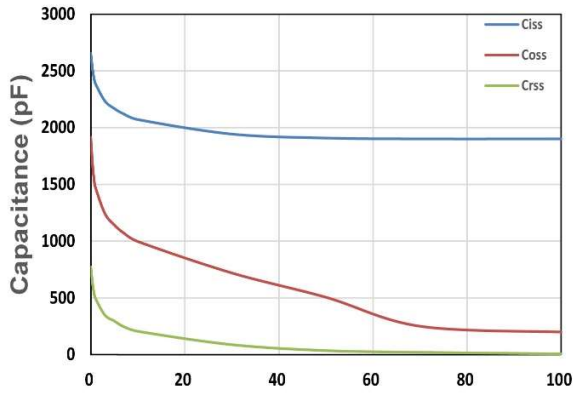
$T_j$ , Junction Temperature( $^{\circ}C$ )  
Figure 4. Gate Threshold Voltage



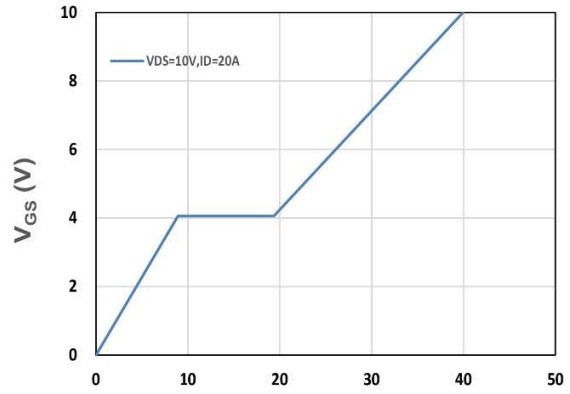
$T_j$ , Junction Temperature( $^{\circ}C$ )  
Figure 5. Drain-Source On Resistance



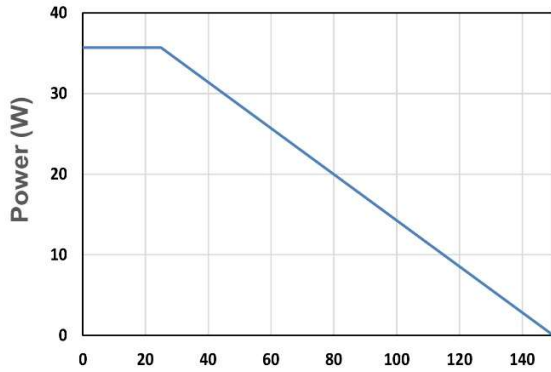
$V_{SD}$ , Source-Drain Voltage(V)  
Figure 6. Source-Drain Diode Forward



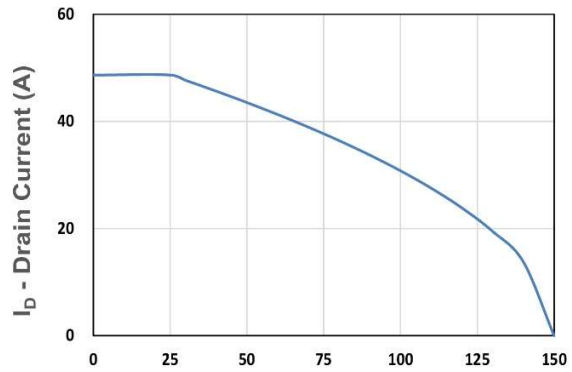
$V_{DS}$  - Drain - Source Voltage (V)  
Figure 7. Capacitance



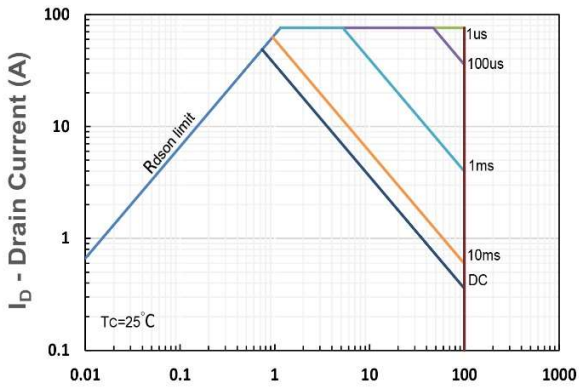
$Q_g$ , Total Gate Charge (nC)  
Figure 8. Gate Charge Characteristics



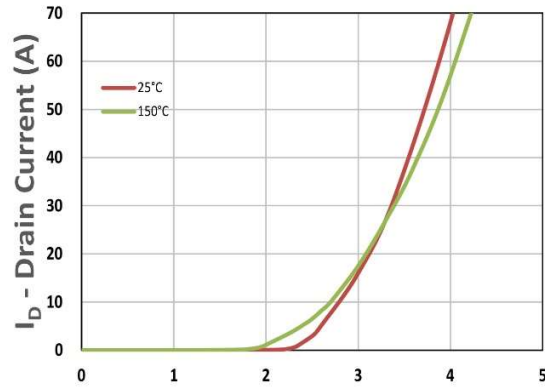
$T_c$  - Junction Temperature (°C)  
Figure 9. Power Dissipation



$T_c$  - Junction Temperature (°C)  
Figure 10. Drain Current



$V_{DS}$  - Drain-Source Voltage (V)  
Figure 11. Safe Operating Area



$V_{GS}$  - Gate - Source Voltage (V)  
Figure 12. Transfer characteristics

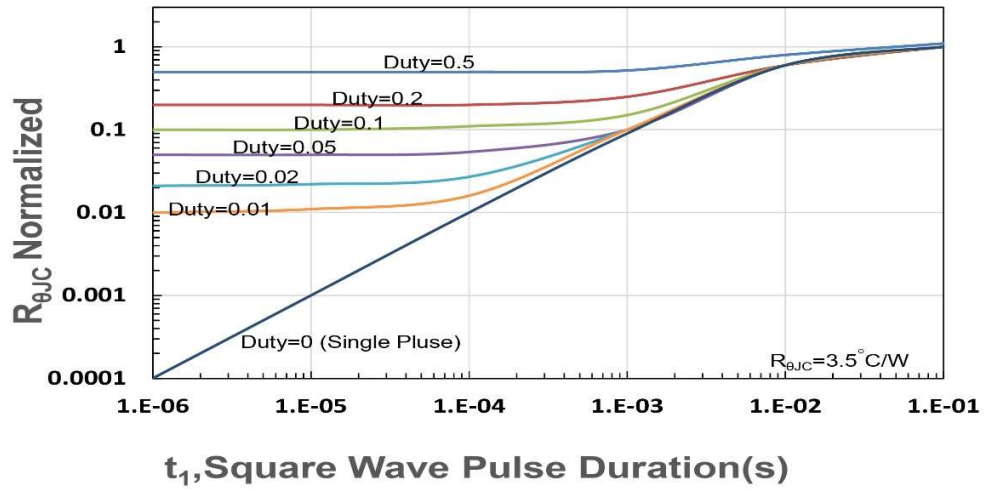


Figure 13.  $R_{\theta JC}$  Transient Thermal Impedance

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