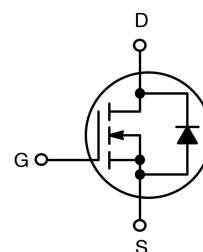
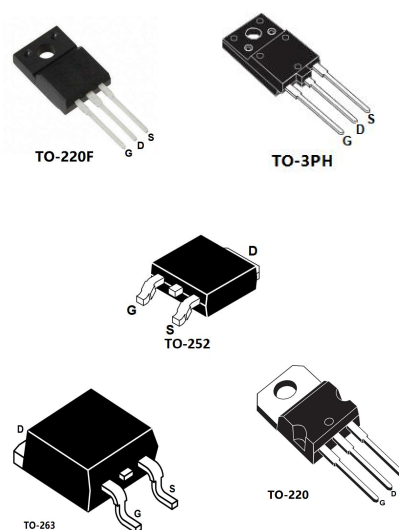


## N-channel 1000V – 3.5Ω 5A

### General features

Type	VDSS(@Tjmax)	RDS(on)	ID
SL5N100P	1000 V	< 4.2 Ω	5A
SL5N100F	1000 V	< 4.2 Ω	5A
SL5N100	1000 V	< 4.2 Ω	5A
SL5N100K	1000 V	< 4.2 Ω	5A
SL5N100D	1000 V	< 4.2 Ω	5A

- Extremely high dv/dt capability
- 100% avalanche tested
- Gate charge minimized
- Very low intrinsic capacitances
- Very good manufacturing repeatability



### Applications

- Switching application

### Order codes

Partnumber	Package
SL5N100P	TO-3PH
SL5N100F	TO-220F
SL5N100	TO-220
SL5N100K	TO-263/D2PAK
SL5N100D	TO-252/DPAK

### Electrical ratings

#### Absolute maximum ratings

Parameter	Symbol	Value				Unit
		TO-3PH	TO-220F	TO-220/ TO-252	TO-263	
Drain-source voltage ( $V_{GS}=0$ )	$V_{DS}$	1000				V
Gate-source voltage	$V_{GS}$	±30				
Drain current (continuous) at $TC=25^{\circ}C$	$I_D$	5				A
Drain current (continuous) at $TC=100^{\circ}C$	$I_D$	3				
Drain current (pulsed)	$I_{DM}$	18	18	18	18	
Total dissipation at $TC=25^{\circ}C$	PTOT	48	60	60	80	W

Drain source ESD (HBM-C=100pF,R=1.5KΩ)	$V_{ESD(GS)}$	4000	V
Peak diode recovery voltage slope	dv/dt	4.5	V/ns
Insulation withstand voltage(RMS)from all three leads to external heat sink (t=1s TC=25°C)	$V_{ISO}$	2500	v
Operating junction temperature	$T_J$	-55 to 175	°C
Storage temperature	$T_{STG}$		

**Thermal data**

Parameter	Symbol	Value				Unit
		TO-220F	TO-3PH	TO-220/ TO-252	TO-263	
Thermal resistance junction max	Rthj-case	4.2	2.6	4.2	0.63	°C/W
Thermal resistance junction-ambient max	Rtha-case	68	58	68	35	°C/W
Maximum lead temperature for soldering purpose	T	350				mJ

**Avalanche characteristics**

Parameter	Symbol	Value	Unit
Avalanche current repetitive or not-repetitive (pulse width limited by Tj Max)	IAR	5	A
Single pulse avalanche energy (starting Tj=25°C Id=Iar Vdd=50V)	EAS	583	mJ

**Electrical characteristics** ( $T_{CASE}=25^{\circ}C$  unless otherwise specified)

**On/off states**

Parameter	Symbol	Test conditions	Min	Typ	Max	Unit
Drain-source breakdown voltage	$V_{(BR)DS}$	$I_D=1mA$ $V_{GS}=0$	1000			V
Zero gate voltage drain current (VGS=0)	IDSS	VDS=Max rating			1	μA
		TC=125°C			50	μA
Gate body leakage current (VGS=0)	IGSS	VGS=±20V			±10	μA
Gate threshold voltage	$V_{GS(th)}$	VDS=VGS ID=100 μA	3	3.5	4.5	V

Static drain-source on resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> =10V I <sub>D</sub> =1.75A		3.5	4.2	Ω
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**Dynamic**

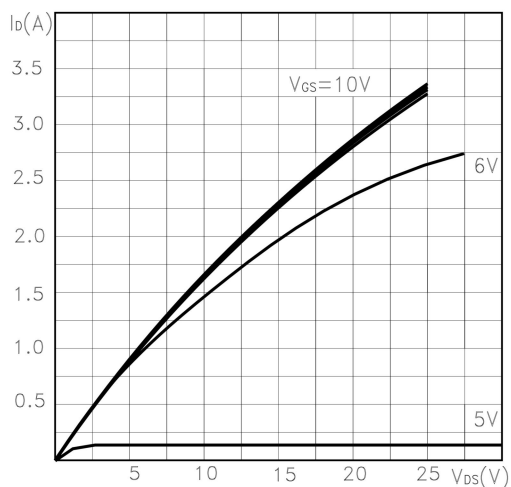
Parameter	Symbol	Test conditions	Min	Typ	Max	Unit
Forward transconductance	g <sub>fs</sub>	V <sub>DS</sub> = 40 V, I <sub>D</sub> = 4A		5		S
Input capacitance	C <sub>iss</sub>	V <sub>DS</sub> =25V, f=1MHz, V <sub>GS</sub> =0		483		pF
Output capacitance	C <sub>oss</sub>			45		
Reverse transfer capacitance	C <sub>rss</sub>			9		
Equivalent Output capacitance	C <sub>oss eq.</sub>	V <sub>GS</sub> =0, V <sub>DS</sub> =0 to 800V		46.8		
Gate input resistance	R <sub>g</sub>	f=1MHz Gate DC Bias=0 Test signal level=20mV open drain		3.65		Ω
Total gate charge	Q <sub>g</sub>	V <sub>DD</sub> =750V, I <sub>D</sub> =4A V <sub>GS</sub> =10V		12.67		nC
Gate-source charge	Q <sub>gs</sub>			3.7		
Gate-drain charge	Q <sub>gd</sub>			4.23		
Turn-on delay time	t <sub>d(on)</sub>	V <sub>DD</sub> = 500 V, I <sub>D</sub> = 1.75 A, R <sub>G</sub> = 4.7 Ω, V <sub>GS</sub> = 10 V		11.3		ns
Rise time	t <sub>r</sub>			18.5		
Turn-off-delay time	t <sub>d(off)</sub>			55		
Fall time	t <sub>f</sub>			17		

**Source Drain Diode**

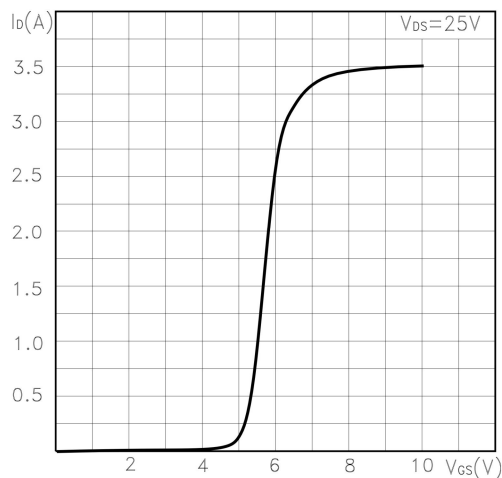
Parameter	Symbol	Test conditions	Min	Typ	Max	Unit
Source Drain Current	I <sub>SD</sub>				5	A
Source Drain Current(Pulsed)	I <sub>SDM</sub>				20	A
Forward On Voltage	V <sub>SD</sub>	I <sub>SD</sub> =5A, V <sub>GS</sub> =0V			1.2	V
Reverse Recovery Time	T <sub>rr</sub>	I <sub>SD</sub> =4A, di/dt=100A/μS		154		ns
Reverse Recovery Charge	Q <sub>rr</sub>	V <sub>R</sub> =100V, T <sub>j</sub> =150°C		677		nC
Reverse Recovery Current	I <sub>RRM</sub>			5.23		A

## Electrical characteristics (curves)

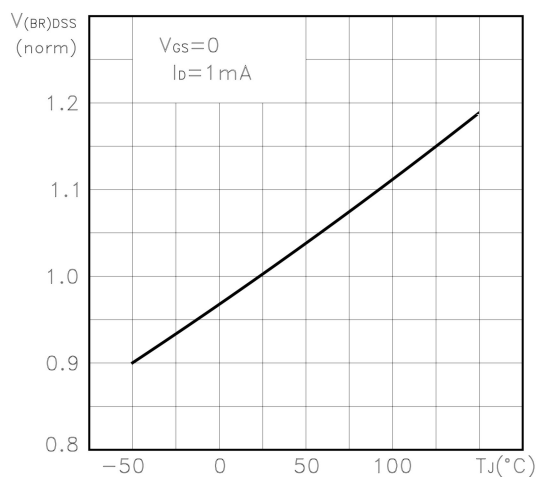
### Output characteristics



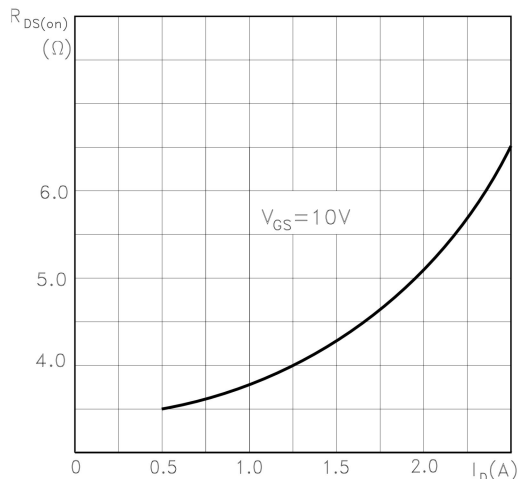
### Transfer characteristics



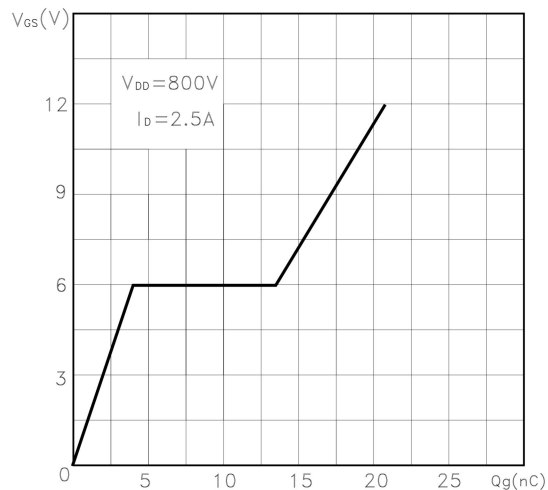
### Normalized $BV_{DSS}$ vs. temperature



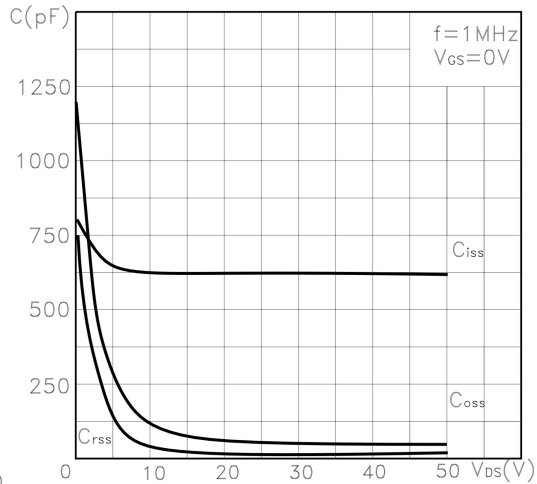
### Static drain-source on resistance



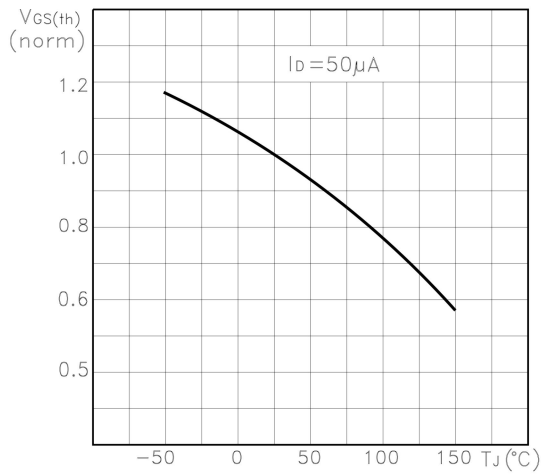
### Gate charge vs. gate-source voltage



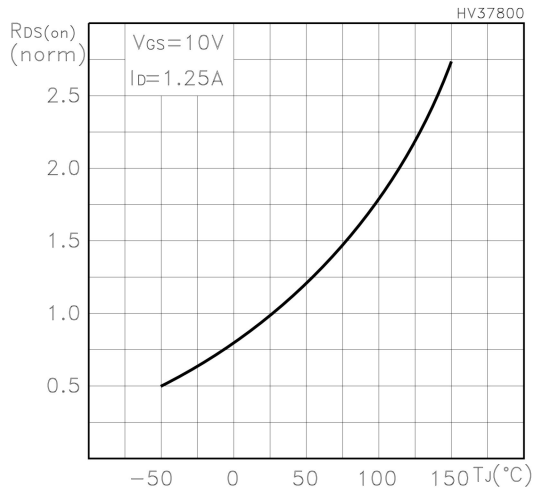
### Capacitance variations



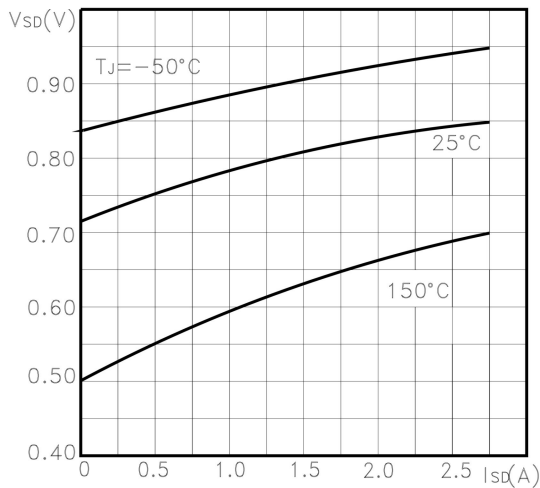
**Normalized gate threshold voltage vs. temperature**



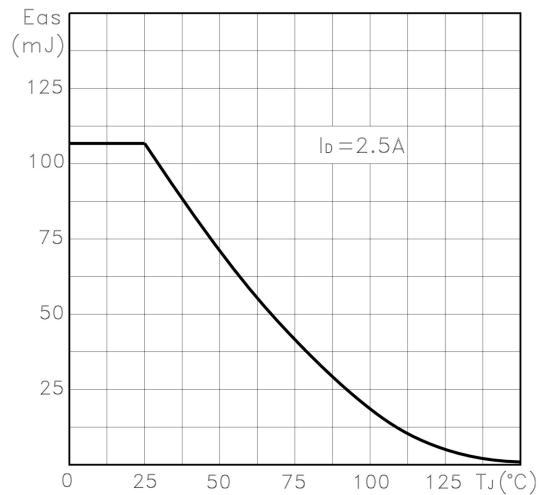
**Normalized on resistance vs. temperature**



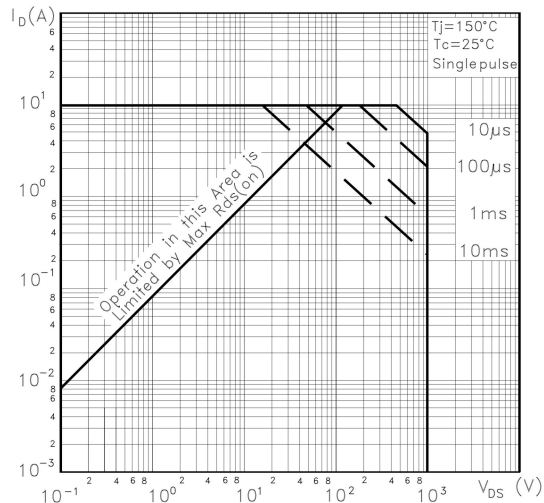
**Source-drain diode forward characteristics**



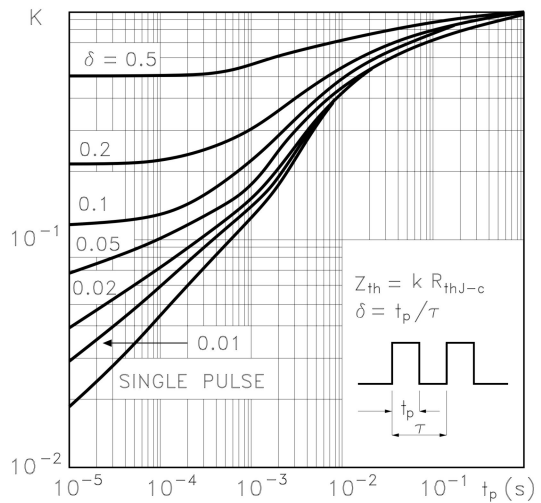
**Maximum avalanche energy vs Tj**



**Safe operating area**

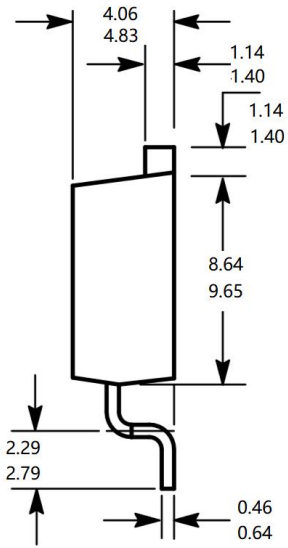
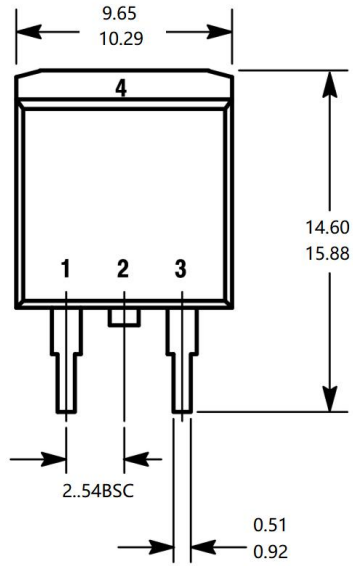


**Thermal impedance**

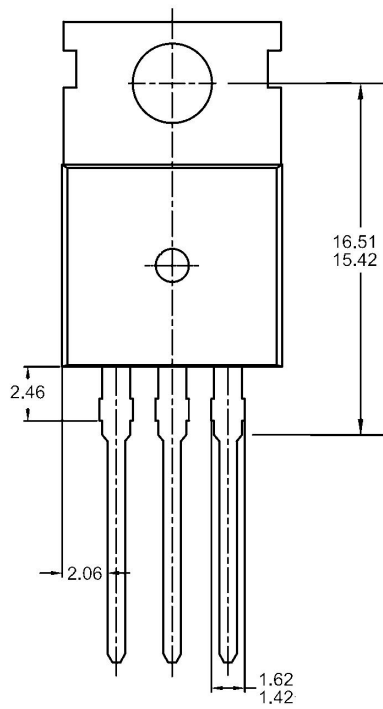


**Package outline dimension**

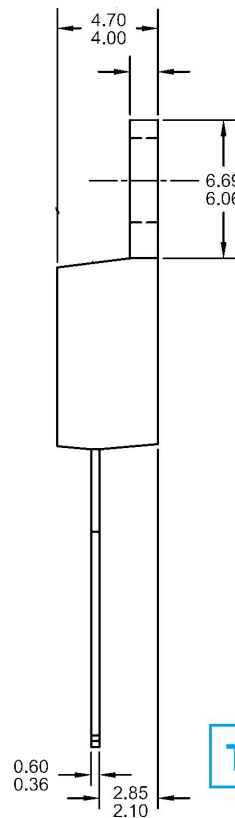
**TO-263/D2PAK**



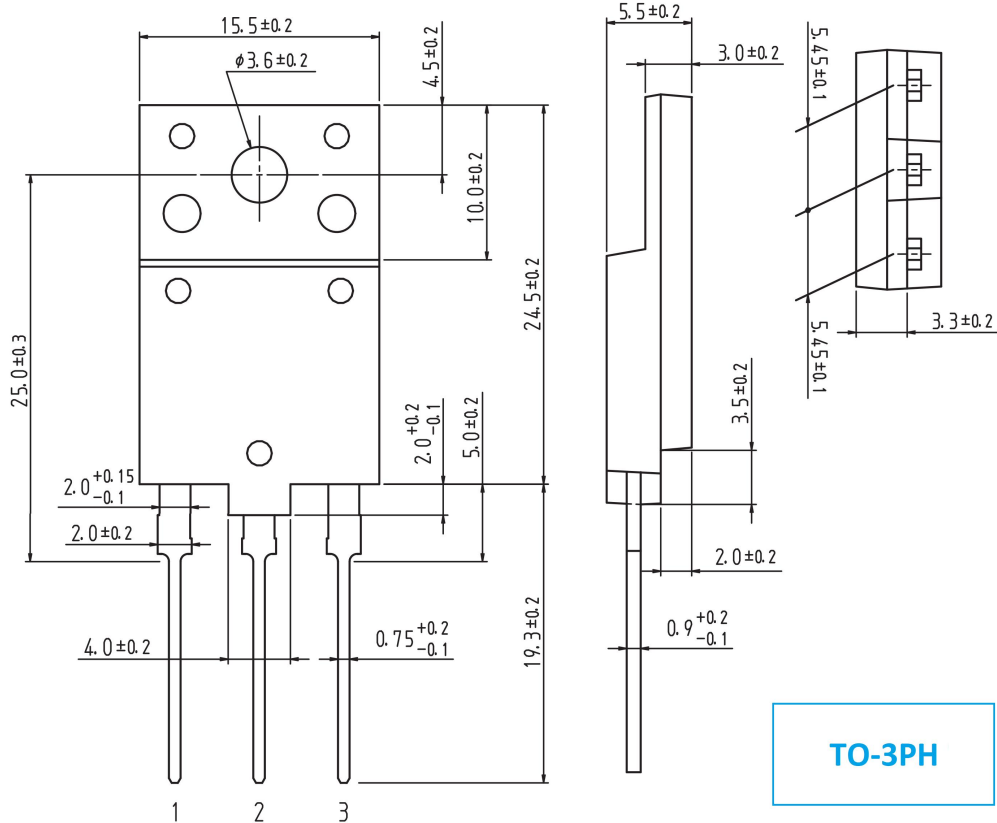
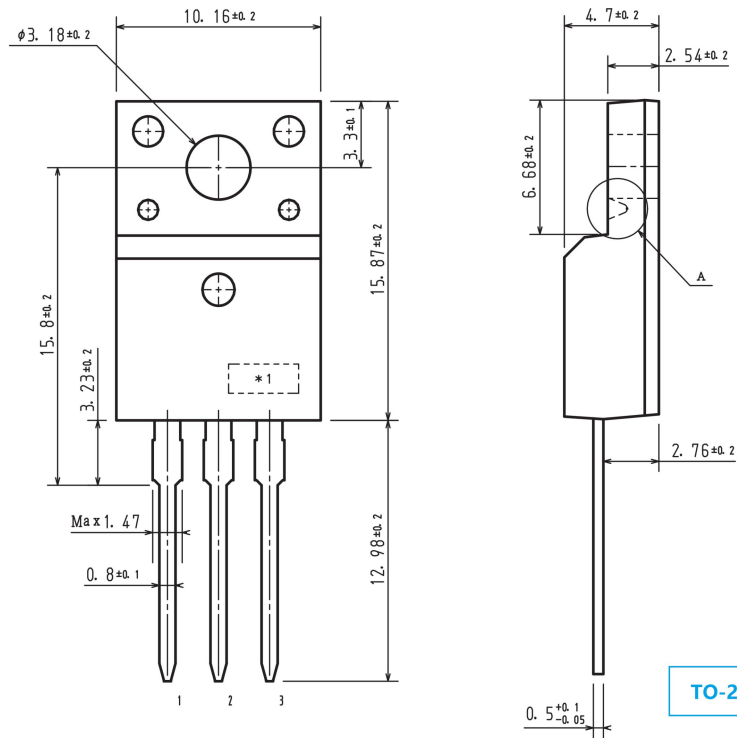
**TO-263/D2PAK**

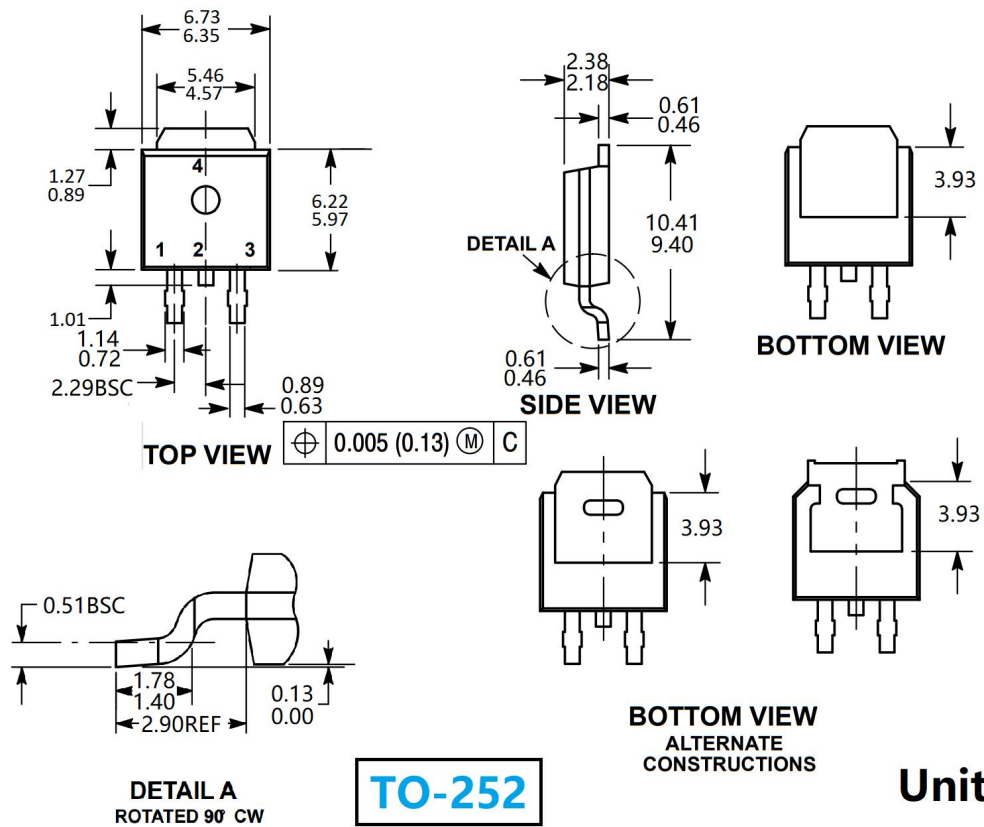


**TO-220**



**TO-220**





**Unit:mm**



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