SA1002 (APM) 80 V Full-bridge or Dual Half-bridge Protected Driver IC

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Device Overview

The SA1002 (APM) is a full-bridge or dual half-bridge driver IC dedicated to control 4 N-channel MOSFETs typically forming the DC/DC converter stage in industrial/telecom power supplies, battery inverters and chargers, and PV micro-inverters. The device is rated for harsh environments and is rated for 80 V operation.

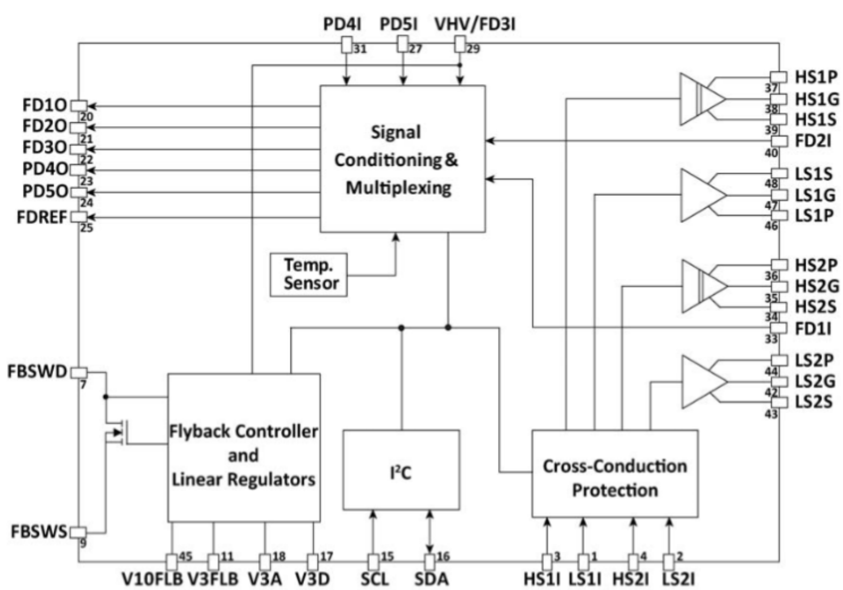
It incorporates integrated hardware for voltage sensing, a 2 W flyback controller (for system self-power), 2 pairs of high-side and low-side MOSFET drivers. It also included critical protection features like: programmable UVLO, temp sensor, and cross-conduction protection functions for each driver pair. The device is easily programmed via industry-standard I^2C interface.

APM Key Features

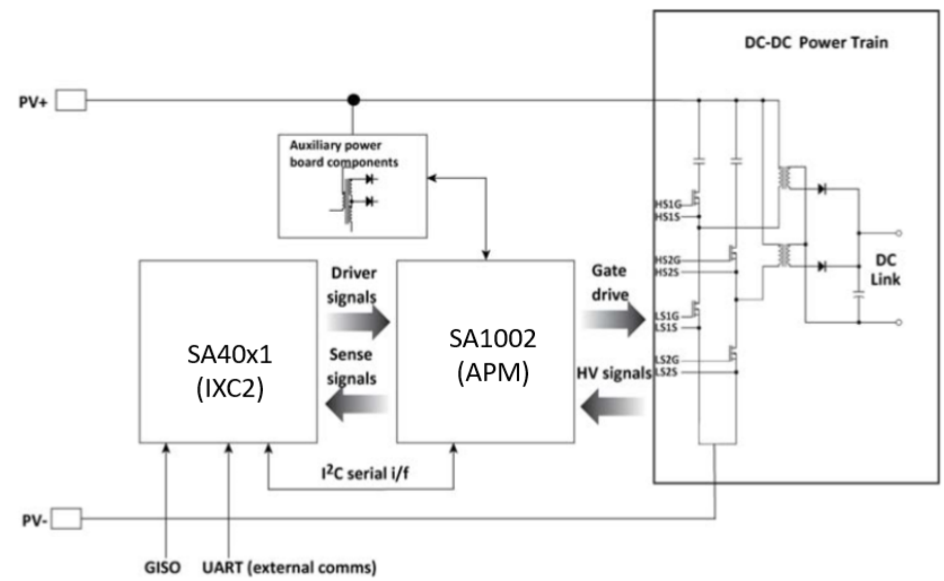
- Dual 12 V / 2.5 A low-side drivers with program-mable under-voltage lock out (UVLO)
- Dual 12 V/0.5 A high-side drivers with
- programmable UVLO
- Integrated MOSFET driver cross-conduction protection (driver interlock)
- Two precision voltage dividers (+/-0.5%) with 80 V maximum input voltage and program-mable division ratios (1/64, 1/32, 1/16, 1/8)
- Three fast voltage dividers (20 MHz) with 80 V maximum input voltage and programmable division ratios (1/64, 1/32, 1/16, 1/8)
- Pseudo-differential analog interface for divider outputs or ground-references, or direct or buffered divider output options
- Flyback controller with 0.5 ohm /90 V switch and soft-switching controller
- 5 V minimum start-up voltage for 300 mW load
- Two 3 V / 50 mA low drop-out linear voltage regulators
- 2 mA / 2.8 V linear regulator with up to 80 V input
- Temperature sensor
- I^2C interface (slave)
- TQFP48 exposed-pad package

Applications

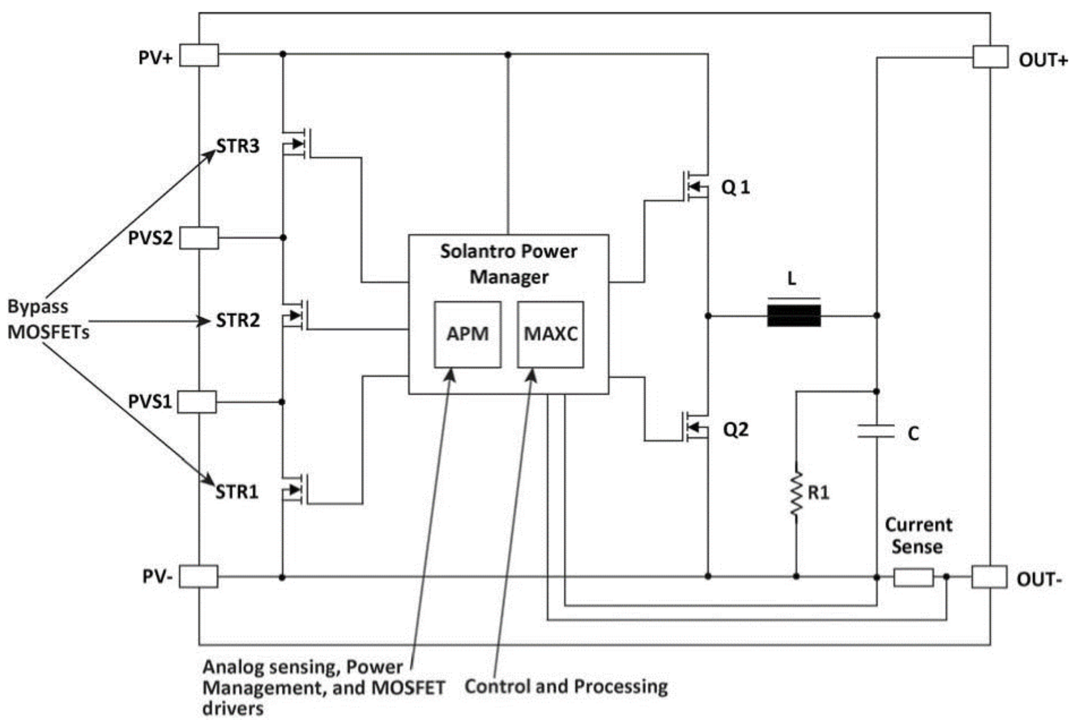
- Battery and fuel cell inverters (bi-directional)
- Dual phase DC/DC power supply
- DC-DC power optimizers



SA1002 (APM) block diagram



Micro-inverter DC-stage block diagram



DC-optimizer block diagram

Description

The SA1002 (APM) has four major functional blocks:

- Power management block
- Signal conditioning block
- High-side and low-side driver block
- I^2C interface

The power management block supplies the SA1002 (APM) blocks and all ICs of a power conversion system. The signal conditioning and multiplexing block scales the analog sensing signals and monitors the SA1002 (APM) temperature. The high-side and low-side driver control block provides gate signals to the power train MOSFETs. The I^2C serial interface allows for reading and writing of the SA1002 (APM) internal registers.

Contents

SA1002 (APM) pinout and pin functions

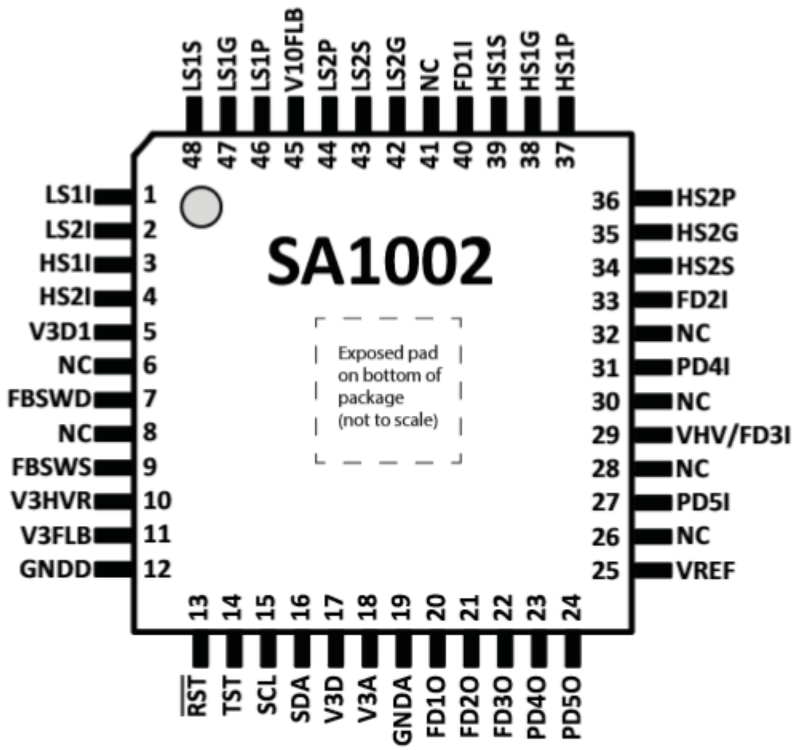


Figure 1 - SA4041 80-LQFP Pinout

Pin descriptions

Pin	Name	T	Description
1	LS1I	DIN	Low-side driver #1 input. Ground if unused.
2	LS2I	DIN	Low-side driver #2 input. Ground if unused.
3	HS1I	DIN	High-side driver #1 input. Ground if unused.
4	HS2I	DIN	High-side driver #2 input. Ground if unused.
5	V3D1	PWR	3 V supply for driver control and interlock logic External decoupling capacitor required.
6	NC	NC	High voltage pin gap. Leave unconnected.
7	FBSWD	HV	Drain (D) of internal flyback MOSFET switch.
8	NC	NC	High voltage pin gap. Leave unconnected.
9	FBSWS	GND	Source (S) of internal flyback MOSFET switch.
10	V3HVR	PWR	Output of HV linear regulator (powered directly off the VHV input). External decoupling capacitor required.

Pin	Name	Type	Description
11	V3FLB	PWR	Flyback feedback input; supply to the internal 3 V linear regulators. External decoupling capacitor required.
12	GNDD	GND	Ground return for digital section and flyback control circuitry.
13	RST	DIO	System reset output. Active LOW.
14	TST	DIN	Manufacturing test use only. Connect to ground.
15	SCL	DIN	Serial peripheral interface clock input.
16	SDA	DIO	Serial peripheral interface data I/O; Open-Drain with external pull-up resistor.
17	V3D	PWR	3 V output from digital linear regulator. External decoupling required (4.7 µF).
18	V3A	PWR	3 V output from analog linear regulator. External decoupling required (4.7 µF min).
19	GNDA	GND	Analog ground.
20	FD1O	AOUT	Fast HV divider #1 output; corresponding to scaled FD1I voltage.
21	FD2O	AOUT	Fast HV divider #2 output; corresponding to scaled FD2I voltage or to the internal signal for temperature, V_{temp}.
22	FD3O	AOUT	Fast HV divider #3 output; corresponding to scaled VHV/FD3I voltage or to the internal signal for voltage reference, V_{REF}.
23	PD4O	AOUT	Precision HV divider output; corresponding to scaled PD4I voltage or to the internal signal for over temperature indicator.
24	PD5O	AOUT	Precision HV divider output, corresponding to scaled PD5I voltage or to the internal signal for temperature, V_{temp}.
25	VREF	AOUT	Reference voltage for pseudo-differential analog output signaling.
26	NC	NC	High voltage pin gap. Leave unconnected.
27	PD5I	HV	Precision high voltage divider input. Scaled input presented at low voltage on PD5O.
28	NC	NC	High voltage pin gap. Leave unconnected.
29	VHV/FD3I	HV	Fast high voltage divider input. Scaled input is presented at low voltage on FD3O. Also used for DC supply input to the high-voltage linear regulator.
30	NC	NC	High voltage pin gap. Leave unconnected.
31	PD4I	HV	Precision high voltage divider input. Scaled input is presented at low voltage on PD4O.
32	NC	NC	High voltage pin gap. Leave unconnected.
33	FD2I	HV	Fast high voltage divider input. Scaled input is presented at low voltage on FD2O.
34	HS2S	HV	High side driver #2 supply return. Connected to HS power MOSFET2 source.
35	HS2G	HV	High side driver #2 gate control output. Connected to HS power MOSFET2
36	HS2P	HV	High side driver #2 power supply. Referenced to HS2S
37	HS1P	HV	High side driver #1 power supply. Referenced to HS1S

Pin	Name	Type	Description

38	HS1G	HV	High side driver #1 gate control output. Connected to HS power MOSFET1 gate.
39	HS1S	HV	High side driver #1 supply return. Connected to HS power MOSFET1 source.
40	FD1I	HV	Fast high voltage divider input. Scaled input is presented at low voltage on FD1O.
41	NC	NC	High voltage pin gap. Leave unconnected.
42	LS2G	DOUT12	Low side driver #2 output. Connected to LS power MOSFET1 gate.
43	LS2S	GND	Low side driver #2 supply return. Connected to LS power MOSFET2 source. Internally connected to exposed pad ground.
44	LS2P	PWR12	Low side driver #2 power supply, referenced to LS2S
45	V10FLB	PWR	Mid-voltage supply (10 V typical) and flyback controller secondary feedback input
46	LS1P	PWR12	Low side driver #1 power supply, referenced to LS1S
47	LS1G	DOUT12	Low side driver #1 gate output. Connected to LS power MOSFET1 gate.
48	LS1S	GND	Low side driver #1 supply return, Connected to HS power MOSFET1 source. Internally connected to exposed pad ground.
	Exposed pad on bottom of package	GND	Connect to ground. A good thermal connection is required for heat sinking.

Pin type legend

Pin type	Description
AOUT	analog output
DIN	3V TTL logic input
DIO	3V TTL input/output
DOUT	digital output
DOUT12	digital output
GND	ground
GND12	ground
HV	high voltage
NC	no connect
PWR	power
PWR12	power

SA1002 (APM) specifications and characteristics

Absolute maximum electrical specifications

Table 1 lists the absolute maximum electrical specifications for the SA1002 (APM).

Warning! Operating beyond the limits specified in the following table may cause permanent damage to the device. Operating at the limits specified for extended periods may affect device reliability and lifetime.

Table 1 - SA1002 (APM) absolute maximum electrical specifications

Rating	Symbol	Pin	Value	Units
High-voltage analog input voltage	V_{HVA}	PD4I, PD5I, VHV/FD3I, FD2I, FD1I	-0.5 to +80	V
3 V flyback input voltage	V_{3FLB}	V3FLB	-0.3 to +3.6	V
10 V flyback input voltage	V_{10FLB}	V10FLB	-0.3 to +18	V
Flyback MOSFET breakdown voltage	V_{FMBD}	FBSWD to FBSWS	-0.5 to +90	V
Maximum Flyback MOSFET drain current*	I_D	FBSWD	1.89	A
High side driver supply voltage	V_{HSnP}	HS*n*P to GND	-0.5 to +80 -	V
High side driver source to ground	V_{HSS}	HS*n*S to GND	-0.5 to +80	V
High side driver supply to source voltage	V_{HSP}	HS*n*P to HS*n*S	-0.3 to +15	V
High side driver output voltage	V_{HSG}	HS*n*G to HS*n*S	15	V
High side driver peak output current	V_{HSIpk}	HS*n*G to HS*n*S	0.5	A
High-side driver dv/dt immunity	SR_{HSIM}	HS*n*S	50	V/ns
Low side driver supply voltage limits	V_{LSP}	LS*n*P to GND	-0.3 to +18	V
Low side driver output voltage	V_{LSG}	LS*n*G to GND	-0.5 to +18	V
Low side driver peak output current (pull up)	V_{LSIpk}	LS*n*G	2.3	A
High side driver peak output current (pull down)	V_{HSIpk}	HS*n*G	1	A
Low-voltage analog outputs	V_{LVA}	FD1O, FD2O, FD3O, PD4O, PD5O, VREF, V3A	-0.3 to +3.6	V
Digital voltage inputs	V_{DI}	HS1I, HS2I, LS1I, LS2I, SCL, SCA	-0.3 to +3.6	V
Digital voltage output	V_{DO}	SCA, V3D	-0.3 to +3.6	V
ESD immunity (Human body model)**	V_{ESD}		500	V

Note: Unless otherwise specified, all voltages are with respect to the voltage at the GNDA (Analog) or GNDD (Digital) return pins.

*Internally limited

**All pins pass 500 V Class 1B as per JEDEC JDS-001-2014.

Thermal information

Table 2 lists the thermal specifications for the SA1002 (APM).

Table 2 - SA1002 (APM) thermal specifications

Parameter	Symbol	Minimum	Typical	Maximum	Units
Operating junction temperature range		-40		125	°C
Storage temperature range		-65		150	°C
Thermal package resistance	$R\theta_{JA}$*		34		°C/W
	$R\theta_{JC}$		3		°C/W
* Thermal resistance is measured under board-mounted and still-air conditions.					

Electrical characteristics

The following tables list the electrical characteristics of the SA1002 (APM).

Table 3 - Flyback controller

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Conditions
Control						
Start-up voltage threshold*	V_{STUP}	3.2	4	4.8	V	Voltage on VHV/FD3I pin, No external loading
Turn-on propagation delay*	t_{ON}	17.8		18.1	ns	
Turn-off propagation delay*	t_{OFF}	39		65	ns	
Minimum turn-on time*	t_{ONmin}		50		ns	
Minimum turn-off time*	t_{OFFmin}		90		ns	
Flyback 3 V input voltage	V_{3FLB}	3.2	3.3	3.4	V	
Flyback 10 V input voltage	V_{10FLB}	9		15	V	
Internal MOSFET						
Peak current	I_{LIMIT}		200		mA	
Drain-source on-state resistance	R_{DSon}		0.5	1.5	ohms	
Output capacitance*	C_{OSS}		93		pF	
Over-temperature protection						
Thermal shutoff	T_{SO}	140	150		°C	
*Guaranteed by design. Parameters in the APM design note: switching frequency, maximum voltage from switch turn off event.						

Table 4 - Linear regulators

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Conditions
Analog 3V						
Output Voltage, no external load	V_{VD3A}	2.85	3	3.15	V	V_{V3FLB} =3.5V
Current Consumption, no load	I_{ALR3}		0.2		mA	V_{V3FLB} =3.5V
Output current			50		mA	
Digital 3V						
Output Voltage, no external load	V_{VD3D}	2.85	3	3.15	V	V_{V3FLB} =3.5V
Current Consumption, no load	I_{DLR}		0.2		mA	V_{V3FLB} =3.5V
Output current			50		mA	

Table 5 - Precision Dividers (buffered conditions)

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Conditions
Divide Ratio Max Error	ME_{PFDV}	-5 -2 -2 -1		1 1 2 3	%	R =64, V_{in} = 80 V R =32, V_{in} = 40 V R =16, V_{in} = 20 V R =8, V_{in} = 10 V
Divider Output Offset*	OS_{PFDV}			10	mV	
Divider Bandwidth 3dB*	BW_{PFDV}	100		400	kHz	
*Guaranteed by design.						

Table 6 - Dividers Matching

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Conditions
Divide Ratio Max Error	ME_{PFDV}	-3 for all listed conditions		3 for all listed conditions	%	R =64, V_{in} = 80 V R =32, V_{in} = 40 V R =16, V_{in} = 20 V R =8, V_{in} = 10 V
*Guaranteed by design.						

Table 7 -Dividers Matching

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Conditions
Fast dividers matching error						
Matching error for fast dividers	ME_{FDV}	-2		2	%	R=64 Vin= 80V
Fast and precision divider matching error						
Matching Error for fast and precision dividers	ME_{FPDV}	-4		4	%	R=64 Vin= 80V
Precision dividers matching error						
Matching Error for precision dividers	ME_{PDV}	-1		1	%	R=64 Vin= 80V
*Guaranteed by design.						

Table 8 - Low-side drivers #1 and #2

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Conditions
Low-side drivers #1 and #2						
Operating Quiescent Current*	I_{QLS}		100	380	uA	V3FLB=3.6 V
Dynamic Current Consumption*	I_{LS}		10		mA	CL= 1 nF, ƒ = 100 kHz LS1P, LS2P =12 V
Peak Pull-up current*	I_{LS_PU}		2.3	2	A	
Pull-up R_{DSon}	$I_{LS\_RDSonPU}$			5	ohm	
Peak Pull-down current*	I_{LS_PD}		3.8	4	A	
Pull-down R_{DSon}	$I_{LS\_RDSonPD}$			2	ohm	
Output voltage rise time (from 10% to 90%)	t_{LS_RISE}		25 60		ns	CL= 1 nF CL= 10 nF
Output voltage fall time (from 90% to 10%)	t_{LS_FALL}		25 60		ns	CL= 1 nF CL= 10 nF
Pull-down propagation delay (from 50% input to 50% output)	t_{LS_PDD}		25 60		ns	CL= 1 nF CL= 10 nF
Pull-up propagation delay (from 50% input to 50% output)	t_{LS_PUD}		25 60		ns	CL= 1 nF CL= 10 nF
Input Threshold Turn-On, Rise*	V_{thLS_TON}		2.5		V	Input Threshold Turn-On, Rise*
Input Threshold Turn-Off, Fall*	V_{thLS_TOFF}		2		V	Input Threshold Turn-Off, Fall*
UVLO threshold, LS1P or LS2P rising	$V_{UVLO\_LS\_Rising}$		8.6 8.5 8.5		V	Temp = -40°C Temp = 25°C Temp = 125°C
UVLO threshold, LS1P or LS2P falling	$V_{UVLO\_LS\_Falling}$		8.4 8.4 8.3		V	Temp = -40°C Temp = 25°C Temp = 125°C
UVLO threshold, LS1P or LS2P hysteresis	$V_{UVLO\_LS\_Hys}$		0.2 0.1 0.2		V	Temp = -40°C Temp = 25°C Temp = 125°C
Low-side driver LSD1 and LSD2 matching error						
Delay matching error, Rise	ME_{LS_DLYR}		1		ns	CL=10nF
Delay matching error, Fall	ME_{LS_DLYF}		1		ns	CL=10nF
Rise time matching error	ME_{LS_RT}		1		ns	CL=10nF
Fall time matching error	ME_{LS_FT}		1		ns	CL=10nF
* Guaranteed by design.						

Table 9 - High-side drivers 1 & 2 (HS1S = 80V, Vdd12=12V)

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Conditions
High-side drivers #1 and #2						
Operating Quiescent Current*	IQHS		800	1800	uA	HS*n* = 1.8 V
Dynamic Current Consumption*	IHS		3.5		mA	CL=1nF, *f* = 100 kHz
Peak Pull-up current*	IHS_PU		0.5	2	A	
Pull-up RDSon	IHS_RDSonPU			5	ohm	
Peak Pull-down current*	IHS_PD		1.5	2	A	
Pull-down RDSon	IHS_RDSonPD			2	ohm	
Output voltage rise time (from 10% to 90%)	THS_RISE		25	data	ns	CL=1 nF CL=10 nF
Output voltage fall time (from 90% to 10%)	THS_FALL		25	data	ns	CL=1 nF CL=10 nF
Pull-down propagation delay (from 50% input to 50% output)	tHS_PDD		25	data	ns	CL=1 nF CL=10 nF
Pull-up propagation delay (from 50% input to 50% output)	tHS_PUD		25	data	ns	CL=1 nF CL=10 nF
Input Threshold Turn-On, Rise*	VthHS_TON		2.5		V	
Input Threshold Turn-Off, Fall*	VthHS_TOFF		2		V	
Cross conduction protection						
Dead time*	tHSLS_DT		70		ns	50% input fall 50% output rise
UVLO threshold, HS1P or HS2P rising	VUVLO_HS_Rising		8.6 8.7 8.6		V	Temp = -40°C Temp = 25°C Temp = 125°C
UVLO threshold, HS1P or HS2P falling	VUVLO_HS_Falling		8.3 8.4 8.3		V	Temp = -40°C Temp = 25°C Temp = 125°C
UVLO threshold, LS1P or LS2P hysteresis	VUVLO_HS_Hys		0.5 0.3 0.3		V	Temp = -40°C Temp = 25°C Temp = 125°C
High-side driver HSD1 and HSD2 matching error						
Delay matching error, Rise	MEHS_DLYR		1	2	ns	CL=1 nF
Delay matching error, Fall	MEHS_DLYF		1	2	ns	CL=1 nF
Rise time matching error	MEHS_RT		1	2	ns	CL=1 nF
Fall time matching error	MEHS_FT		1	2	ns	CL=1 nF
*Guaranteed by design.						

Characterization plots

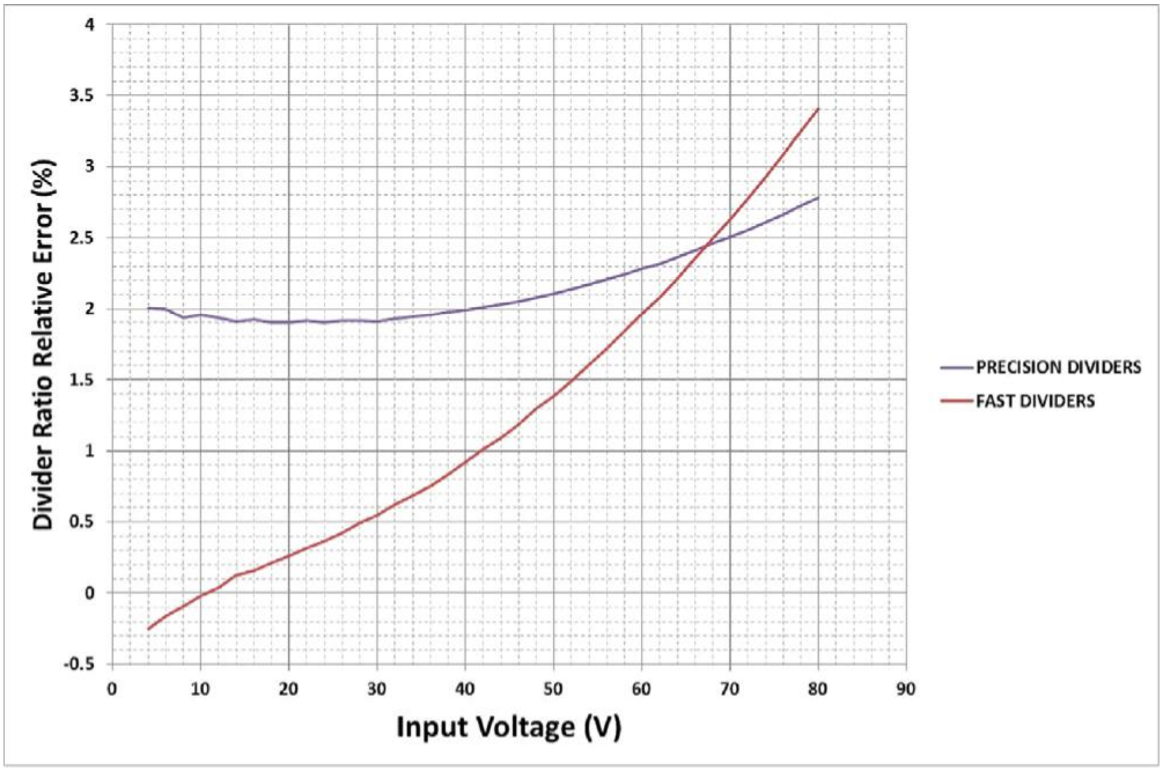


Figure 2 - Relative error (divider ratio 1/64) vs input voltage at 25°C.

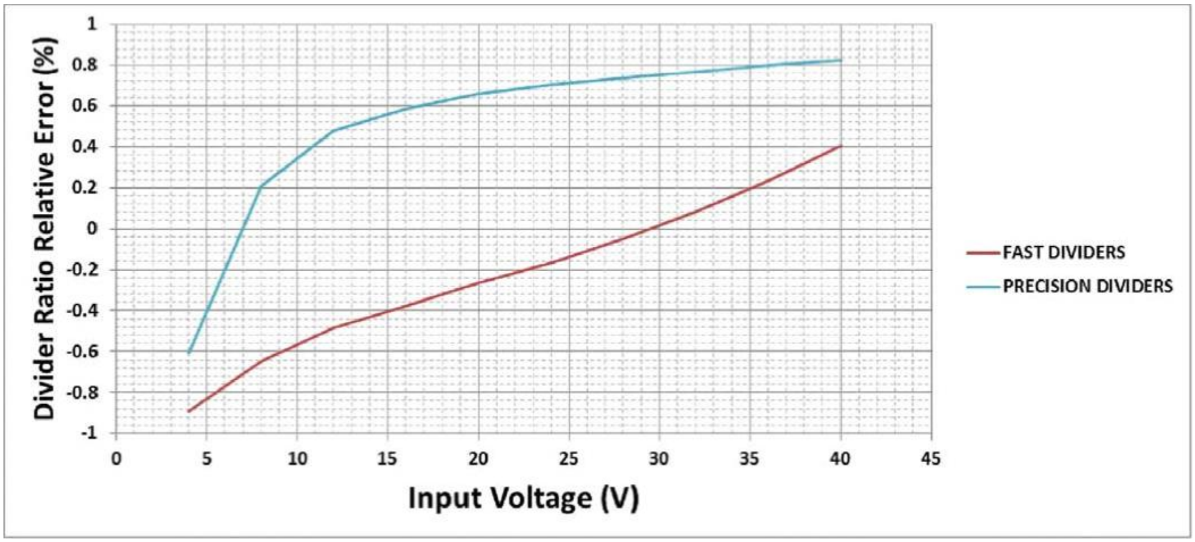


Figure 3 - Relative error (divider ratio 1/32) vs input voltage at 25°C

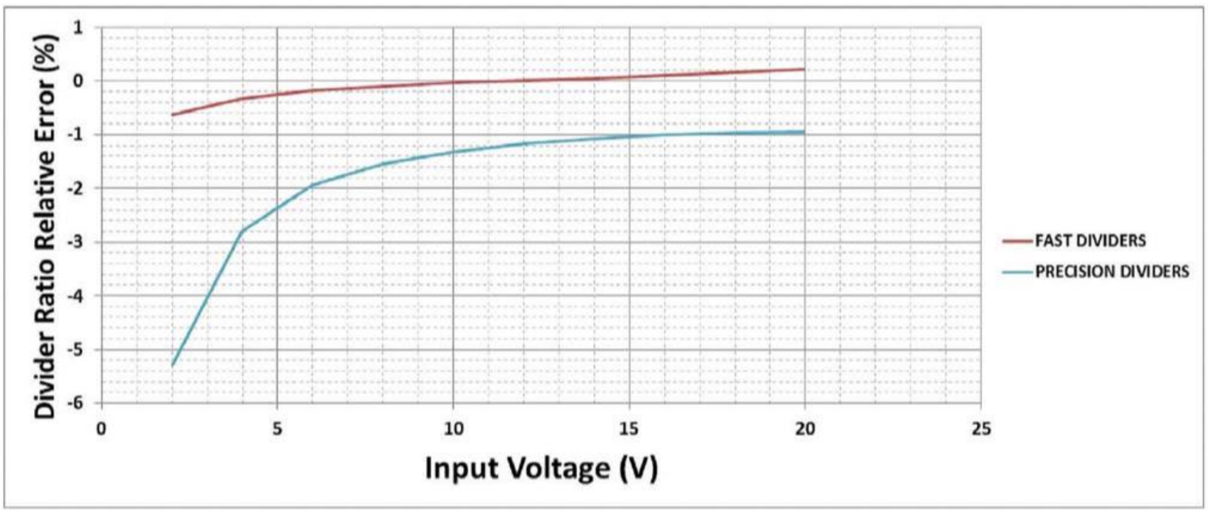


Figure 4 -Relative error (divider ratio 1/16) vs input voltage at 25°C

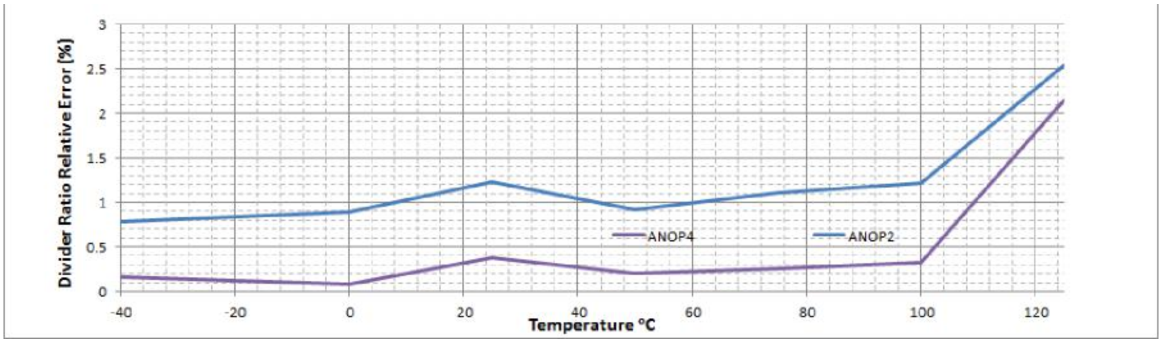


Figure 5 - Relative error (divider ratio 1/32) vs temperature at Vin = 80 V

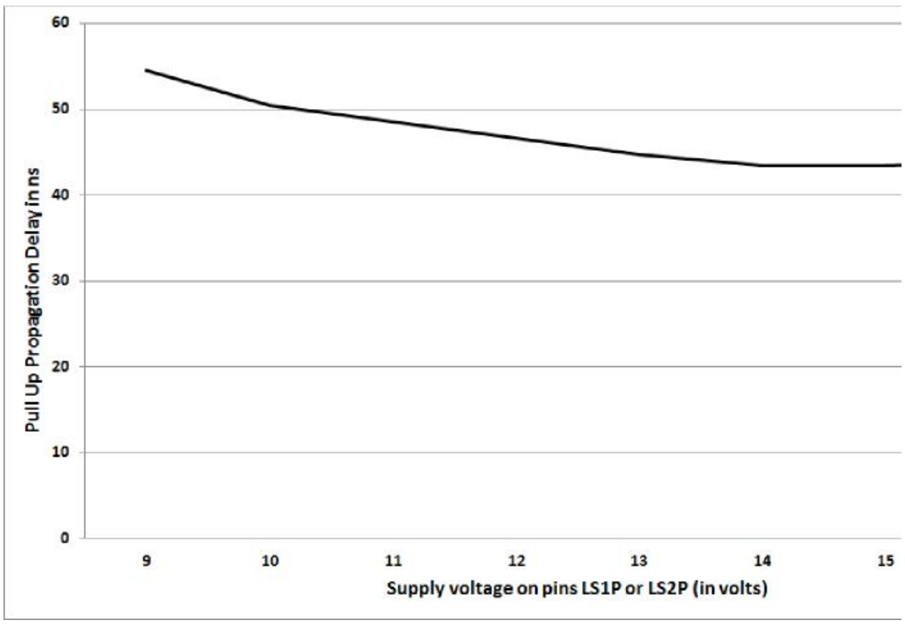


Figure 6 - Low side driver (LS1G or LS2G) pull up propagation delay versus supply voltage (pins LS1P or LS2P) at 25°C

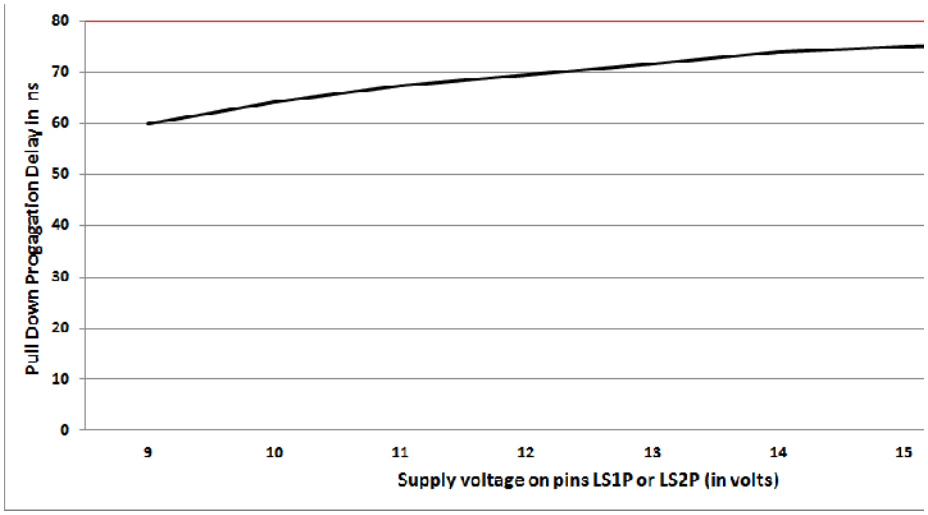


Figure 7 - Low side driver (LS1G or LS2G) pull down propagation delay versus supply voltage (pins LS1P or LS2P) at 25°C

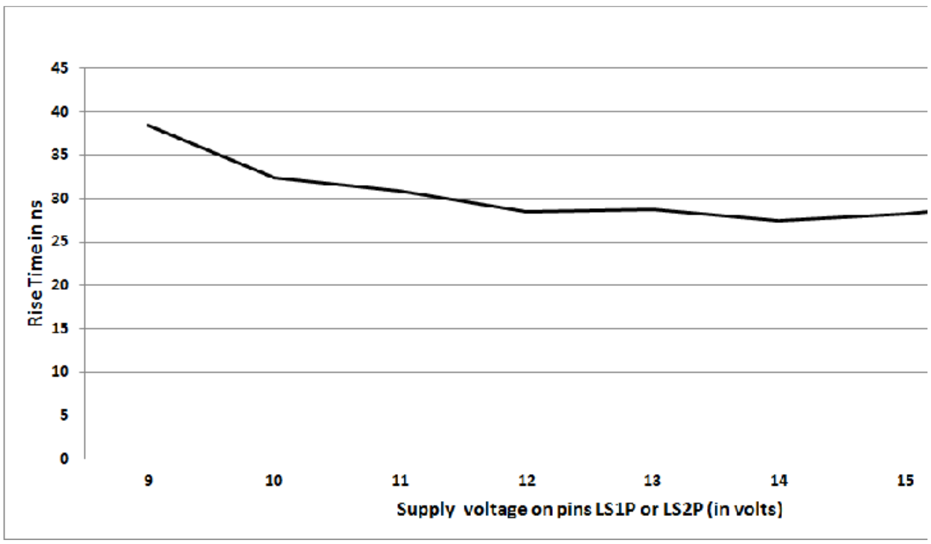


Figure 8 - Low side driver (LS1G or LS2G) rise time versus supply voltage (pins LS1P or LS2P) at 25°C

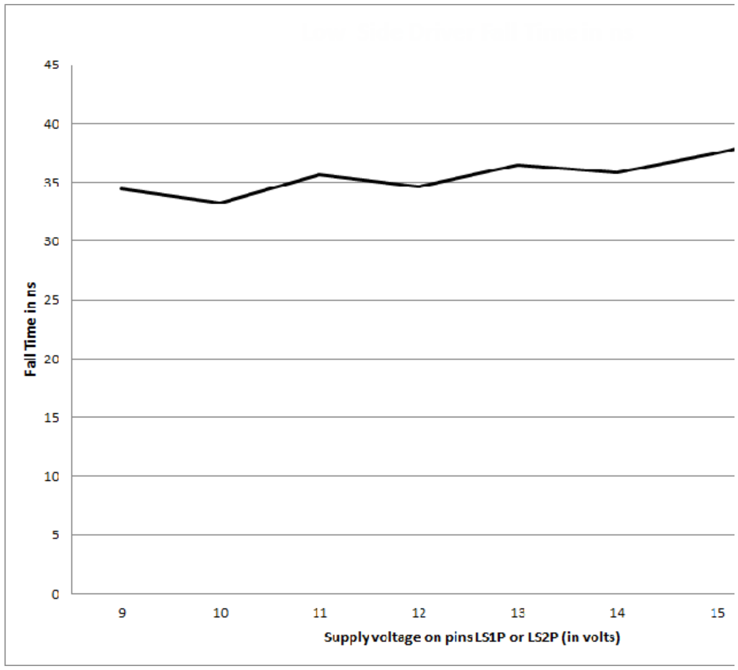


Figure 9 - Low side driver (LS1G or LS2G) fall time versus supply voltage (pins LS1P or LS2P) at 25°C.

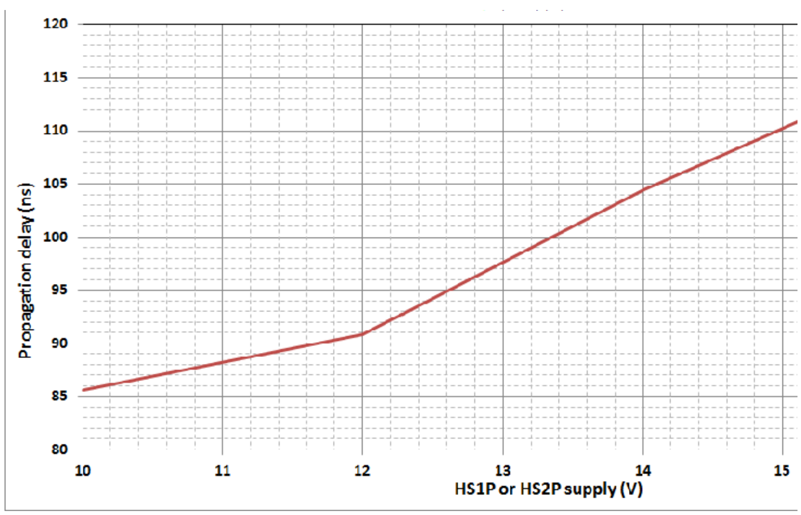


Figure 10 - High side driver (HS1G or HS2G) propagation delay versus supply voltage (pins HS1P or HS2P) at 25°C

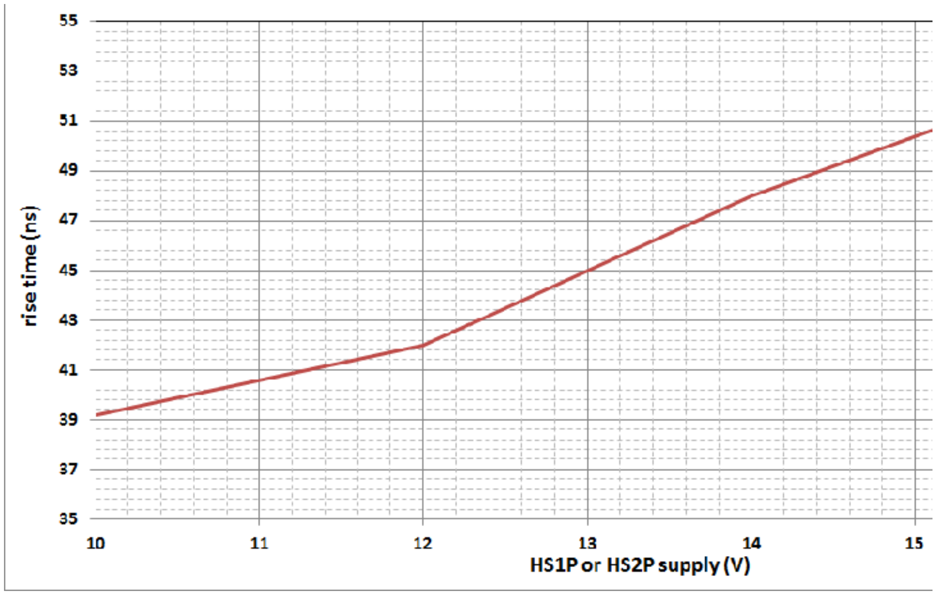


Figure 11 High side driver (HS1G or HS2G) rise time versus supply voltage (pins HS1P or HS2P) at 25^{o}C

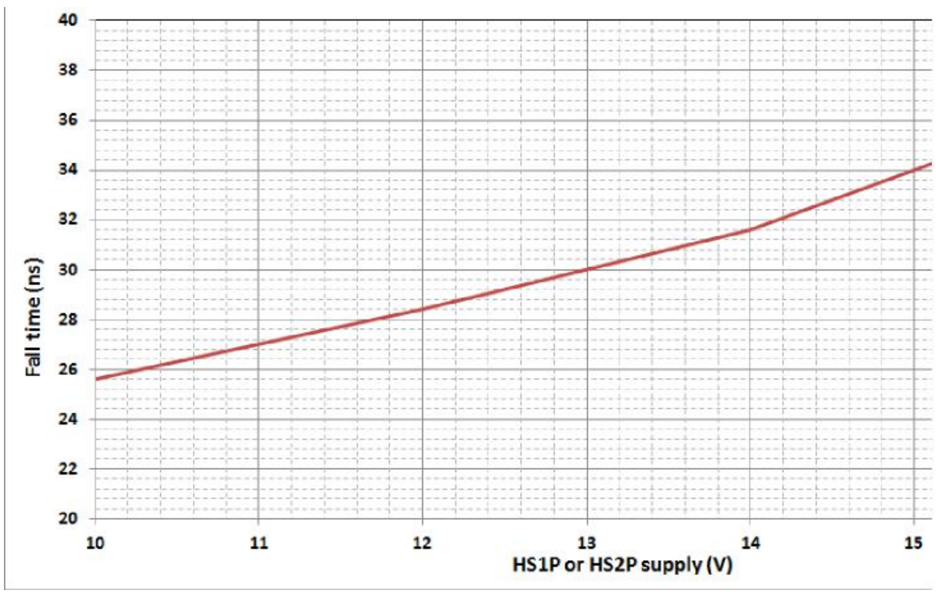


Figure 12 - High side driver (HS1G or HS2G) fall time versus supply voltage (pins HS1P or HS2P) at 25oC

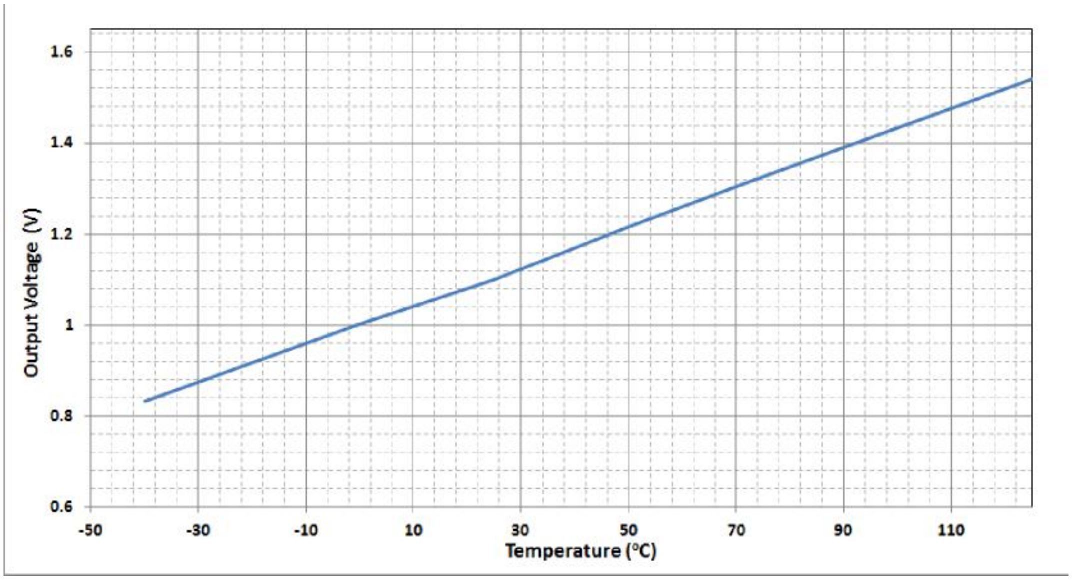


Figure 13 -Temperature sensor output voltage versus temperature

Functional Description

Functional Description

This section describes the functioning of the SA1002 (APM). The SA1002 (APM) has four major functional blocks, which are described in the following sections:

- Power management block
- Signal conditioning block
- High-side and low-side driver block
- I^2C interface

The power management block supplies the SA1002 (APM) blocks and can be used to design isolated power conversion topologies that created necessary output voltage for powering discrete components and ICs for a power conversion system. The signal conditioning and multiplexing block scales the analog sensing signals and monitors the SA1002 (APM) temperature. The high-side and low-side driver control block provides gate signals to the power train MOSFETs. The I^2C serial interface allows for reading and writing of the SA1002 (APM) internal registers.

Power management block

Error! Reference source not found. Figure 14 shows a diagram of the SA1002 (APM) power management block. The power management block consists of a hysteretic controlled flyback switching mode power supply (SMPS) with an integrated 90 V LDMOS switch, four linear voltage regulators, two shunt regulators, and power-on-reset (POR). The flyback controller allows for design of isolated power topologies for example flyback convertor. Adding more secondary windings to the flyback transformer provides isolated supplies for a second-stage of a DC/AC inverter.

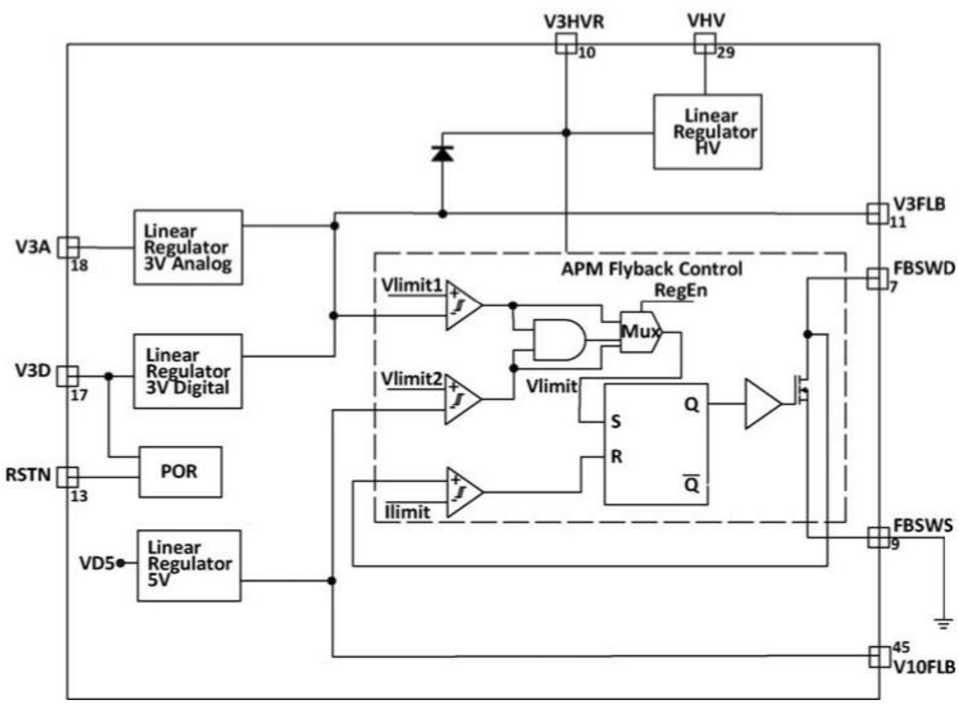


Figure 14 - Power management block.

Pin 29 (VHV/FD3I) has two functions. It is input to the high-voltage linear regulator (VHV) and also it is input to fast divider #3 (FD3I).

Flyback controller with integrated switch

The power MOSFET drain is connected to the primary side of an external transformer which is connected to a high-voltage input (for example, a PV-panel or battery), VHV, and together with the flyback controller switches the current through the primary winding ON and OFF. Figure 15 shows a flyback block diagram. Figure 16 shows a simple flyback supply implemented with a part of the SA1002 (APM) power management block. The flyback controller regulates the voltage on V3FLB pin by a hysteretic control.

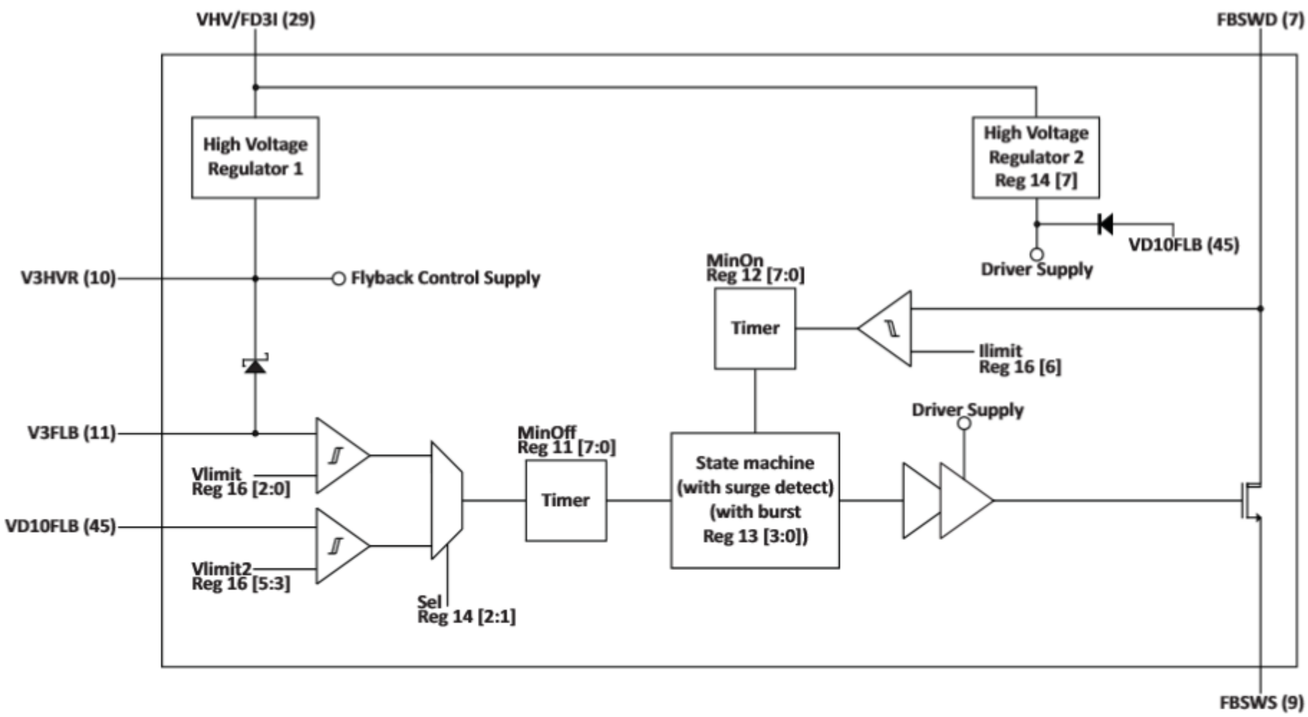


Figure 15- Flyback block diagram.

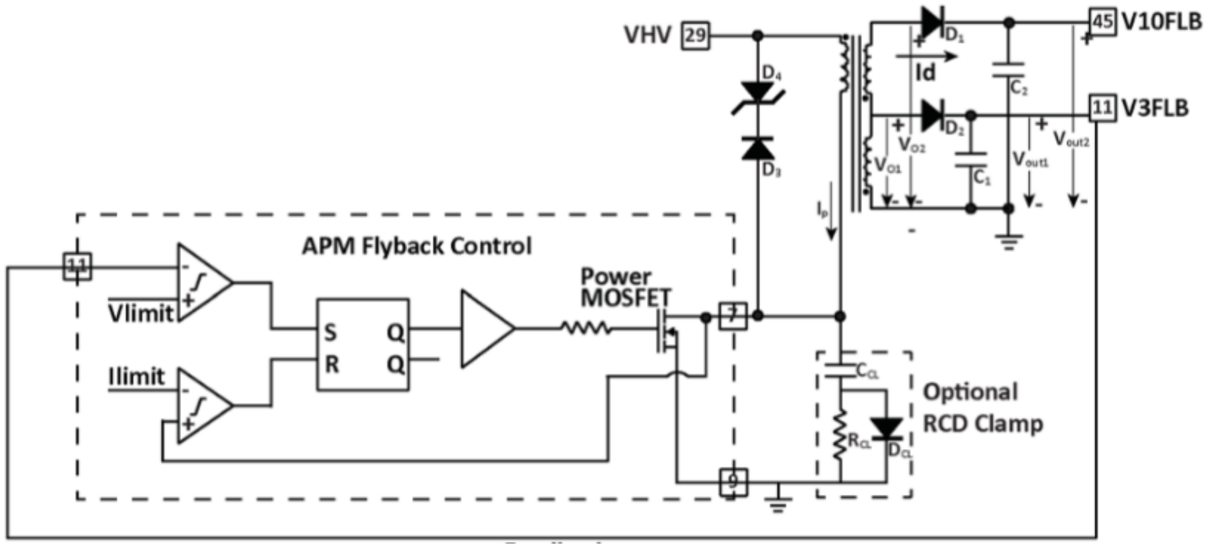


Figure 16 - SA1002 (APM) simple hysteretic flyback supply.

VHV is the input voltage applied to the flyback (for example, by a PV-panel or a battery). V3FLB is the feedback controller input and the directly connected flyback output. By default, this voltage is set to 3.3 V, but can be set from 2.0 V to 3.5 V through an I^2C software register as shown in Table 10 - Flyback V3FLB regulation voltage selection.

Table 10 - Flyback V3FLB regulation voltage selection.

fbc_set3V<2:0>	V3FLB voltage (V)
100	2.0
101	2.2
110	2.4
111	3.0
000	3.3 (Default)
001	3.5
010	unused
011	unused

The maximum rating for the flyback internal power MOSFET is 90 V. Therefore, when the flyback transformer clamp circuitry is designed, the clamping zener diode value should be selected so that the maximum voltage at the MOSFET drain does not exceed 90 V. For better protection, an RCD clamp circuitry can be also added, as shown in Figure 16. The calculations for determining the values for the external components are detailed in the *APM Application Note*.

Flyback operation

The flyback has several operational features:

- startup
- hysteretic (normal) operation
- surge protection
- peak current limit

The following illustration shows the flyback hysteretic operation flowchart.

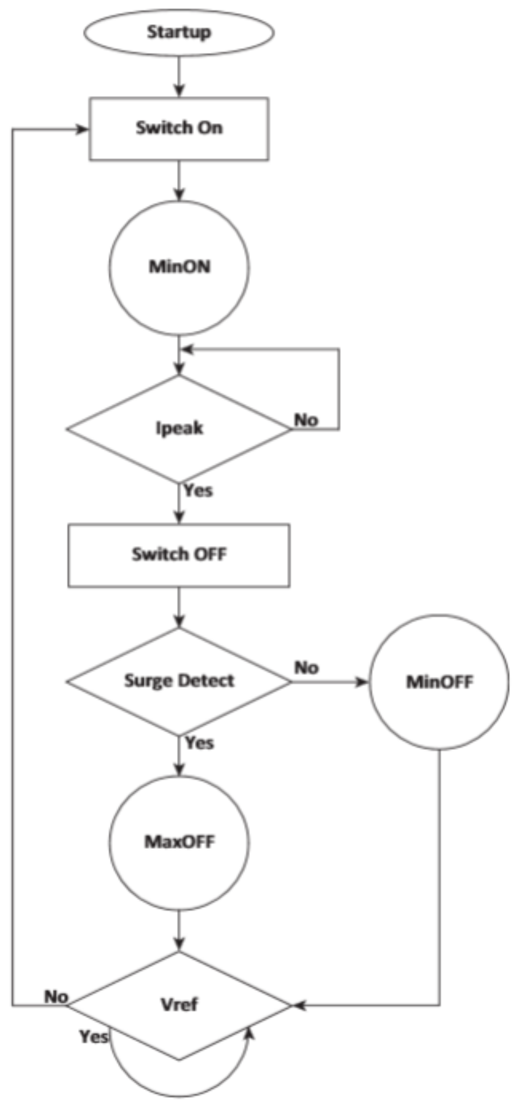


Figure 17- Flyback hysteretic operation flowchart.

Flyback startup mode

During startup, the mode of operation is constant frequency and constant duty cycle. Startup mode ends when **Vlimit** is reached. During this mode, peak current is ramped up by 4 mA every 1000 switching cycles.

Hysteretic (normal) operation

shows an example of the SA1002 (APM) flyback supply waveforms and parameters. In Table 11are given flyback waveform parameters and registers for the settings. The I^2C serial interface is used for controlling the switching parameters.

The MOSFET drain current, **Ip**, on the primary side, is sensed and used by the flyback controller to control the switching. When the supply output voltage, **V3FLB**, falls below the reference voltage, **Vlimit**, the switch is turned ON and the current begins to flow in the primary winding. After the initial current transient, the drain current begins to rise. When the current reaches the peak current threshold, **Ilimit**, the switch is turned OFF and the primary voltage rises quickly above **VHV**, settles, and begins to resonate with the parasitic capacitance. The transformer's secondary winding voltages are rectified by the diodes and filtered by the output capacitors.

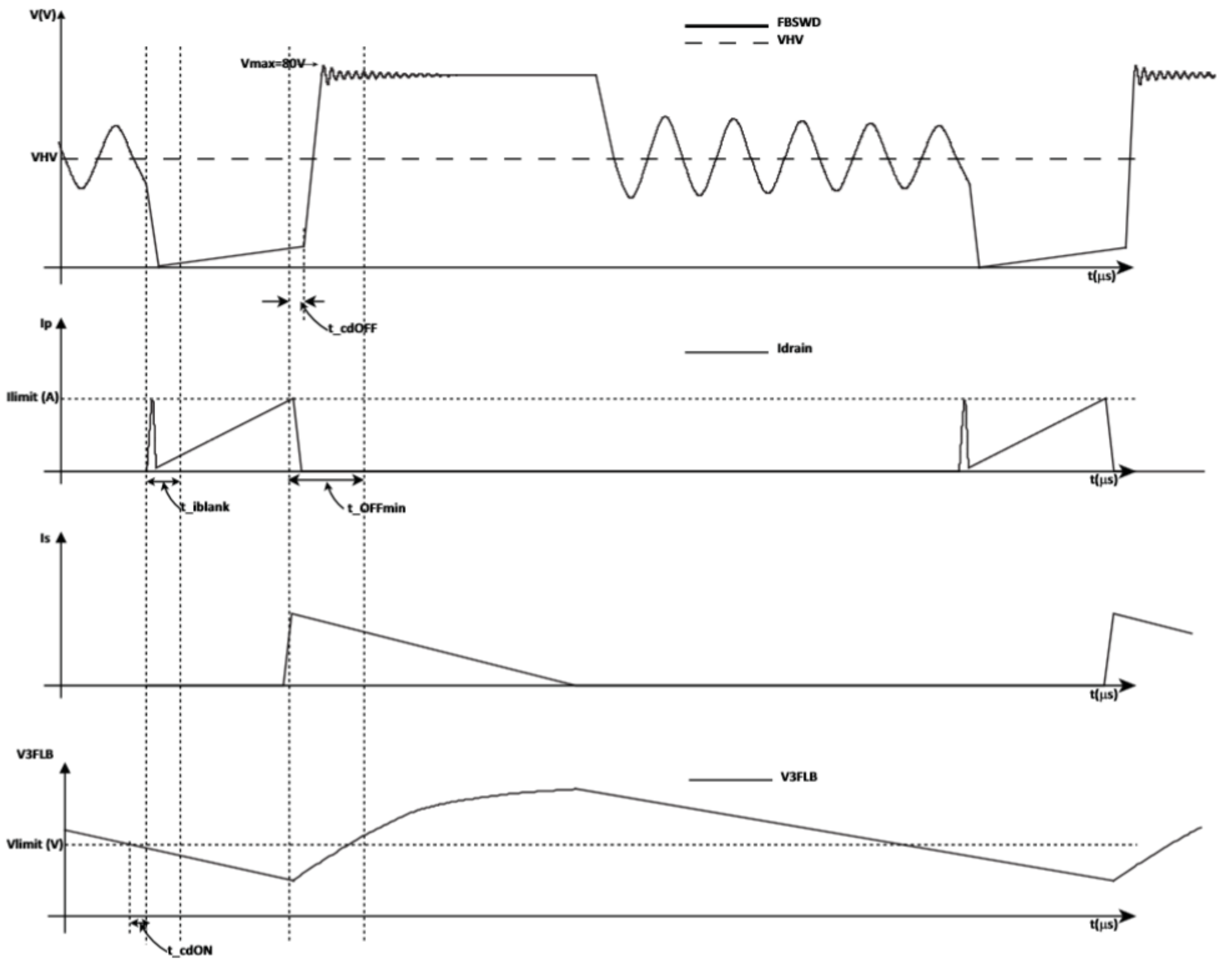


Figure 18 - SA1002 (APM) flyback hysteretic waveforms and settings.

Table 11 - SA1002 (APM) flyback waveform parameters and registers for the settings

Parameter	Register	Description
t_OFFmin	fbc_minOff	Number of clock cycles for minimum time OFF.
t_iblank	fbc_minON	Number of clock cycles for minimum time ON.
Ilimit	fbc_enHiCrt	Peak threshold current
Vlimit	fbc_set3V	Sets the reference voltage for turning ON the switch when the drain voltage falls the below the limit. The bits fbc_allRegEn and fbs_v12RegEN should be low.
T_cdON	NA	Fixed, inherent - Turn ON delay - circuit delay from time voltage crosses Vlimit to time switch is turned ON.
T_cdOFF	NA	Fixed, inherent - Turn OFF delay - circuit delay from time current crosses Ilimit to time switch is turned OFF.

The hysteretic flyback controller is augmented with a programmable valley-detection state machine that can be programmed to search for the minimum voltage of the LC resonance so that the MOSFET can be switched back ON with minimal switching loss (soft switching).

The regulated threshold voltage, **Ilimit**, is proportional to the MOSFET current and can be can be set through the serial interface to 0.2 A or 0.4 A (refer to Table 11). The **Ilimit** values shown are settable through the programming register bit Fbc_enHiCrt (register 16, bit 6).

Table 12 - Peak threshold current settings

Fbc_enHiCrt	Ilimit (A)
0	0.2
1	0.4

The flyback controller shuts down when the die temperature reaches approximately 145^{o}C (typical). Operation resumes when the temperature falls below approximately 85^{o}C (typical) or if the voltage on V3D drops below 2 V. The over-temperature shut-down circuit can be disabled via the I^2C interface.

The minimum MOSFET OFF and ON times, t_OFFmin and t_iblank, are specified in register fbc_min_Off[7:0] and register fbc_min_ON[7:0]. The minimum on time also serves as the hold-off or blanking time for the current comparison, so that the current-comparator output is ignored during turn-ON transients.

The flyback timing is provided by an internal free-running 50 MHz switch oscillator (±20%). The ON and OFF time intervals are calculated by multiplying the oscillator period by the register values fbc_min_Off and fbc_min_On. By default, the flyback controller is clocked from the 50 MHz oscillator. If the fbc_oscLowSpeed bit is set, the clock is reduced to approximately 12 MHz. Further, the clock can be divided down for ultra-low speed operation (for example, for a transformer with very large inductance) using the fbc_clkDiv[2:0] bits. The clock divider is 2^{N-1}, where N is the 3-bit value set in fbc_clkDiv[2:0] register.

The two circuit delay times, the turn ON circuit delay t_cdON, and the turn OFF circuit delay t_cdOFF, as seen in Figure 18 are defined as follow:

- Turn ON circuit delay, t_cdON, is the time from when the output regulated voltage falls below **Vlimit** to the time when the switch is turned ON.
- Turn OFF circuit delay, t_cdOFF, is the time from when the drain current rises above **Ilimit** to the time when the switch is turned OFF.

Surge protection

If the drain voltage does not go below Ilimit(V) (internal reference) when the switch is ON, then the OFF time is expanded to 20 μs to ensure protection of the IC. Waveforms for surge detection/protection are shown in Figure 9 on page 15.

Peak current limit

The peak current limit is the point at which the drain voltage crosses **Ilimit**(V) (internal reference).

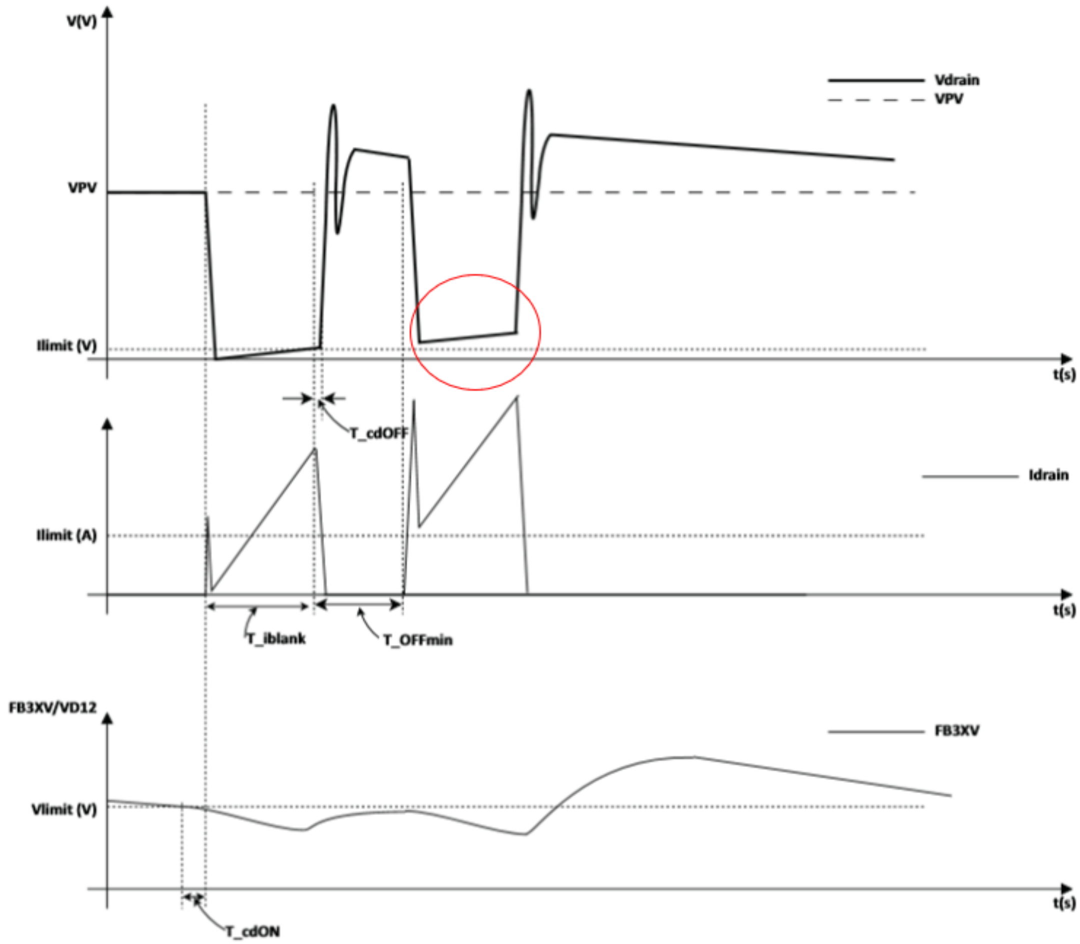


Figure 19 - Surge detection/protection waveforms.

Other flyback modes of operation

The hysteretic voltage mode control of flyback operation, as detailed in the previous section, is the default mode of operation. The SA1002 (APM) supports two other modes of flyback operation; simple mode and burst mode.

Simple mode

In the simple mode of flyback operation the flyback feedback loop ignores valley search and peak current optimization. Bit fbc_enaSimple in register 14 is set high.

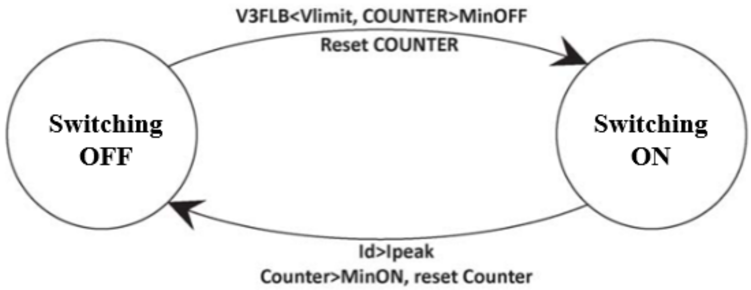


Figure 20 - Simple mode of flyback operation.

Burst mode

The hysteretic flyback controller can regulate the output voltage in a burst mode. Burst mode improves efficiency by finding a better point for quasi-resonant operation, but it also increases the output voltage ripple.

In burst mode, Vlimit is ignored for a set number of flyback cycles when the flyback cycle switch is turning ON and then OFF. The number of bursts is controlled by fbc_delta<3:0> in register 13. Care must be taken especially under light or variable loads as an over-voltage situation can be created for high values of fbc_delta. Figure 11 on page 16 illustrates the burst mode algorithm.

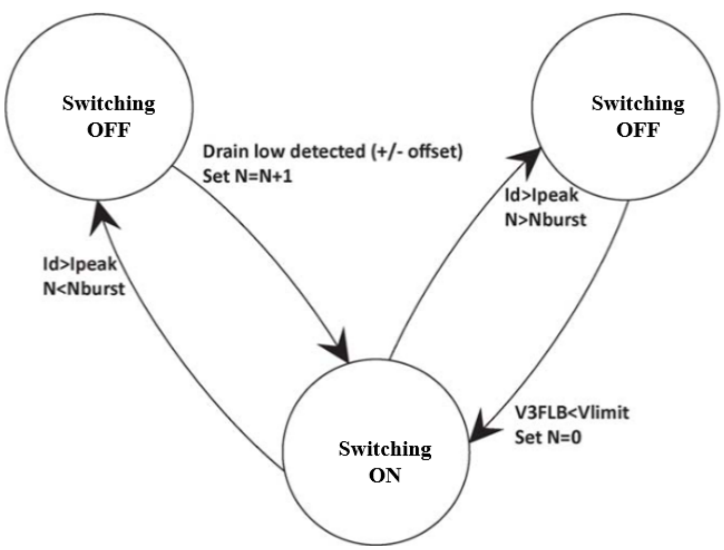


Figure 21 - Burst mode of flyback operation.

Linear regulators

As shown in Figure 14, the SA1002 (APM) power management block has four linear regulators. A high-voltage regulator is supplied directly from the VHV pin and generates the start-up voltage (typically 2.8 V), which is available on pin V3HVR. The high-voltage regulator and its associated bandgap reference consume approximately 200µA from the primary supply input, VHV.

The high-voltage linear regulators are in standby mode when V3FLB and V10FLB voltages are provided by the flyback regulator to the SA1002 (APM) inputs. If flyback regulation is turned OFF by setting control bit top_FBCenB high, then high-voltage linear regulators inside of the SA1002 (APM) are turned on automatically.

Voltage regulation threshold Vlimit

The VHV signal is the primary voltage supplied from to the flyback circuit (from a PV-panel or the battery, for example). Once VHV is above 6 V, the HV linear regulator generates a 2.8 V start-up voltage on pin V3HVR. This supply is used to start the flyback controller which starts regulating, and its output voltage, V3FLB, becomes approximately 3.3 V. When 3.3 V is reached on V3FLB, an internal signal from the flyback controller enables the analog and digital linear regulators, generating 3 V on V3A and V3D. The two regulators are intended to supply limited power to external devices (50 mA per output, ~300 mW in total). V3D also supplies the digital I/O pins that interface with the system controller via pin V3D1 (pin 5). System power-on-reset (POR) is generated by V3D. The external pin RSTN is an open collector output that is connected to an external pull-up resistor, and is driven from the internal POR signal. When the power-on-reset is high, it disables RSTN, and the SA1002 (APM) begins normal operation.

DC-side startup sequence with power from a PV-panel

The DC-side startup sequence is summarized as follows:

1. Voltage higher than 6 V is applied to VHV.
2. SA1002 (APM) internal circuitry wakes up and starts the flyback.
3. All devices - the SA1002 (APM) and other devices are all now powered, but may have slightly different supply rise times, and slightly different timing for the release of internal POR signals.
4. The SA1002 (APM) disables RSTN.

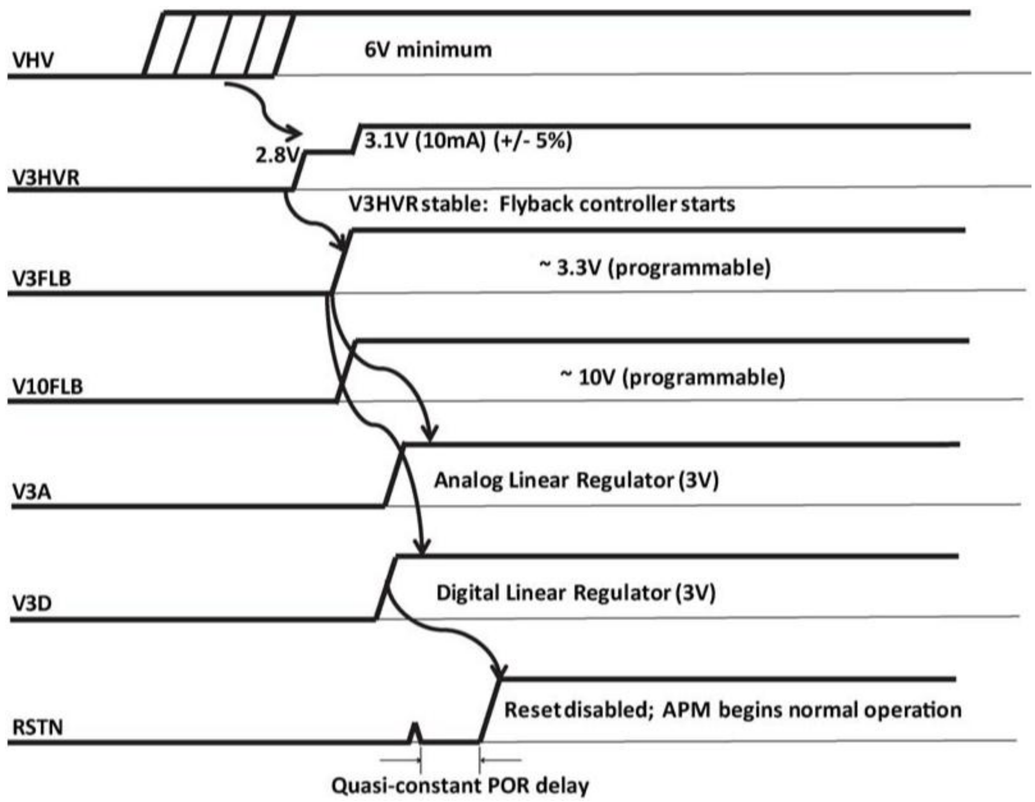


Figure 22 - SA1002 (APM) power management block timing diagram.

Disable control signals for the power management block

The following register bits are used to disable the power management block functions:

- bit top_dsg disables all analog blocks except for the regulators, bandgap, and the flyback
- bit top_lr3enB disables all regulators except for bandgap
- bit lrg_LRA3enB and lrg_LRD3enB disable the analog and digital regulators
- bit lrg_BGenB disables the bandgap
- bit bgr_enB disables the bandgap replicator. When disabled it sends out bandgap current.

Other power management control signals

The voltage regulation point for the analog and digital 3 V regulators can be set to 3.0 V or to 3.2V by setting bits lrg_aset and lrg_dset low for 3.0 V or high for 3.2 V.

The flyback regulator can use the V10FLB input by setting fbc_v12RegEn high. When fbc_v12RegEn is low (the default) the regulator input is V3FLB.

The flyback regulator can use both V10FB and V3FLB inputs by setting the bit fbc_allRegEn high. Otherwise regulation is on individual pins, depending on the setting of bit fbc_v12RegEn.

Note that when V10FLB is used, the flyback regulation voltages are programmable using bit fbc_set12V.

Signal conditioning block

To optimize the efficiency of DC-AC micro-inverters, DC-DC power optimizers, and intelligent disconnect switching products, some of the signals need to be sensed and conditioned during operation. An example of the sensing of signals of a DC-DC converter is shown in Figure 23 The SA1002 (APM) signal conditioning and multiplexing block diagram is shown in Figure 24. The block conditions two types of analog sensing signals:

- fast high-voltage sensing signals with a bandwidth of 20 MHz
- precision high-voltage sensing signals with a precision of 0.5% and a bandwidth of 1 MHz

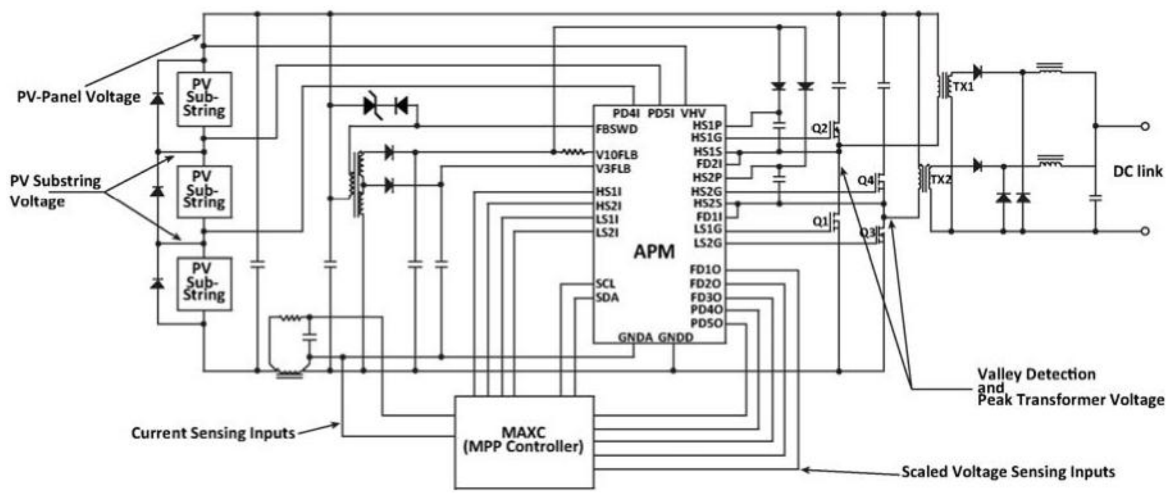


Figure 23 - Signal sensing in a DC-DC converter.

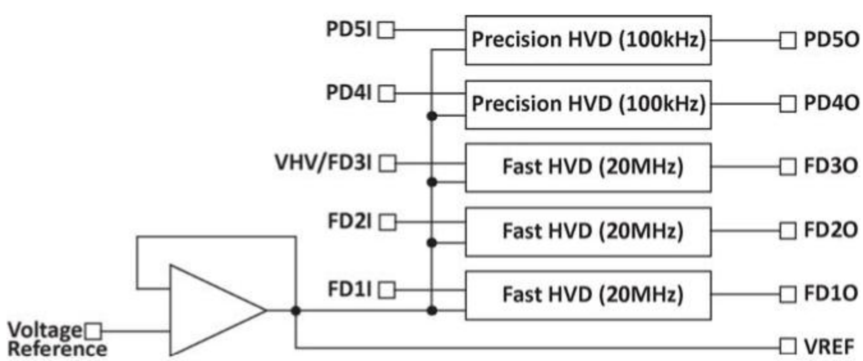


Figure 24 - APM signal conditioning and multiplexing block diagram.

The high-voltage analog inputs for the three fast high-voltage dividers are FD1I, FD2I, and FD3I. The scaled down inputs are presented on low-voltage analog outputs FD1O, FD2O, and FD3O. The VHV/FD3I input is dual function; VHV is for the power management block, and FD3I is for the signal conditioning block. The high-voltage inputs for the two precision high-voltage dividers are PD4I and PD5I. The scaled down inputs are presented on low-voltage analog inputs PD4O and PD5O.

To minimize the effects of common mode noise between ICs, both of the outputs are referenced to a voltage, VREF. When the high-voltage analog inputs set to 0 V., the dividers output are VREF. The VREF value is programmable using register bit hvd_refHi with VREF =125 mV when the bit is set to 0, and 250 mV when the bit is set to 1.

The buffering operation control register bits for generic control of all of the voltage dividers are as follows:

- hvd_refenB enables (set low) the reference generator
- hvd_opaEnb enables (set low) op-amps (buffers) for dividers
- hcd_SDOAenB enables (set low) slow divider op-amps (buffer and level-shift)

Fast high-voltage dividers

The three fast high-voltage analog inputs, FD1I, FD2I, and VHV/FD3I can be used for sensing the voltages of two power train switching nodes and a high voltage source, for example. Figure 25 shows a simplified circuit diagram of the 80 V programmable voltage dividers with pseudo-differential analog outputs. Variable voltage division ratios implemented internally are 1/64, 1/32, 1/16, and 1/8.

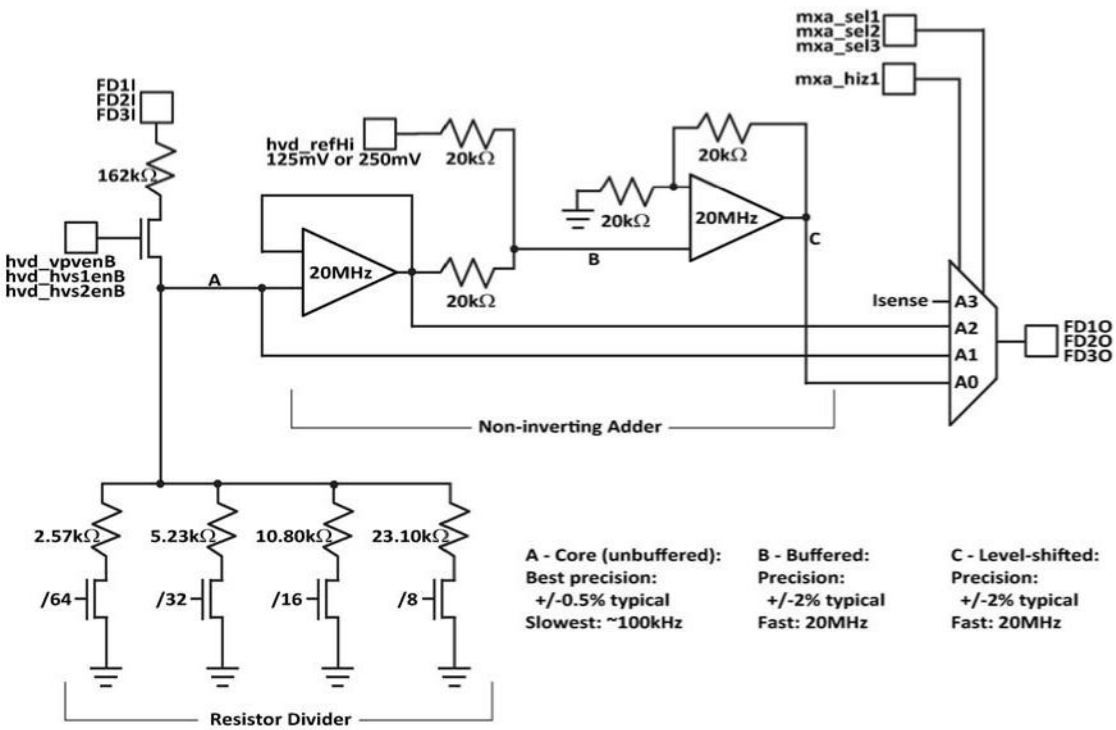


Figure 25 - Fast high-voltage divider functional block diagram.

The voltage divider ratio for fast dividers is selected by the bits hvd_hvs1[2:0] for the first divider, hvd_hvs2[2:0] for the second divider, and hvd_vpv[2:0] for the third divider. The voltage divider selection ratio is given in Table 13. The divider ratio electrical pairs are independently selectable for each sense signal.

Table 13 - Fast voltage divider ratio selection

hvd_hvs*X**[2:0] and hvd_vpv[2:0]	Voltage division ratio

000	64
001	32
010	16
011	8
100	NA
101	NA
110	Force zero (for calibration)
111	OFF (power down)
* *X* is 1 or 2, depending on the selected divider.	

The resistive divider output is buffered and then summed with VREF by a non-inverting adder. The level-shifting of the output with VREF signal minimizes the effects of common mode noise between ICs. For a default state the output signals are:

$$FDxO = \frac{R_{SEL}}{R_F + R_{SEL}} FDxI + V_{REF}$$

where: *x*=1, 2, or 3

RSEL= 2.57 kΩ for /64
5.23 kΩ for /32
10.8 kΩ for /16
23.1 kΩ for /8

RF = 162 kΩ

All thee output options, unbuffered, buffered with no level shifting, or buffered with level shifting, can be selected via the state of the mxa_sel1<1,0> bits of the serial interface register 8. The internal sensing point, Vbg or Lbg (When bgr_enB is low, it is Vbg (this is the default). When bgr_enB is low, it is Ibg), for bandgap is output on pin FD1O, temperature is output on FD2O, and VREF is output on FD3O. The control register with the mode selection is detailed in Table 14 .

Table 14 -Fast dividers mode selection.

mxa_sel1<1:0>	Slow sensor output function
00	Buffered, level-shifted by VREF
01	Unbuffered, no level shifting
10	Buffered, no level shifting
11	Internal sensing: VREF - FD3O bandgap - FD1O

The unbuffered output provides the best precision +/-0.25% typical with calibration, or +/-0.5% without calibration. The bandwidth is approximately 100 kHz. The buffered output, with or without level-shifting, has a precision of +/-2% typical, and a bandwidth of 20 MHz.

Each of the fast high-voltage dividers is enabled individually by setting the corresponding control register bits hvd_hvs1enB, hvd_hvs2enB, and hvd_vpvenB to 0. The fast dividers can be disabled by setting the divider ratios of bits hvd_hvs1[2:0], hvd_hvs2[2:0], and hvd_vpv[2:0] to 111. When a divider is disabled, the high-voltage MOSFET switches turn off the sensing paths so that there is no current drawn from the sensed node. When set to 110, the high-voltage switches are disabled, but all bottom switches are enabled, forcing zero output from the resistive divider.

Precision high-voltage dividers

The two precision voltage analog inputs, PD4I and PD5I, can be used, for example, to sense the voltage of the PV-panel and the substring voltages as shown in Figure 23. In Figure 26a simplified circuit diagram for the 80 V programmable voltage dividers with power-down and pseudo-differential analog output are shown. Variable voltage division ratios implemented internally are 1/64, 1/32, 1/16, and 1/8.

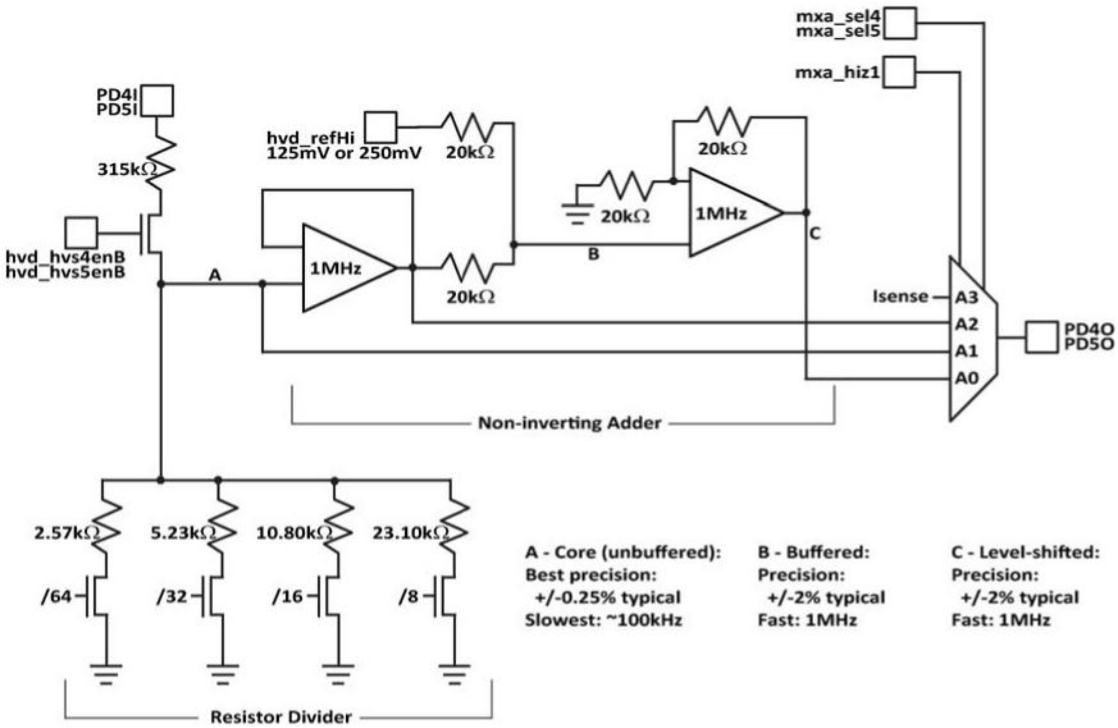


Figure 26 - Precision high-voltage divider functional block diagram.

The divider ratios can be set by programming the bits hvd_hvs4[2:0] and hvd_hvs5[2:0]. The voltage divider ratio selection is shown in Table 15. They are independently selectable for each input signal. Better precision can be achieved after offset/gain calibration of the system is complete.

Table 15 - Precision voltage divider ratio selection.

hvd_hvs*X*<2:0>	Voltage division ratio
000	64
001	32
010	16

011	8
100	NA
101	NA
110	Force zero (for calibration)
111	OFF
* *X* = 3 for divider 1, *X* = 4 for divider 2, and *X* = 1 for divider 3.	

The resistive divider output is buffered and then summed with VREF by a non-inverting adder. The level-shifting of the output with VREF signal minimizes the effects of common mode noise between ICs. For a default state the output signals are:

$$PDxO = \frac{R_{SEL}}{R_F + R_{SEL}} PDxI + V_{REF}$$

PD*x*O = RSEL/(RF+RSEL)*PD*x*I+VREF

where: *x* = 4 or 5

R_{SEL}= 2.57 kΩ for /64
5.23 kΩ for /32
10.8 kΩ for /16
23.1 kΩ for /8

R_F=315 kΩ

All four output options, unbuffered, buffered with no level shifting, buffered with level shifting, or internal sensing, can be selected via the state of the mxa_sel4<1,0> and mxa_sel5<1,0> bits of serial interface register 8. The internal sensing point for the flyback high-temperature flag, fbc_hitempF is output on pin PD4O, and internal temperature is output on PD5O. The control register with the mode selection is detailed in Table 16.

Table 16 - Precision dividers mode selection

mxa_sel*X*<1:0>	Slow sensor output function
00	Buffered, level-shifted by VREF volts
01	Unbuffered, no level shifting
10	Buffered, no level shifting
11	Flyback temperature indicator - PD4O temperature sensing - PD5O
* *X* = 4 for precision divider 4, *X* = 5 for precision divider 5	

The scaled output of the inputs PD4I and PD5I are presented on PD4O and PD5O. Precision high-voltage divider 4 is enabled by bit hvd_hvs4enB=0, precision high-voltage divider 5 is enabled by bit hvd_hvs5enB=0. By default, the precision high-voltage dividers are enabled.

The unbuffered output provides the best precision +/-0.25 % typical WITH CALIBRATION, or +/-0.5% without calibration. The bandwidth is approximately 100 kHz. The buffered output, with or without level-shifting, has a precision of +/-2% typical, and a bandwidth of 1 MHz.

The precision dividers can be disabled by setting the divider ratios of bits hvd_hvs4[2:0] and hvd_hvs5[2:0] to 111. When a divider is disabled, the high-voltage MOSFET switches turnOFF the sensing paths so that there is no current drawn from the sense node.

Temperature sensing

The temperature sensor operates over a temperature range of - 40^{o} C to +125^{o} C. The temperature reading is analog-multiplexed by the serial interface control onto the FD2O or PD5O outputs. Setting the two bits of mxa_sel1 or mxa_sel5 to high causes the temperature to be output on FD2O or PD5O.

The status flag for the over-temperature protection is analog multiplexed by the serial interface control onto PD4O. Setting the two bits of mxa_sel4 to high causes the status flag to be output on PD4O. A high on this output indicates an over-temperature condition.

High-side and low-side driver block

The SA1002 (APM) includes four custom level-switching MOSFET gate drivers for implementing a variety of power-conversion topologies. These drivers convert the logic-level inputs LS1I, LS2I, HS1I, and HS2I to MOSFET drive signals LS1G, LS2G, HS1G, and HS2G with internal controls that implement under-voltage lock-out and cross-conduction protection. The ground of the high-side drivers can float up to 80 V.

The drivers can be supplied with either standard driver supply levels (9 V to 15V) or with logic-level power MOSFET supply levels (4 V to 6V). The under-voltage lock-out (UVLO) levels are programmable to allow for the two types of driver supply.

Figure 27 shows the block diagram for the high-side and low-side drivers with the outputs connected to the MOSFETs of a full-bridge topology. The driver block includes:

- Two low-side drivers (LSD) with two levels of programmable UVLO (4 V or 8 V)
- Two 80 V high-side drivers (HSD) with up to 80 V floating ground and independent programmable UVLO option to prevent inadvertent turn-off/on and destruction of the power train switches when the driver supply voltage falls below a certain threshold.

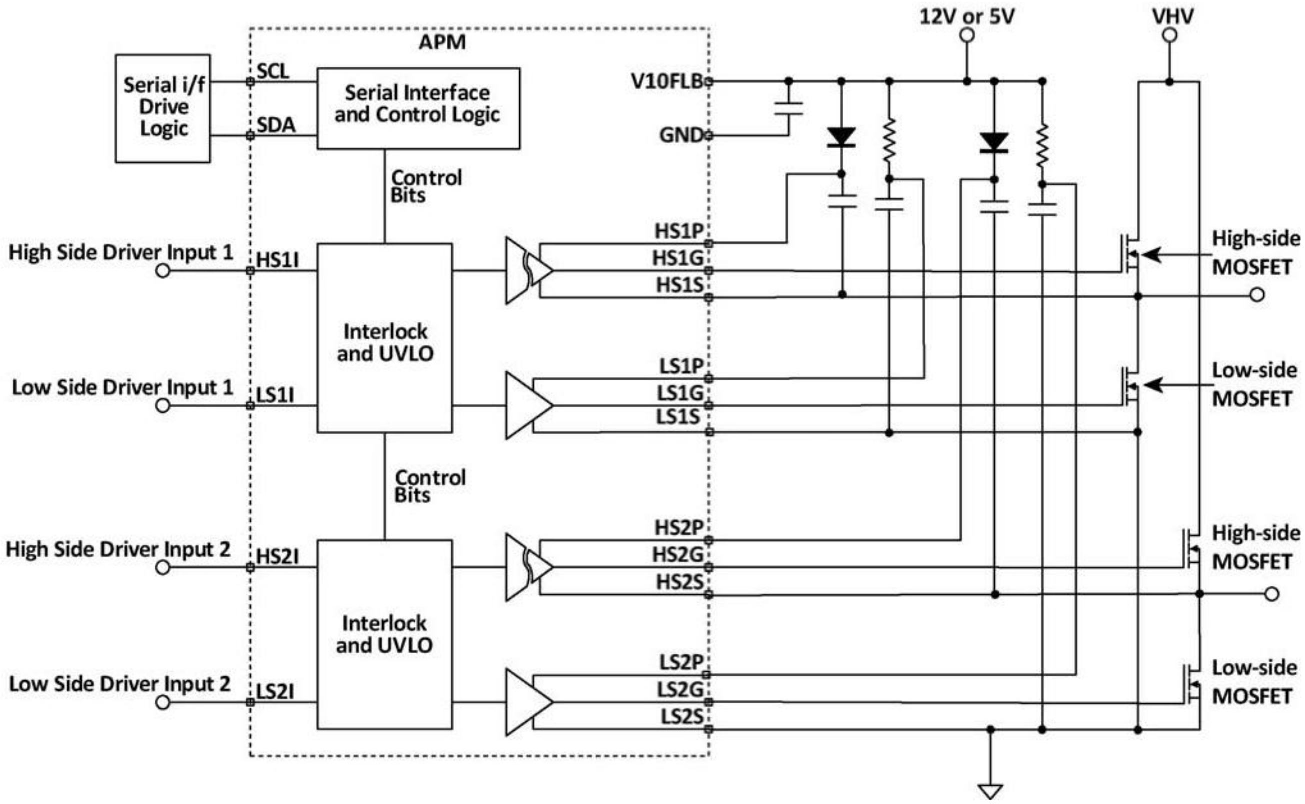


Figure 27 - High-side and low-side drivers block diagram.

Gate drive currents

A gate driver must provide a high enough output current to charge the equivalent gate capacitance of the switch within the time required by the system design. This ensures that the driving of the MOSFET gate operates without excess ringing and with minimum switching times. It is strongly recommended that the driver outputs, HS1S and HS2S, and LS1S and LS2S, be directly connected to the MOSFET source, as seen in Figure 27.

The gate drive currents are most significant to the application circuit during hard switching when the gate is at the gate-source threshold. In this instance, the gate drive current determines the rate at which the charge is transferred to or from the Miller capacitance, and therefore also determines the switching time of the MOSFET.

The gate threshold voltage, sink and source currents vary with temperature and with the MOSFET type used for different applications. The worst case turn-ON is when V_{GSth} is maximum at low temperature. The worst case turn-OFF is when V_{GSth} is minimum at high temperature.

Cross-conduction protection

For converter topologies where two MOSFETs are connected in series, the drain of the lower MOSFET is connected to the source of the upper MOSFET, a minimum dead-time limit is required to eliminate cross conduction caused by the gate drive skew. Cross-conduction protection is enabled by default, but can be disabled with control bit drv_noLock. The minimum dead-time for preventing a cross-conduction condition is a function of the maximum skew time between turn-OFF of one of the MOSFETs and turn ON of the other MOSFET.

An example of cross-conduction events are shown in Figure 18 on page 26.

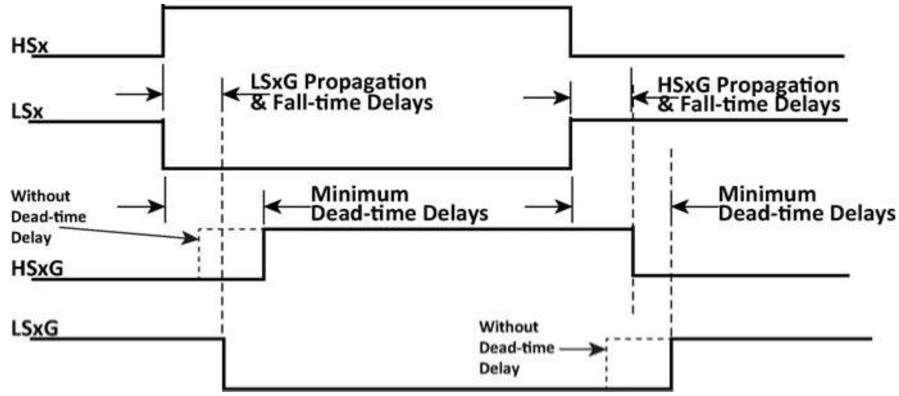


Figure 28 -Cross-conduction event due to the drivers' propagation delays.

Although the two driver inputs are not cross conducting, due to the drivers' propagation delays both the upper and lower MOSFETs are simultaneously in their turn-on state. In this case, cross-conduction protection is necessary. Using the cross-conduction protection, both MOSFETs will never be on at the same time, as shown in Figure 29.

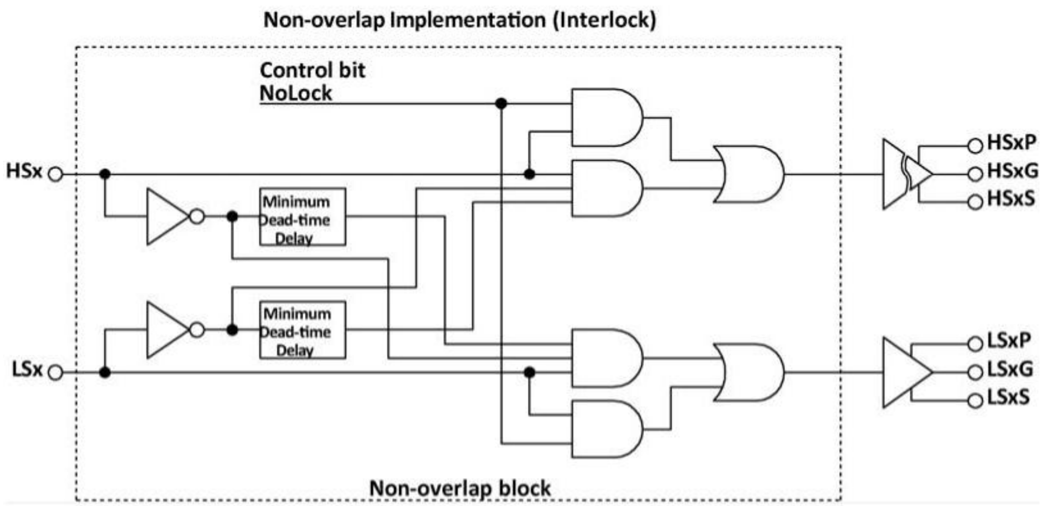


Figure 29 - Driver non-overlap and minimum dead-time implementation.

In some instances, the gate control signals HS1I and HS2I, and LS1I and LS2I may overlap. Some causes of cross-conduction are propagation delays, rise-time delays, and fall-time delays. There are multiple components contributing to a delay for MOSFETs hard-switching:

- driver delay variation
- driver current variation
- MOSFET gate source capacitance variation
- MOSFET gate-to-source threshold voltage variation
- MOSFET gate resistance variation
- MOSFET gate drain capacitance variation

Non-overlap and minimum dead-time

Variations in timing delays can result in simultaneous conduction of MOSFETs even if the drivers are configured to prevent an overlap. To prevent an overlap condition, a minimum dead-time must be set such that the dead-time is greater than the worst case combination of the maximum delay on the MOSFET that is turning off and the minimum delay on the MOSFET that is turning on. Figure 19 on page 27 shows a block diagram of the driver non-overlap and minimum dead-time implementation. The non-overlap function can be disabled with a control bit setting (drv_noLock). By design the minimum dead-time is 50 ns.

High-side and low-side driver under-voltage lock-out (UVLO)

The SA1002 (APM) includes a mechanism to detect an under-voltage condition on the supplies of the drivers to prevent the driving of the power MOSFETs with a gate drive that is too low. This mechanism ensures complete switching of the MOSFETs. The SA1002 (APM) is programmable to drive MOSFETs at the logic-level of 5 V or at the standard level of 10 V.

The UVLO threshold voltage can be set by control bits of register 3, drv_hsdUVsetHi and drv_lsdUVsetHi. Setting the control bit high enables the threshold voltages for 5 V MOSFET gate drives, while setting the control bit low enables the threshold voltages for 10 V MOSFET gate drives. By default, the threshold voltage is set for 10 V MOSFETs. The control bit drv_hsdUVlck of register 3 can be used to set whether a UVLO event on either high-side driver inhibits both drivers or if it inhibits only the associated driver. When the bit is high, both drivers are stopped. The control bit drv_UVLOenB can be used to disable the UVLO circuit for all four drivers. UVLO is enabled by default. Figure 30 shows a diagram of the programmable high-side driver under-voltage lock-out function.

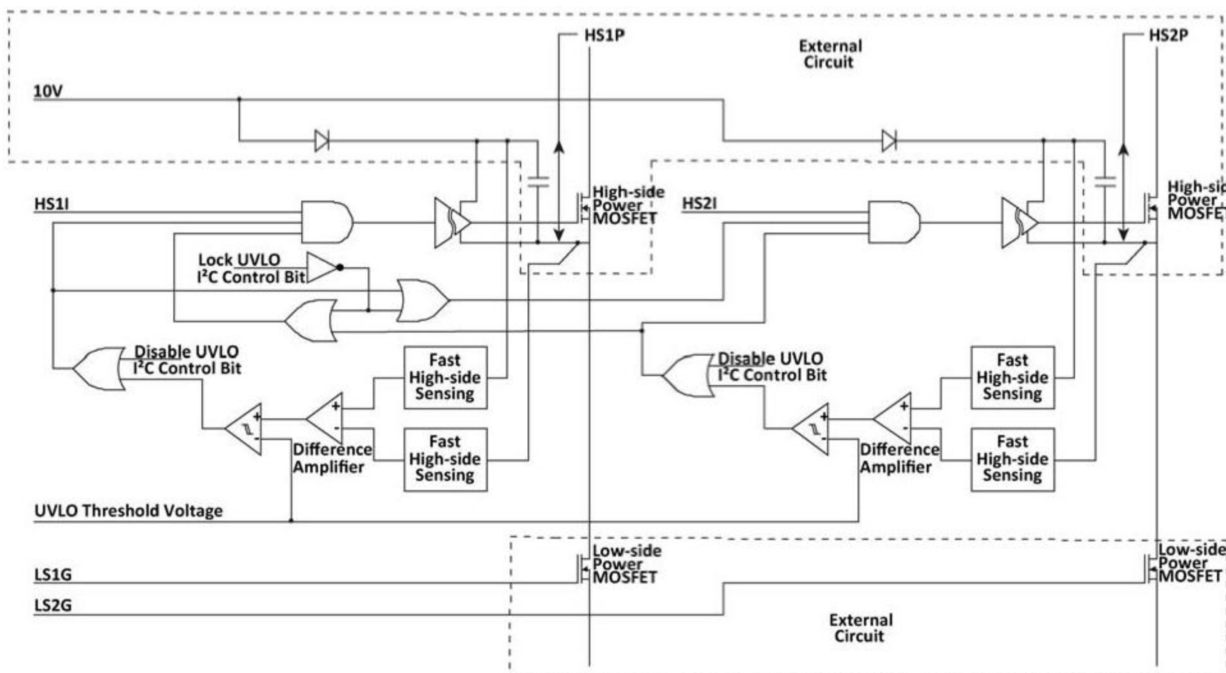


Figure 30 - Programmable under-voltage lock-out.

Figure 31shows a diagram of the high-side UVLO waveforms.

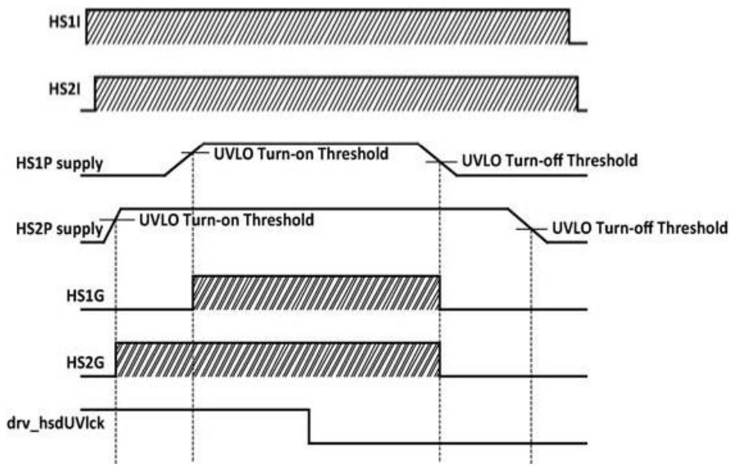


Figure 31 - High-side UVLO waveforms.

Disabling the drivers

The inputs to the low side and high side drivers can be disabled using the register 1 control bits drv_lsdEnb (low side) and drv_hsdEnB (high side) by setting the bits high. When disabled, the inputs are internally forced low.

I^2C interface

The SA1002 (APM) I^2C serial interface allows reading from and writing to internal registers. The registers control the programmable auxiliary flyback regulation, the programmable voltage division and the drivers. The SA1002 (APM) implements the standard-mode 100 kHz slave function only and does not implement clock stretching. The slave device address is hard-coded to 0x00001000 (address 8). Figure 32 shows the I^2C interface clock and data timing diagram.

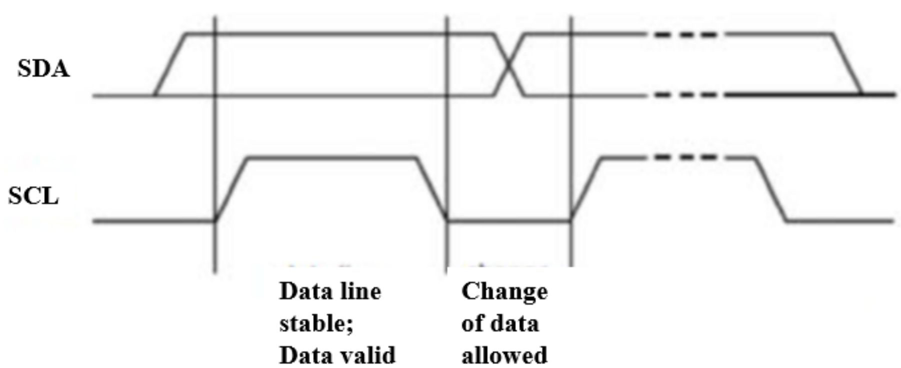


Figure 32 - I2C interface clock and data timing.

As seen in Figure 23 on page 29, serial clock and data timing data on the SDA pin is allowed to change only when the SCL clock is low.

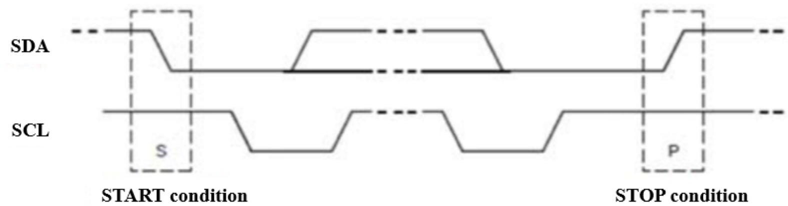


Figure 33 - I²C interface start and stop bits.

The exceptions to this are the start and stop bits. Figure 34 shows a typical data transfer. The transfer begins with the start bit, the device address, and the R/W bit. The addressed slave (that is, the SA1002 (APM)) responds with the ACK (or NACK) bit, and then a sequence of acknowledged 8-bit data transfers occurs.

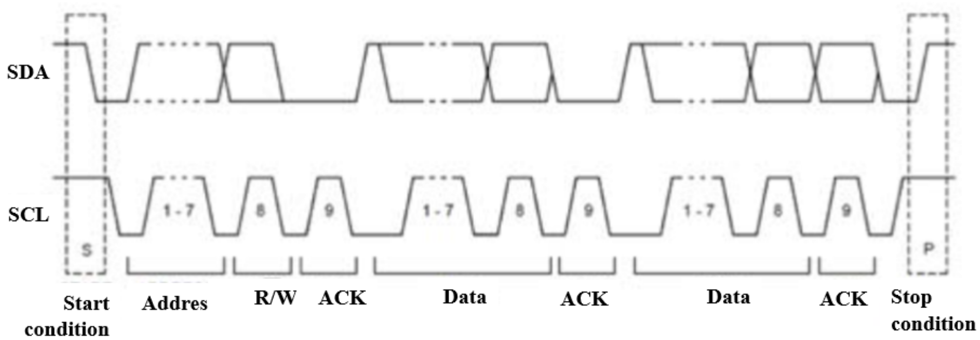


Figure 34 - Serial interface data transfers.

Serial interface registers and bit definitions

Internal registers can be read and written using the I²C interface. For a description of the interface registers, refer to List of registers.

List of registers

Table 17 lists the SA1002 (APM) hardware registers. Note that all registers, except register 0, default to all zeros on power-up.

Table 17 - SA1002 (APM) hardware registers

Register		Description	Settings	Bit name
0 IC HW ID Read-only 16 bits	15:0	16-bit hardware identification number	Fixed at 8230h	
1 General IC enablers / driver controls Read/Write 8 bits	0	Disable all analog block (regulator, bandgap and flyback are still operational)	High - disable	top_dsg
	1	Allows disabling of analog blocks separately (regulator, bandgap and flyback are still operational)	High - disable	top_engB
	2	Disable flyback	High - disable	top_FBCenB
	3	Disable regulators (bandgap is still active)	High - disable	top_lr3enB
	4	Disable input to low side driver (input internally forced low)		drv_lsdEnb
	5	Disable input to high side driver (input internally forced low)		drv_hsdEnB
	6	Disable interlock feature. Both low and high side drivers can be on at the same time.		drv_noLock
	7	Reserved		
2 Regulator settings Read/Write 8 bits	0	Disable analog regulator	High - disable	lrg_LRA3enB
	1	Disable digital regulator	High - disable	lrg_LRD3enB
	3:2	Set voltage regulation point for analog regulator	D0 - 3.0 V D1 - 3.2 V	lrg_aset
	5:4	Set voltage regulation point for digital regulator	D0 - 3.0 V D1 - 3.2 V	lrg_dset
	6	Reserved		
	7	Disable bandgap		lrg_BGenB
3 Driver UVLO settings / Bandgap Settings Read/Write 8 bits	0	Set high side UVLO to logic MOSFETs	High – 4 V Low – 8 V	drv_hsdUVsetHi
	1	Set low side UVLO to logic MOSFETs	High – 4 V Low – 8 V	drv_lsdUVsetHi
	2	UVLO internal debug		drv_hsdUVlck
	3	Disable UVLO circuit		drv_UVLOenB
	4	Spare		lrh_SPARE1
	5	Spare		lrh_SPARE2
	6	Disable bandgap replicator		bgr_enB
	7	Do not use. It disables 5V regulator feedback circuit. If disabled, output will be same as input (Potentially 15V)		lr5_v5enB
4 GPIO controls Read/Write 8 bits	7:0	Reserved		

Register		Description	Settings	Bit name
5 Settings for fast sense dividers Read/Write 8 bits	0	Disable fast high-voltage divider 1 (FD1I)		hvd_hvs1enB
	3:1	Fast high-voltage divider 1 ratio settings	000 – 64 001 - 32 010 - 16 011 - 8 100 - OFF (reserved) 101 - NA 110 - NA 111 - OFF	hvd_hvs1
	4	Disable fast high-voltage divider 2 (FD2I)		hvd_hvs2enB
	7:5	Fast high-voltage divider 2 ratio settings	000 - 64 001 - 32 010 - 16 011 - 8 100 - OFF (reserved) 101 - NA 110 - NA 111 - OFF	hvd_hvs2
6 Settings for PD4I and PD5I Read/Write 8 bits	0	Disable precision high-voltage divider 1 (PD4I)		hvd_hvs3enB
	3:1	Precision high-voltage divider 1 ratio settings	000 - 64 001 - 32 010 - 16 011 - 8 100 - OFF (reserved) 101 - NA 110 - Zero calibration 111 - OFF	hvd_hvs3
	4	Disable precision high-voltage divider 2 (PD5I)		hvd_hvs4enB
	7:5	Precision high-voltage divider 2 divider ratio settings	000 - 64 001 - 32 010 - 16 011 - 8 100 - OFF (reserved) 101 - NA 110 - NA 111 - OFF	hvd_hvs4
7 VHV divider settings/ General divider settings Read/Write 8 bits	0	Disable fast high-voltage divider 3 (VHV/FD3I)		hvd_VHVenB
	3:1	Fast high-voltage divider 3 ratio settings	000 - 64 001 - 32 010 - 16 011 - 8 100 - OFF (reserved) 101 and 110 - NA 111 - OFF	hvd_VHV
	4	Disable reference generator		hvd_refenB
	5	Disable amplifiers in fast dividers used in buffering and level shifting		hvd_opaEnb
	6	Sets VREF reference voltage for analog pseudo-differential outputs	0 - VREF = 0.125V 1 - VREF = 0.250V	hvd_refHi
	7	Enables precision divider OpAmps (buffer and level-shift)	0 - Enable 1 - Disable	hvd_SDOAenB

Register		Description	Settings	Bit name
8 PD4O and PD5O Slow Divider Output Settings Read/Write 8 bits	1:0	FD1O, FD2O, and FD3O divider output settings	00 - Level shifted and buffered 01 - Unbuffered (no level shift) 10 - Buffered FD10: 11 - 1.2V bandgap reference FD20: 11 - Temperature sensor output (Vtemp) FD30: 11 - 0.125V reference	mxa_sel1
	3:2	PD4O divider output settings	00 - Level shifted and buffered 01 - Unbuffered (no level shift) 10 - Buffered 11 - Flyback OverTemp flag	mxa_sel4
	5:4	PD5O divider output settings	00 - Level shifted and buffered 01 - Unbuffered (no level shift) 10 - Buffered 11 - Temperature sensor output (Vtemp)	mxa_sel5
	6	Set all divider outputs to high impedance		mxa_hiz1
	7	ZCD comparators reference level shift value select		Spare
9 Reserved				Reserved
10 Reserved				Spare
11 Flyback setting for minimum time off Read/Write 8 bits	7:0	Number of clock cycles for minimum time off. Blanking time. Write bits = clock cycles XOR 00101110 Clock cycles = read bits XOR 00101110 (Refer to the example following this table for an XOR example.)	Toff=fbc_minOff[7:0]*Tclk Default number of clock cycles = 46	fbc_minOff
12 Flyback setting for minimum time on Read/Write 8 bits	7:0	Number of clock cycles for minimum time on. Blanking time. Write bits = clock cycles XOR 00010100 Clock cycles = read bits XOR 00010100 (Refer to the example following this table for an XOR example.)	Ton=fbc_minOn[7:0]*Tclk Default number of clock cycles = 20	fbc_minOn
13 Flyback burst settings Read/Write 8 bits	3:0	Number of cycles flyback will burst ignoring voltage comparator. Write bits = clock cycles XOR 0001 Clock cycles = read bits XOR 0001 (Refer to the example following this table for an XOR example.)	No_of_burst_cycles = fbc_delta [3:0] + 1 Default burst cycles = 2	fbc_delta
	7:4			Spare

Register	Bit	Description	Settings	Bit name
14 Flyback general settings Read/Write 8 bits	0	Spare		Spare
	1	Enable regulation on Pin 45 (V10FLB). When this bit is set high, then this pin is regulated to value set by fbc_set12[2:0]	1 - Regulate on pin 45 (V10FLB) 0 - Regulate on pin 11 (V3FLB)	fbc_v12RegEn
	2	Regulate on V10FLB and V3FLB. When this bit is set high voltage on pin V10FLB will not drop below voltage set by fbc_set12V[2:0], and voltage on pin V3FLB will not drop below voltage set by fbc_set3V[2:0]. Both conditions are satisfied at the same time.	0 - Regulate on individual pins V3FLB or V10FLB depending on settings on bit fbc_v12RegEn 1 - Ensures that minimum voltage set by words fbc_set3V[2:0] and fbc_set12V[2:0] on pins V3FLB and V10FLB respectively	fbc_allRegEn
	3	Slow down the flyback oscillator.	0 - 50MHz oscillator 1 - 12MHz oscillator	fbc_oscLowSpeed
	4	When set high, flyback feedback loop ignores valley search and peak current optimization state machine.		fbc_enaSimple
	5	Reserved		Reserved
	6	Disable over-temperature protection	0=Enabled 1=Disabled	fbc_tempCntrlEn
	7	Lower regulation on initial driver regulation	0=4.5 V 1=3.5 V	fbc_en35HVLR
15 Flyback settings for current and clock divider Read/Write 8 bits	3:0	Reserved	Keep at default value of 0000	Reserved
	6:4	Clock divider for digital, in case that we want to go to ultra-slow operation (much bigger transformer). Divider is 2^N-1, where N is specified by 3-bit binary word. write bits = N XOR 001 N = read bits XOR 001 (Refer to the example following this table for an XOR example.)	Settings 0 and 1 are the same (divide by 1). The rest follow: Fclk=2^{N-1} Flyback clock = (50 MHz or 12 MHz)/2^{N-1} Default is N=1	fbc_clkDiv
	7	Reserved	Keep at default value of 0	Reserved
16 Flyback settings for regulating voltage and additional current settings Read/Write 8 bits	2:0	Sets regulated voltage on pin V3FLB	100 - 2.0 101 - 2.2 110 - 2.4 111 - 3.0 000 - 3.3 (Default) 001 - 3.5 010 - unused 011 - unused	fbc_set3V
	5:3	Sets regulated voltage on pin V10FLB	101 - 5 100 - 6 111 - 7 110 - 8 001 - 9 000 - 10 (Default) 011 - 11 010 - 12	fbc_set12V
	6	Increases peak current for higher power output	0 – no increase in peak current 1 – add 200 mA to peak	fbc_enHiCrt
	7	Reserved		Reserved

Register		Description	S	Bit name
17 Reserved		Reserved		Reserved
18 Reserved		Reserved		Reserved
19 Reserved		Reserved		Reserved
20 Status Read-only 8 bits	0	High temperature indicator from flyback temperature sensor		fbc_hiTempF
	1	Interlock state for drivers LS1 and HS1		drv_lock1
	2	Interlock state for drivers LS2 and HS2		drv_lock2
	3	UVLO state for drivers		drv_UVLO
	7:4	Spare		Spare

Example of XOR calculation for register 11

The default register value is 00000000. Therefore, the default number of clock cycles is:

```
    00000000
XOR 00100010
  = 00100010 (decimal 34)
```

To change the number of clock cycles from 34 to 40, where 40 is binary 00101000, the value to write is:

```
    00101000
XOR 00100010
  = 00001010 (value to write to register 11)
```

Note: Occasionally some or all APM internal register content can be corrupted due to excessive noise. This behavior is more frequent on boards that have a high level of noise due, typically, to heavy switching in its proximity. Another source of failure is a voltage on APM pin 29 (VHV/FD3I) that is out of operational specification. A good PCB design will reduce this failure significantly but will not necessarily eliminate it.

To work around this issue, the targeted APM register content should be written periodically. This can be done a few times per second with a non-critical process running in the main loop of the processor that is connected to the APM via the I^2C port.

Applications, Implementation and Layout

Application

The SA1002 (APM) integrated circuit contains essential functions for building power conversion systems such as DC-AC micro-inverters, DC-DC power optimizers and intelligent disconnect products. AMP has two precision and three fast voltage dividers for analog sensing, a flyback controller with an integrated switch providing 2 W of power (transformer dependent) for on-board supplies, and high-side and low-side MOSFET drivers. The MOSFET drivers are protected against erroneous driving signals on their inputs by embedded cross-conduction protection circuitry.

APM has been used in different applications:

- DC POD and DC- PODX
- MI-P300A
- MI P700A
- ACBI

For example, For MI-300 A, the power manager block with the fly back controller provide around 2 W power to the inverter ICs. The APM four drives control the stolid state switches and the two precision voltage dividers are used, one scaling down the PV voltage and other for scaling down the buck convertor output voltage. An example of MI-P300A APM coupling and flyback circuitries is shown in Figure 35. The APM pins that are not used are grounded. For design of flyback converter using AMP see *Solantro SA1002 (APM) Analog Power Manager Application Note*.

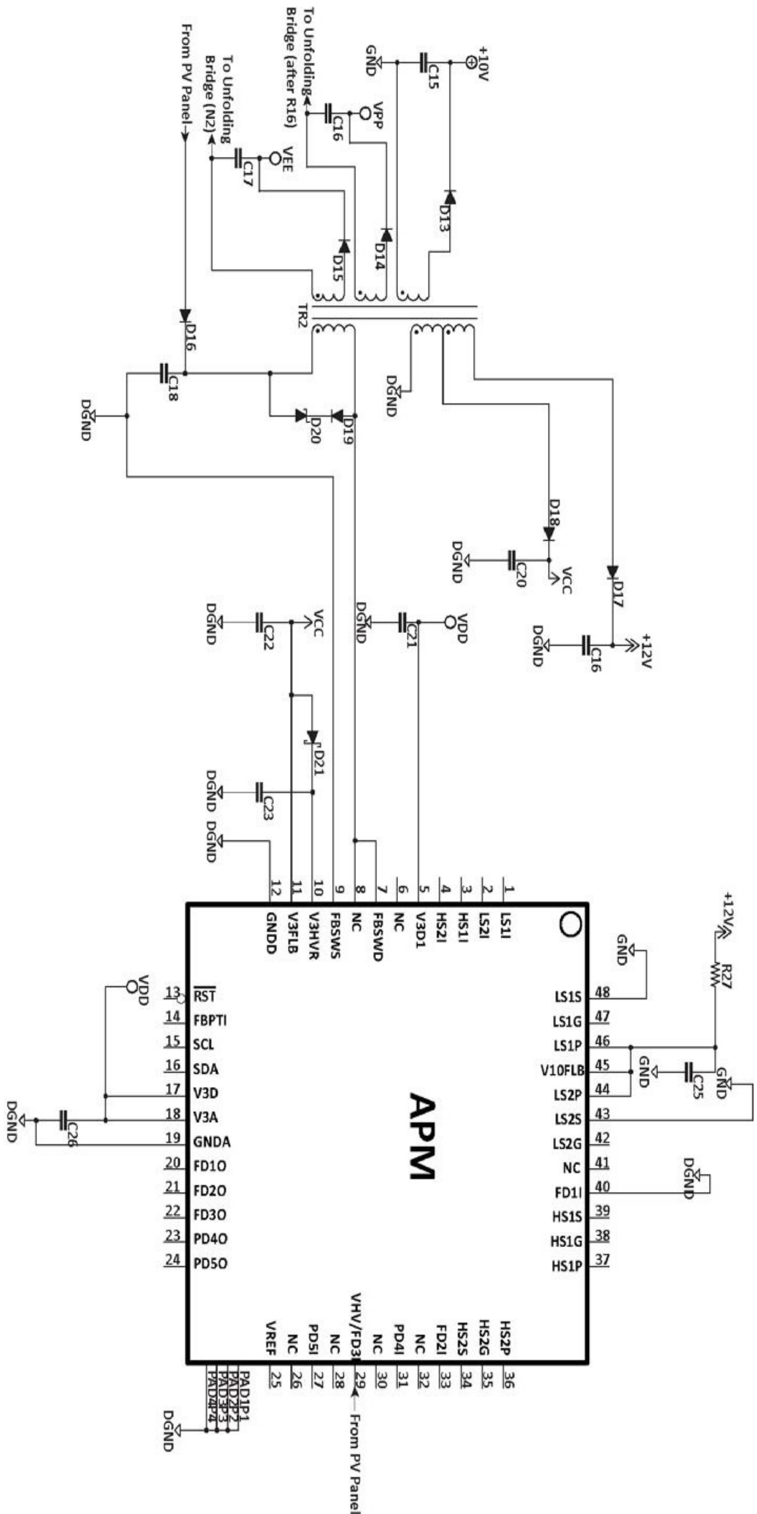


Figure 35 - MI-P300A APM coupling and flyback circuitries.

SA1002 (APM) schematic checklist

The SA1002 (APM) is intended to work in a noisy environment, therefore to ensure reliable operation it must be protected from the noise. The designer should follow the best practice for electromagnetic compatibility and the recommendations listed in this section must be followed. Specifically, decoupling capacitors should be placed very close to the power pins, and pins not used in the design to be grounded.

VHV/FD3I (pin 29) connection

VHV pin is an input to high voltage (HV) regulator and it is the primary voltage supplied of APM. Once VHV is above 6 V, the HV linear regulator generates a 2.8 V start-up voltage on pin V3HVR. This supply is used to start the flyback controller which starts regulating, and its output voltage, V3FLB, becomes approximately 3.3 V. No decoupling capacitor is required for VHV pin.

V3HVR (pin 10) connection

V3HVR pin is the output of the HV regulator. It requires at list 100 nF decupling capacitor between it and the ground.

V3D1 (pin 5) connection

Pin V3D1 is an input for 3 V supply for driver control and interlock logic. It requires a 100 nF decouplinc capacitor between it and the ground.

V3FLB (pin 5) connection

V3FLB is a Flyback feedback input. It is also a supply voltage to the internal 3 V linear regulators. External decoupling capacitor required. Recemented 100 nF near to APM and 22 µF parallel to it.

V3D (pin 17) and VPA (pin 18) regulators connections

V3D is the output of the 3 V digital linear regulator. V3A is the output of the 3 V analog linear regulator. The two regulators require external decoupling required (4.7 µF min). In some application these two outputs are connected together and a capacitor is used as it is shown in Figure 35.

Unused pins

NC pins are used for high voltage pin gap. They should be leaved unconnected. While the other unused analog pins should be grounded.

Layout Example

Figure 36 shows a layout example with SA1002 (APM) in Solantro ACBI.

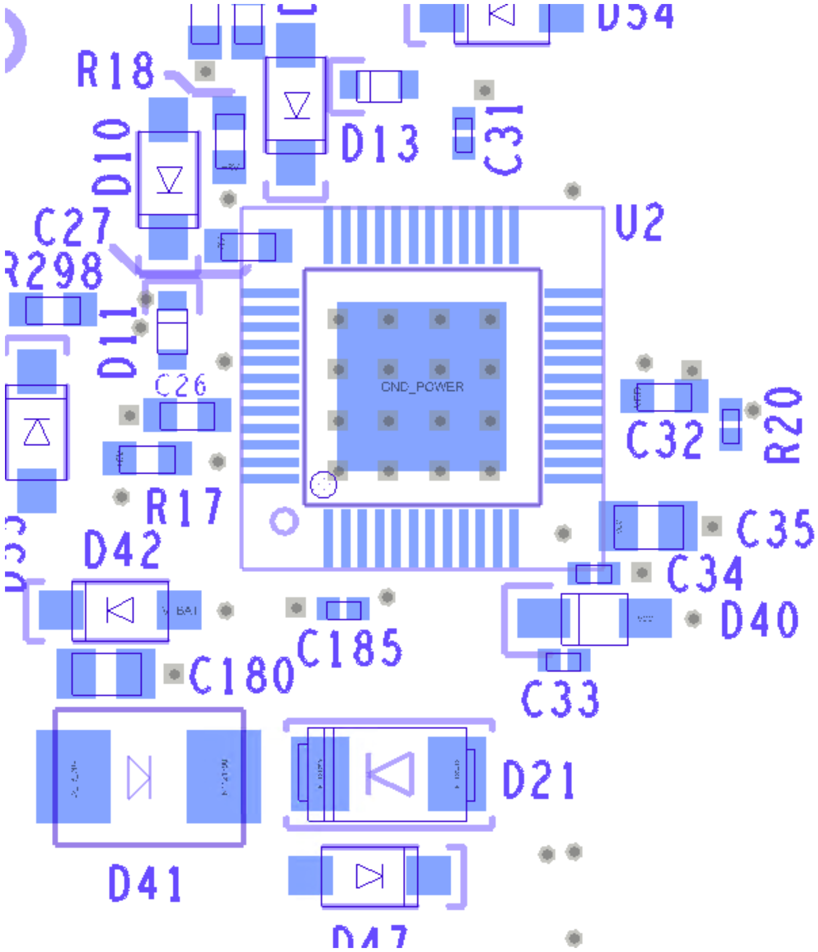


Figure 36 – ACBI APM layout example.

Documentation Support

DPD1001 - Solantro SA1002 (APM) Analog Power Manager Application Note

SA40x1 Packaging

The SA1002 (APM) is packaged in a 48 TQFP, 7x7x1mm package, as seen in Figure 37.

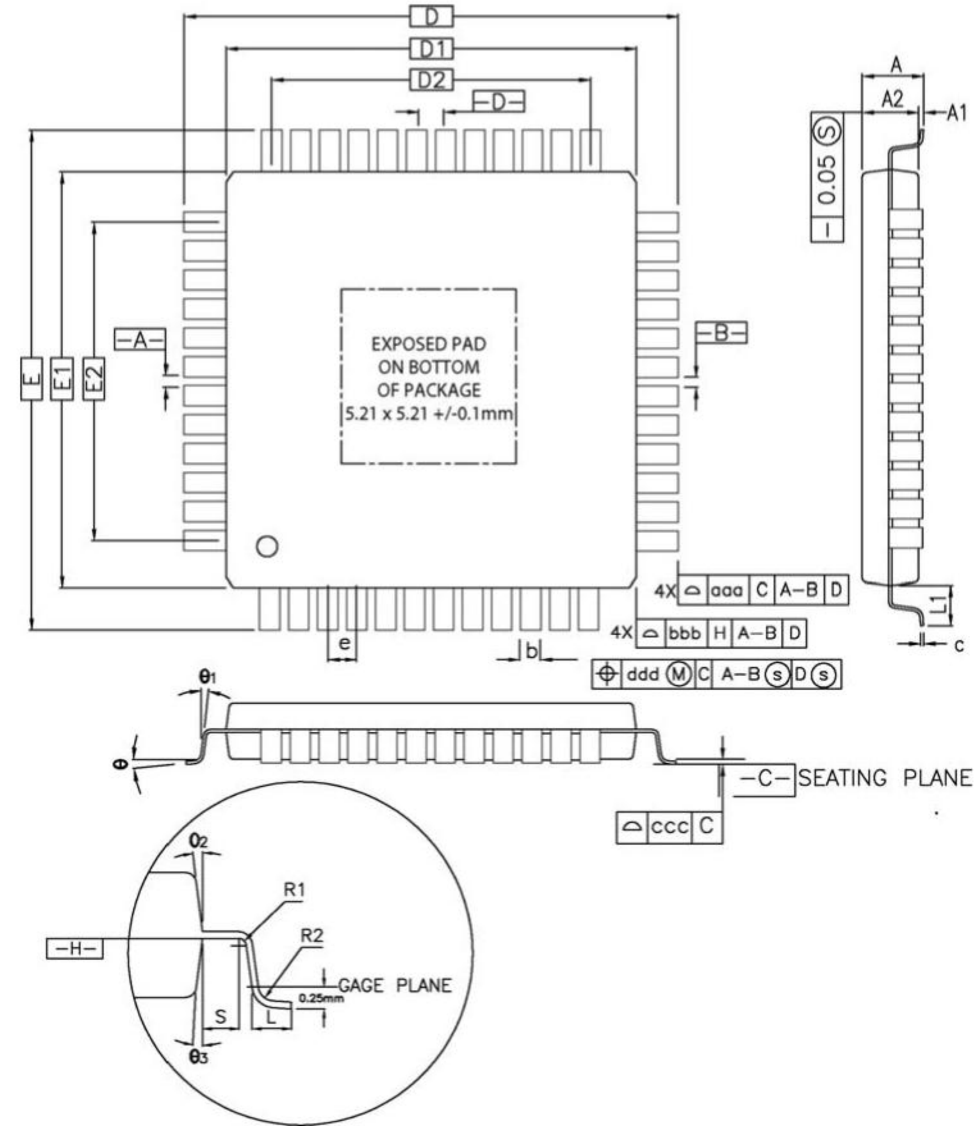


Figure 37 - SA1002 (APM) 48 TQFP packaging.

Table 18lists the packaging dimensions for the SA1002 (APM).

Table 18 - SA1002 (APM) 48 TQFP package dimensions

Symbol	Millimeters			Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	NA	NA	1.20	NA	NA	0.047
A1	0.05	NA	0.15	0.002	NA	0.006
A2	0.95	1.00	1.05	0.037	0.039	0.041
D	9.00 BSC.			0.354 BSC.		
D1	7.00 BSC.			0.276 BSC.		
E	9.00 BSC.			0.354 BSC.		
E1	7.00 BSC.			0.276 BSC.		
R2	0.08	NA	0.20	0.003	NA	0.008
R1	0.08	NA	NA	0.003	NA	NA
0	0°	3.5 °	7 °	0°	3.5 °	7 °
0_1	0°	NA	NA	0°	NA	NA
0_2	11°	12°	13°	11°	12°	13°
0_3	11°	12°	13°	11°	12°	13°
c	0.09	NA	0.20	0.20	NA	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
S	0.20	NA	NA	0.008	NA	NA
b	0.17	0.20	0.27	0.007	0.008	0.011
e	0.50 BSC.			0.016 BSC.		
D2	5.50			0.217		
E2	5.50			0.217		
Tolerances of form and position						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.08			0.003		

Revision History

Revision	Description	Date
1	Preliminary Document	June., 2016
2	Revision	April 2019

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