60V P-Channel Enhancement Mode MOSFET

■ DESCRIPTION

The SM409 is P channel enhancement mode power effect transitor which is produced using high cell density advanced trench technology.

The high density process is especially able to minize on-state resistance.These devices are. especially suited for low voltage application power management DC-DC converters.

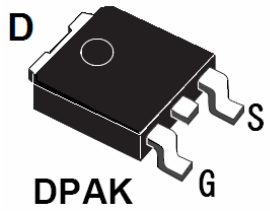
■ FEATURE

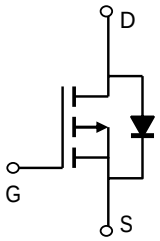
- ***-60V/-26 A, $R_{DS(ON)}$=30 mΩ(typ.)@VGS= -10V***
- ***-60V/-20A, $R_{DS(ON)}$=40 mΩ(typ.)@VGS= -4.5V***
- Super high design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and Maximum DC current capability
- Full RoHS compliance
- TO252 package design
- 100% UIS Tested
- 100% Rg tested

■ APPLICATIONS

- Power Management
- DC/DC Converter
- Load Switch

■ PIN CONFIGURATION





■ *ORDERING INFORMATION*

Part Number	Package Code	Package	Shipping
SM409T9RL	409	TO-252	2500EA / T&R

■ *ABSOLUTE MAXIMUM RATINGS* (T_A = 25℃ *Unless otherwise noted*)

Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	-60	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current [G]	T_C=25°C	I_D	-26	A
	T_C=100°C		-18	
Pulsed Drain Current [C]		I_{DM}	-60	
Avalanche Current [C]		I_{AR}	-26	A
Repetitive avalanche energy L=0.1mH [C]		E_{AR}	33.8	mJ
Power Dissipation [B]	T_C=25°C	P_D	60	W
	T_C=100°C		30	
Power Dissipation [A]	T_A=25°C	P_{DSM}	2.5	W
	T_A=70°C		1.6	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 175	°C

Thermal Characteristics					
Parameter		**Symbol**	**Typ**	**Max**	**Units**
Maximum Junction-to-Ambient [A]	t ≤ 10s	$R_{\theta JA}$	16.7	25	°C/W
Maximum Junction-to-Ambient [A]	Steady-State		40	50	°C/W
Maximum Junction-to-Case [C]	Steady-State	$R_{\theta JC}$	1.9	2.5	°C/W

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress rating only and functional device operation is not implied

■ *ELECTRICAL CHARACTERISTICS(T_A=25℃ Unless otherwise noted)*

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Static Parameters						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D= -250uA	-60			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D= -250uA	-1.0		-2.5	V
I_{GSS}	Gate Leakage Current	V_{DS}=0V, V_{GS}=±25V			±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=-48V, V_{GS}=0			-1	uA
		V_{DS}=-48V, V_{GS}=0 T_J=85℃			-5	
$R_{DS(ON)}$	Drain-Source On-Resistance	V_{GS}=-10V, I_D= -20 A		30	40	mΩ
		V_{GS}= -4.5V,I_D= -20 A		40	55	
Source-Drain Diode						
V_{SD}	Diode Forward Voltage	I_S= -1 A, V_{GS}=0V		0.7	1.3	V
Dynamic Parameters						
Q_g	Total Gate Charge	V_{DS}= -30V V_{GS}= -10V I_D=-20 A		53		nC
Q_{gs}	Gate-Source Charge			12		
Q_{gd}	Gate-Drain Charge			13		
C_{iss}	Input Capacitance	V_{DS}= -30V V_{GS}=0V f=1MHz		1886		pF
C_{oss}	Output Capacitance			540		
C_{rss}	Reverse Transfer Capacitance			240		
$T_{d(on)}$	Turn-On Time	V_{DS}= -30V R_L=1.50Ω V_{GEN}=-10V R_G=3.0Ω		19		nS
T_r				15		
$T_{d(off)}$	Turn-Off Time			52		
T_f				17		

Note: 1. Pulse test: pulse width<=300uS, duty cycle<=2%

2.Static parameters are based on package level with recommended wire bonding

■ *TYPICAL CHARACTERISTICS (25℃ Unless Note)*

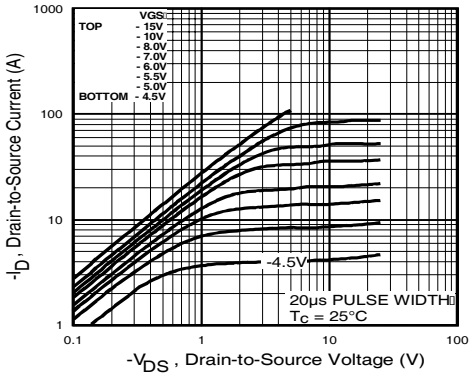


Fig 1. Typical Output Characteristics

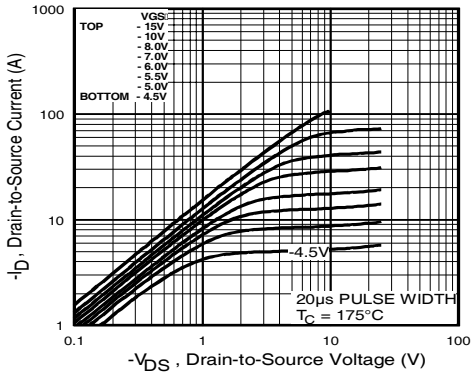


Fig 2. Typical Output Characteristics

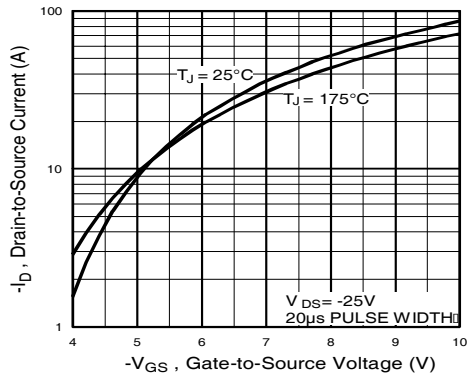


Fig 3. Typical Transfer Characteristics

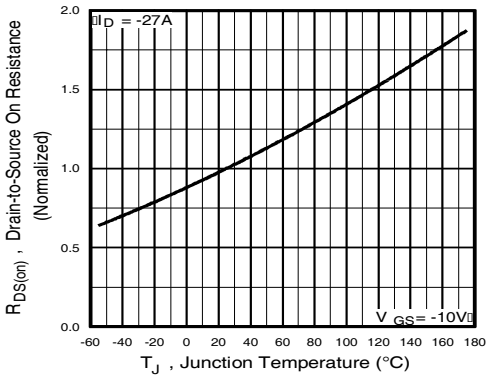


Fig 4. Normalized On-Resistance Vs. Temperature

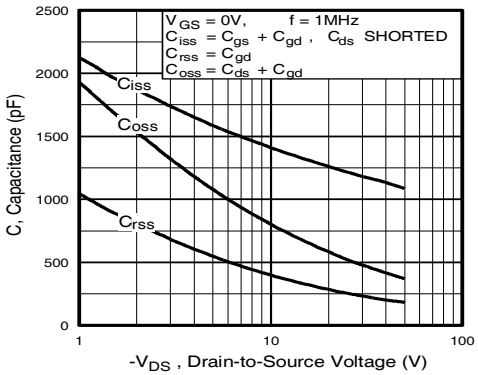


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

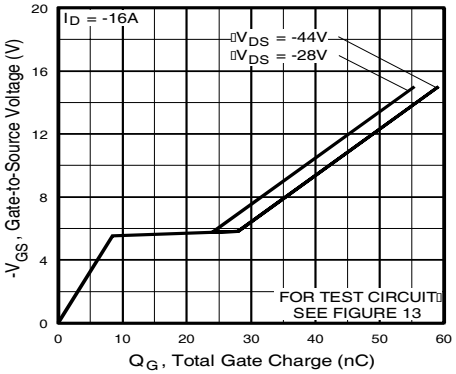


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

■ *TYPICAL CHARACTERISTICS (continuous)*

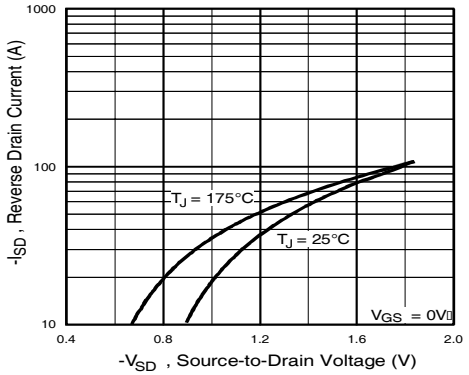


Fig 7. Typical Source-Drain Diode Forward Voltage

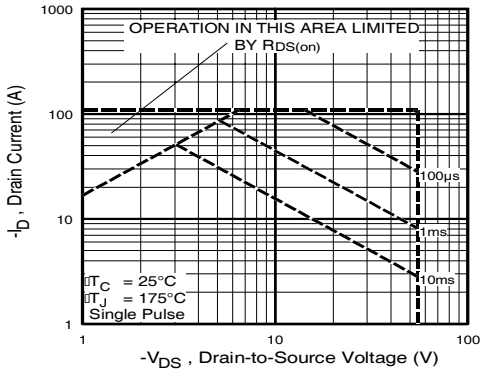


Fig 8. Maximum Safe Operating Area

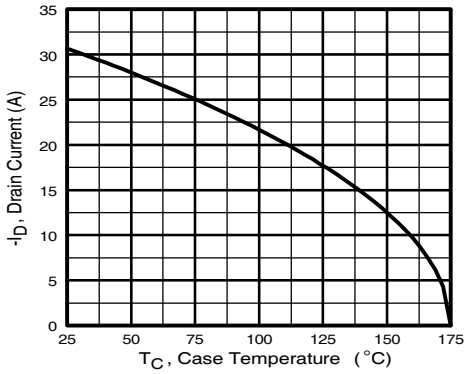


Fig 9. Maximum Drain Current Vs. Case Temperature

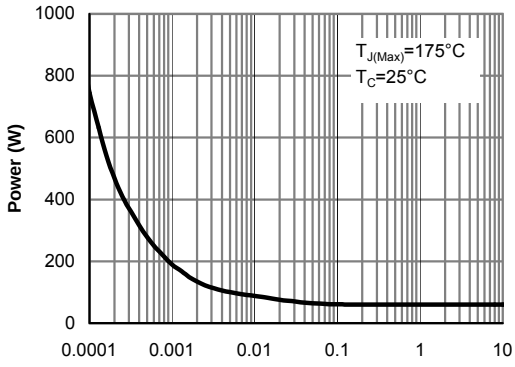
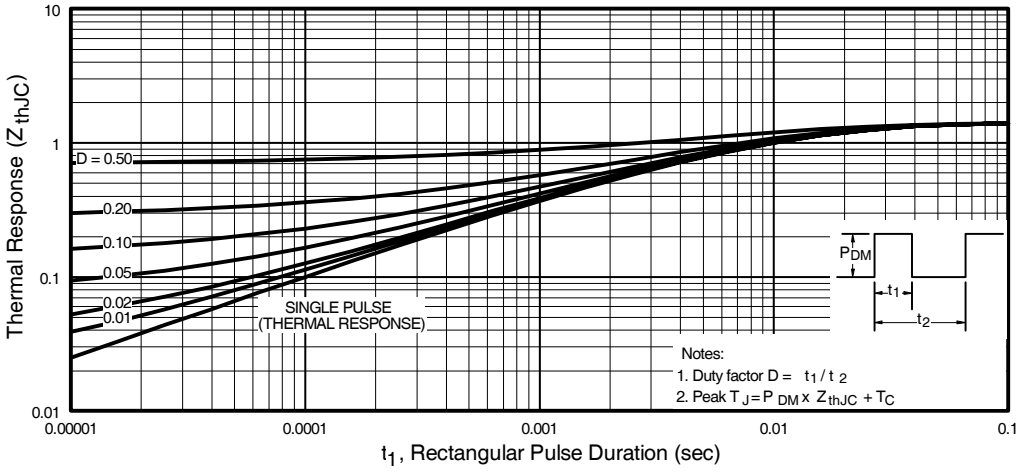
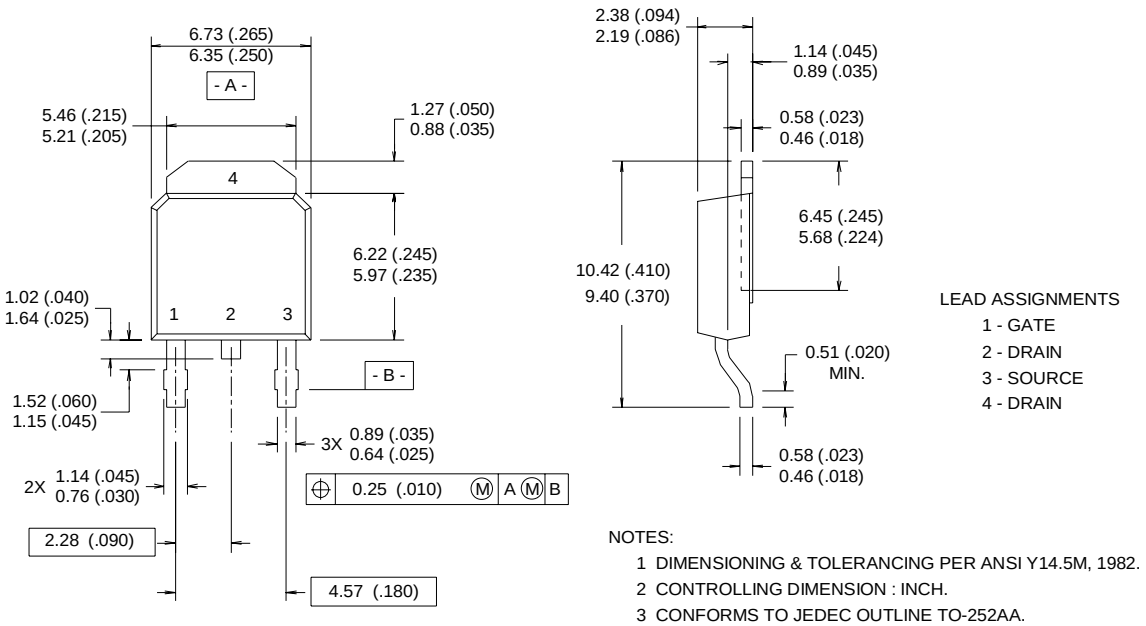


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)



■ TO-252 Outline Package Dimension

Dimensions are shown in millimeters (inches)



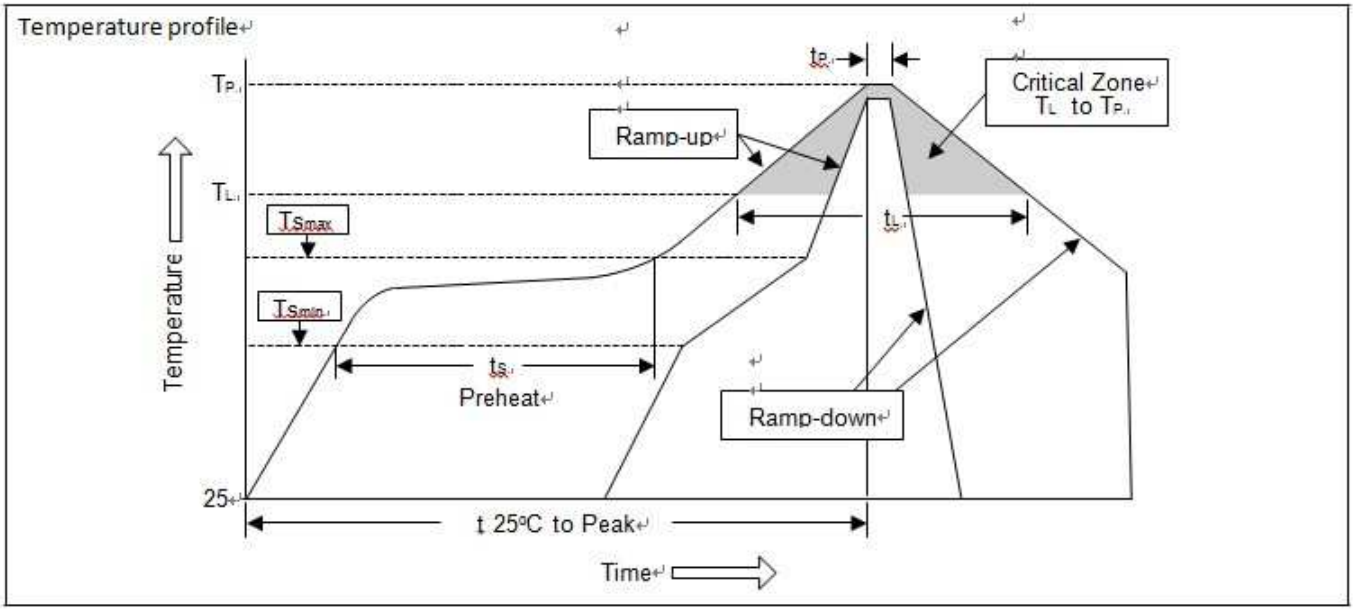
LEAD ASSIGNMENTS
1 - GATE
2 - DRAIN
3 - SOURCE
4 - DRAIN

NOTES:
1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION : INCH.
3 CONFORMS TO JEDEC OUTLINE TO-252AA.
4 DIMENSIONS SHOWN ARE BEFORE SOLDER DIP, SOLDER DIP MAX. +0.16 (.006).

■ *SOLDERING METHODS FOR UNIVERCHIP*

Storage environment Temperature=10℃~35℃ Humidity=65%±15%

Reflow soldering of surface mount device



Profile Feature	Sn-Pb Eutectic Assembly	Pb free Assembly
Average ramp-up rate (T_L to T_P)	<3℃/sec	<3℃/sec
Preheat -Temperature Min (Ts_{min}) -Temperature Max (Ts_{max}) -Time (min to max) (ts)	 100℃ 150℃ 60~120 sec	 150℃ 200℃ 60~180 sec
Tsmax to T_L -Ramp-up Rate	<3℃/sec	<3℃/sec
Time maintained above -Temperature (T_L) -Time (t_L)	 183℃ 60~150 sec	 217℃ 60~150 sec
Peak Temperature (T_P)	240℃+0/-5℃	260℃+0/-5℃
Time within 5℃ of actual Peak Temperature (t_P)	10~30 sec	20~40 sec
Ramp-down Rate	<6℃/sec	<6℃/sec
Time 25℃ to Peak Temperature	<6 minutes	<6 minutes

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