



ST3401SRG 
P Channel Enhancement Mode MOSFET

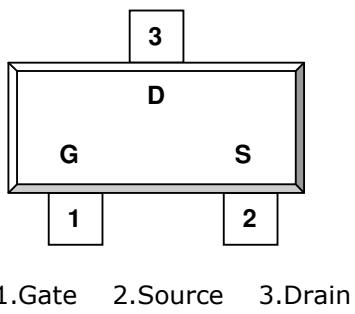
-4.0A

DESCRIPTION

ST3401RSG is the P-Channel logic enhancement mode power field effect transistor which is produced using high cell density DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management, other battery powered circuits, and low in-line power loss are required. The product is in a very small outline surface mount package.

PIN CONFIGURATION

SOT-23

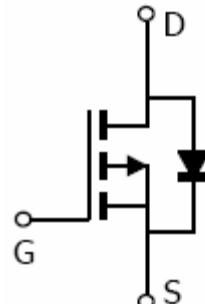
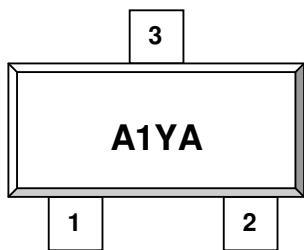


FEATURE

- -30V/-4.0A, $R_{DS(ON)} = 55m\Omega$ (Typ.)
@ $V_{GS} = -10V$
- -30V/-3.2A, $R_{DS(ON)} = 62m\Omega$
@ $V_{GS} = -4.5V$
- -30V/-1.2A, $R_{DS(ON)} = 90m\Omega$
@ $V_{GS} = -2.5V$
- Super high density cell design for
Extremely low $R_{DS(ON)}$
- Exceptional on-resistance and
maximum DC current capability
- SOT-23 package design

PART MARKING

SOT-23





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ABSOLUTE MAXIMUM RATINGS (Ta = 25°C Unless otherwise noted)

Parameter	Symbol	Typical	Unit
Drain-Source Voltage	V _{DSS}	-30	V
Gate-Source Voltage	V _{GSS}	±12	V
Continuous Drain Current(T _J =150°C)	I _D	-4.0 -3.2	A
Pulsed Drain Current	I _{DM}	-15	A
Continuous Source Current (Diode Conduction)	I _S	-1.0	A
Power Dissipation	P _D	1.20 0.8	W
Operation Junction Temperature	T _J	150	°C
Storage Temperature Range	T _{STG}	-55/150	°C
Thermal Resistance-Junction to Ambient	R _{θJA}	120	°C/W

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ELECTRICAL CHARACTERISTICS (Ta = 25°C Unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} =0V, I _D =-250uA	-30			V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =-250uA	-0.4		-1.0	V
Gate Leakage Current	I _{GSS}	V _{DS} =0V, V _{GS} =±12V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =-24V, V _{GS} =0V			-1	uA
		V _{DS} =-24V, V _{GS} =0V T _J =55°C			-10	
Drain-source On-Resistance	R _{DS(on)}	V _{GS} =-10V, I _D =-4.0A V _{GS} =-4.5V, I _D =-3.2A V _{GS} =-2.5V, I _D =-1.2A	55 62 90	61 70 98		mΩ
Forward Transconductance	g _f s	V _{DS} =-5V, I _D =-4.0V		10		S
Diode Forward Voltage	V _{SD}	I _S =-1.0A, V _{GS} =0V			-1.2	V
Dynamic						
Total Gate Charge	Q _g	V _{DS} =-15V V _{GS} =-10V I _D =-4.0A		14	21	nC
Gate-Source Charge	Q _{gs}			1.9		
Gate-Drain Charge	Q _{gd}			3.7		
Input Capacitance	C _{iss}	V _{DS} =-15V V _{GS} =0V F=1MHz		540		pF
Output Capacitance	C _{oss}			131		
Reverse Transfer Capacitance	C _{rss}			105		
Turn-On Time	t _{d(on)} tr	V _{DS} =-15V V _{GS} =-15V I _D =-1A R _L =6Ω R _G =-10Ω		10	15	nS
Turn-Off Time	t _{d(off)} tf			15	25	
				31	50	
				20	30	



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TYPICAL CHARACTERISTICS (25°C Unless noted)

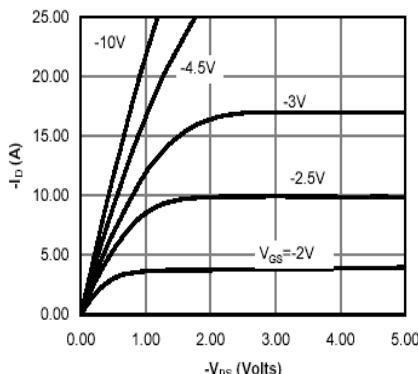


Fig 1: On-Region Characteristics

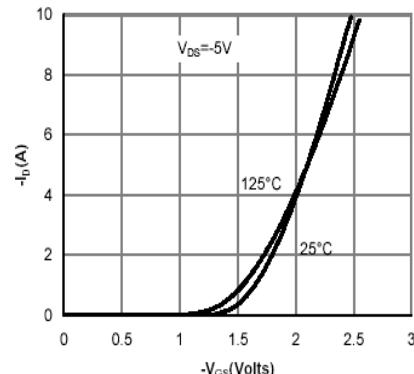


Figure 2: Transfer Characteristics

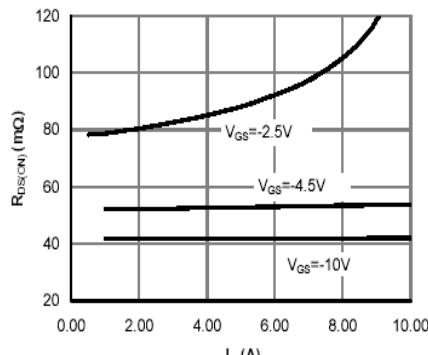


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

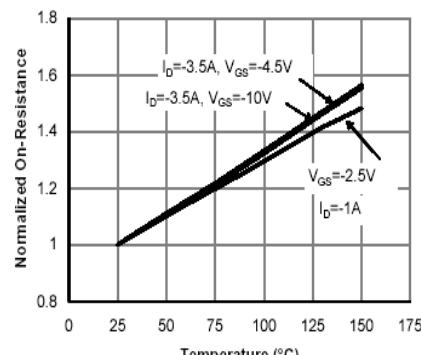


Figure 4: On-Resistance vs. Junction Temperature

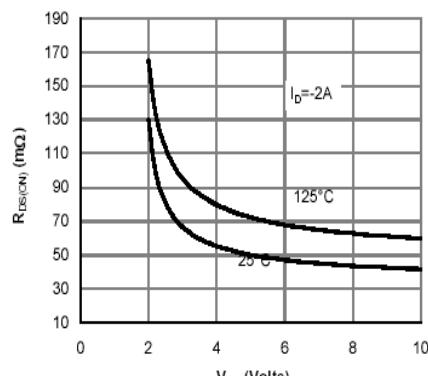


Figure 5: On-Resistance vs. Gate-Source Voltage

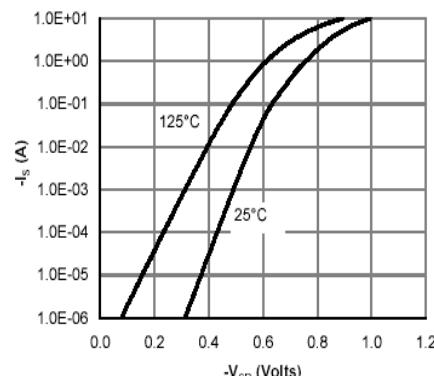


Figure 6: Body-Diode Characteristics

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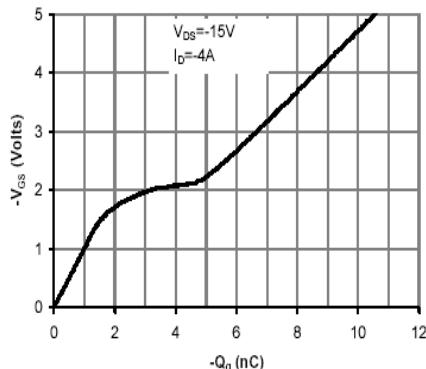


Figure 7: Gate-Charge Characteristics

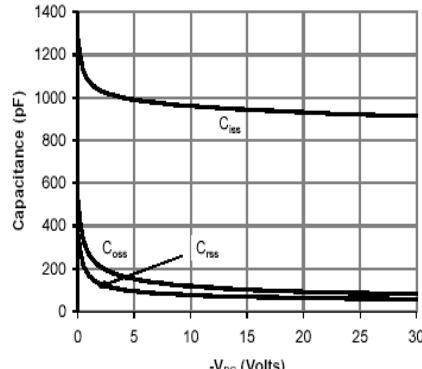


Figure 8: Capacitance Characteristics

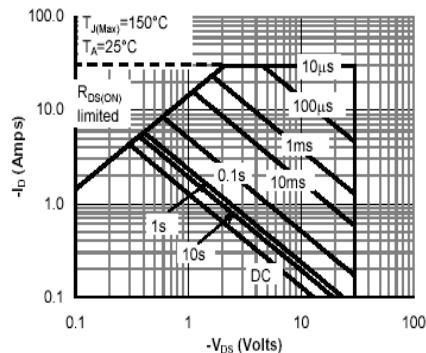


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

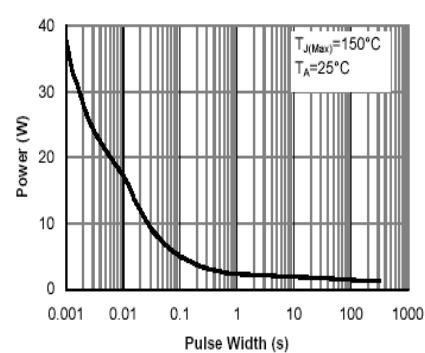
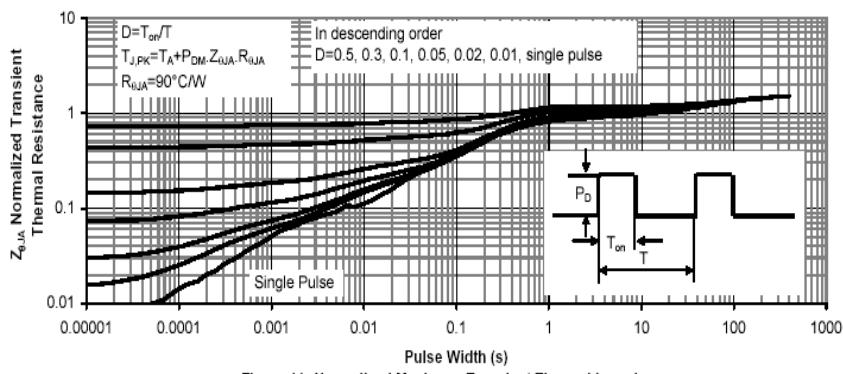


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)



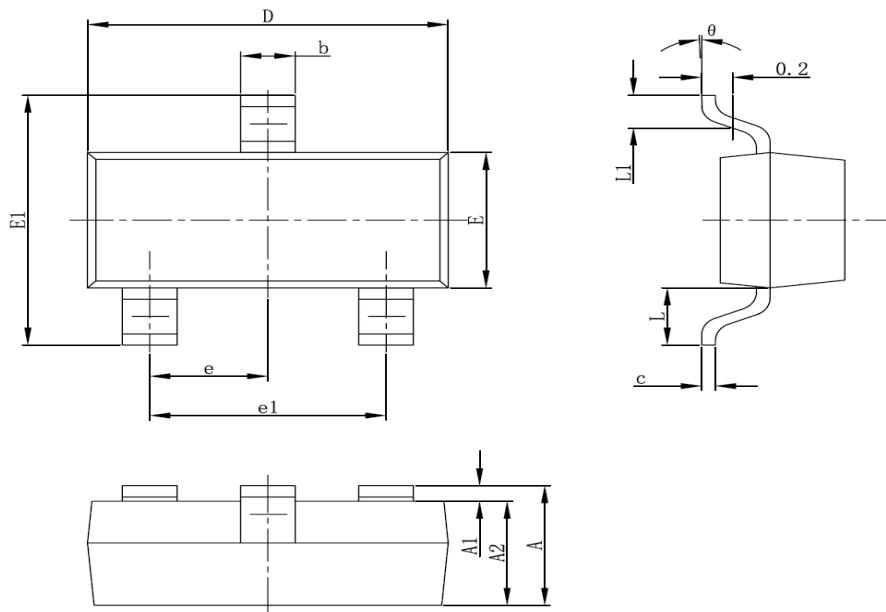
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SOT-23 PACKAGE OUTLINE



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.900	1.100	0.035	0.043
A1	0.000	0.100	0.000	0.004
A2	0.900	1.000	0.035	0.039
b	0.300	0.500	0.012	0.020
c	0.080	0.150	0.003	0.006
D	2.800	3.000	0.110	0.118
E	1.200	1.400	0.047	0.055
E1	2.250	2.550	0.089	0.100
e	0.950TYP		0.037TYP	
e1	1.800	2.000	0.071	0.079
L	0.550REF		0.022REF	
L1	0.300	0.500	0.012	0.020
θ	0°	8°	0°	8°

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