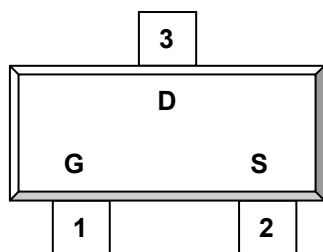


DESCRIPTION

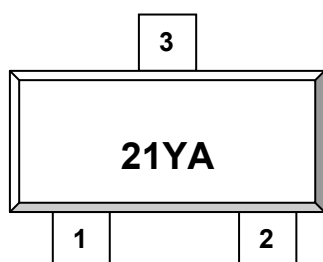
ST3421SRG is the P-Channel logic enhancement mode power field effect transistor which is produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management, other battery powered circuits, and low in-line power loss are required. The product is in a very small outline surface mount package.

**PIN CONFIGURATION
SOT-23**


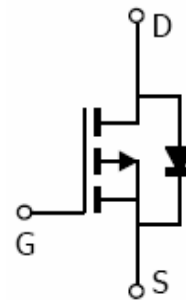
1.Gate 2.Source 3.Drain

FEATURE

- -60V/-5.0A, $R_{DS(ON)} = 150\text{m-ohm}$ (Typ.) @VGS = -10V
- -60V/-2.5A, $R_{DS(ON)} = 185\text{m-ohm}$ @VGS = -4.5V
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- SOT-23 package design

**PART MARKING
SOT-23**


Y: Year Code A: Process Code





ST3421SRG 

P Channel Enhancement Mode MOSFET

-5.0A

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C Unless otherwise noted)

Parameter	Symbol	Typical	Unit
Drain-Source Voltage	V _{DSS}	-60	V
Gate-Source Voltage	V _{GSS}	±20	V
Continuous Drain Current (T _J =150°C)	I _D	T _A =25°C -5.0	A
		T _A =70°C -3.5	
Pulsed Drain Current	I _{DM}	-12	A
Continuous Source Current (Diode Conduction)	I _S	-1.25	A
Power Dissipation	P _D	T _A =25°C 1.25	W
		T _A =70°C 0.8	
Operation Junction Temperature	T _J	150	°C
Storage Temperature Range	T _{STG}	-55/150	°C
Thermal Resistance-Junction to Ambient	R _{θJA}	100	°C/W



ST3421SRG 

P Channel Enhancement Mode MOSFET

-5.0A

ELECTRICAL CHARACTERISTICS (Ta = 25°C Unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=-10\mu A$	-60			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-250\mu A$	-1.0		-3.0	V
Gate Leakage Current	I_{GSS}	$V_{DS}=0V, V_{GS}=\pm 20V$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=-48V, V_{GS}=0V$			-1	uA
		$V_{DS}=-48V, V_{GS}=0V$ $T_J=55^\circ C$			-10	
Drain-source On-Resistance	$R_{DS(on)}$	$V_{GS}=-10V, I_D=-5.0A$ $V_{GS}=-4.5V, I_D=-2.5A$		0.150 0.185	0.160 0.200	Ω
Forward Transconductance	g_{fs}	$V_{DS}=-10V, I_D=-1.7V$		2.4		S
Diode Forward Voltage	V_{SD}	$I_S=-1.25A, V_{GS}=0V$		-0.8	-1.2	V
Dynamic						
Total Gate Charge	Q_g	$V_{DS}=-30V$ $V_{GS}=-10V$ $I_D=-2A$		16		nC
Gate-Source Charge	Q_{gs}			8		
Gate-Drain Charge	Q_{gd}			3.0		
Input Capacitance	C_{iss}	$V_{DS}=-30V$ $V_{GS}=0V$ $F=1MHz$			1200	pF
Output Capacitance	C_{oss}			115		
Reverse Transfer Capacitance	C_{rss}			7		
Turn-On Time	$t_{d(on)}$ t_r	$V_{DD}=-10V$ $R_L=15\Omega$ $I_D=-1.0A$ $V_{GEN}=-3V$ $R_G=2.5\Omega$		9		nS
				109		
Turn-Off Time	$t_{d(off)}$ t_f			25		
				11		

TYPICAL CHARACTERISTICS (25°C Unless noted)

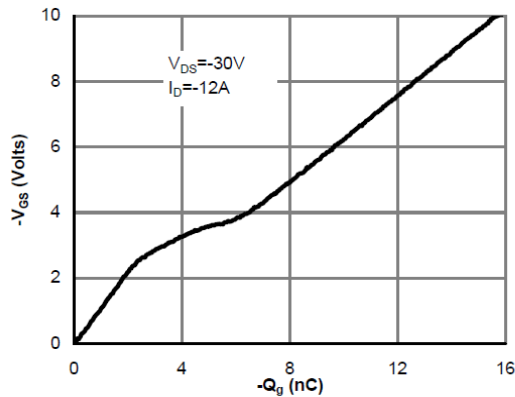


Figure 7: Gate-Charge Characteristics

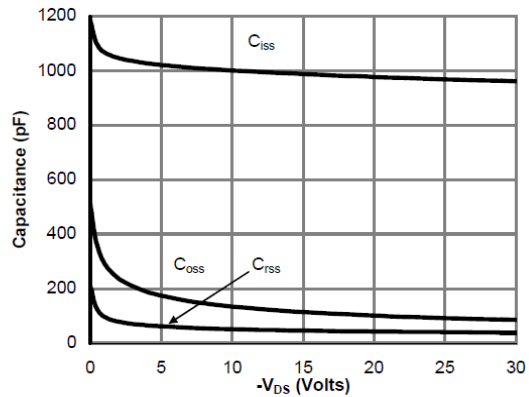


Figure 8: Capacitance Characteristics

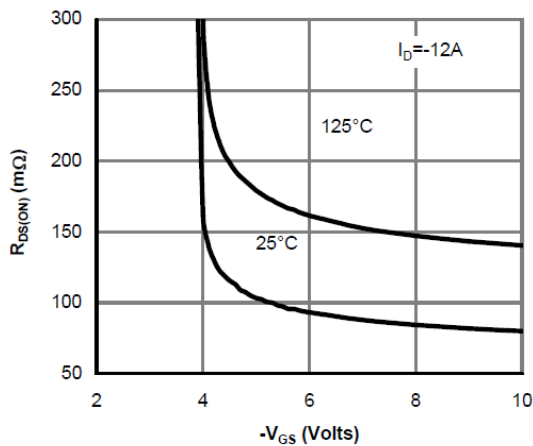


Figure 5: On-Resistance vs. Gate-Source Voltage

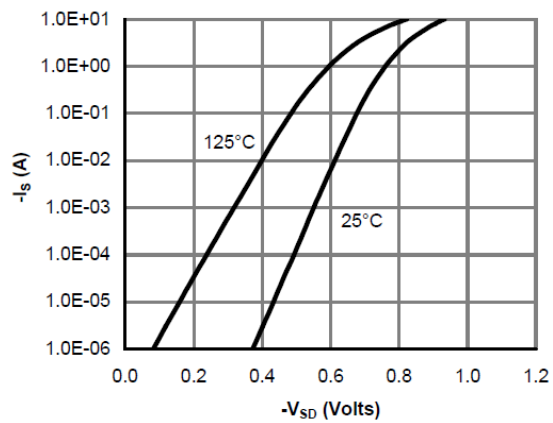


Figure 6: Body-Diode Characteristics

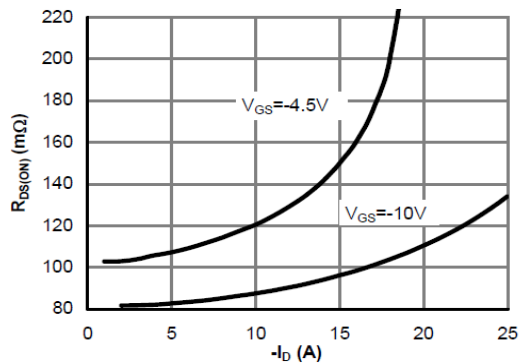


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

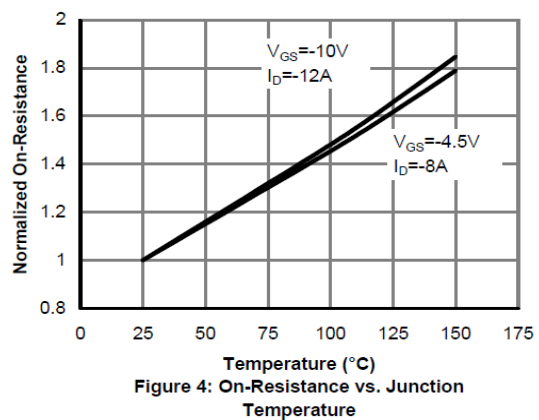


Figure 4: On-Resistance vs. Junction Temperature

TYPICAL CHARACTERISTICS (25°C Unless noted)

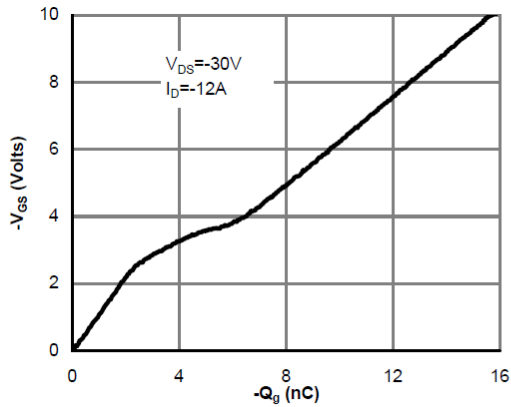


Figure 7: Gate-Charge Characteristics

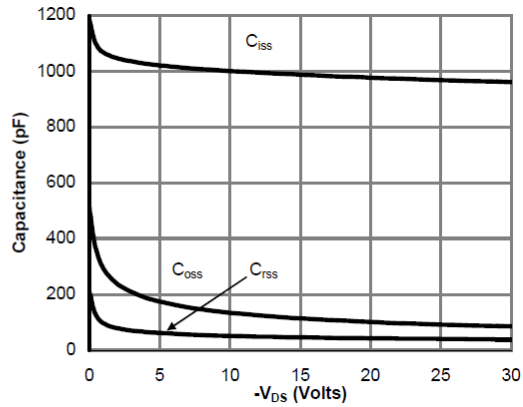


Figure 8: Capacitance Characteristics

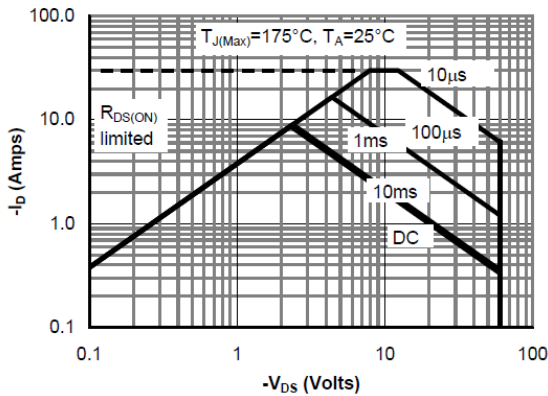


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

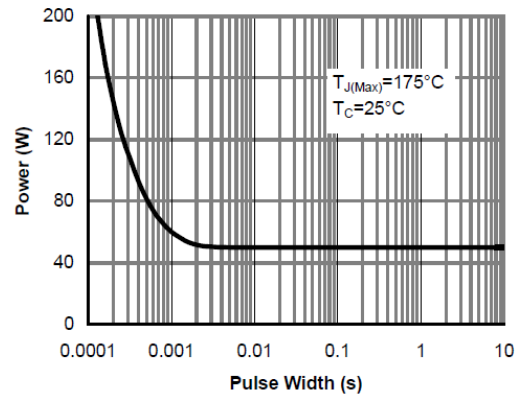


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

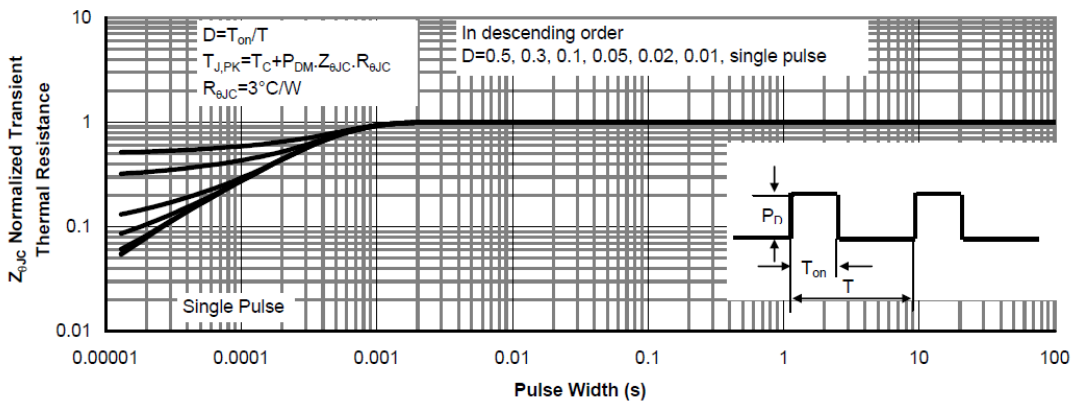
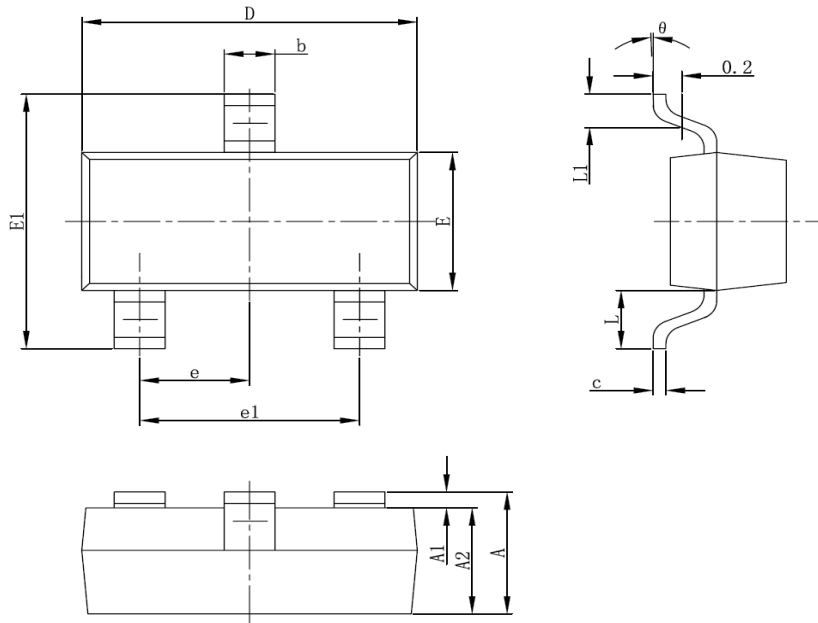


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

SOT-23 PACKAGE OUTLINE


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.900	1.100	0.035	0.043
A1	0.000	0.100	0.000	0.004
A2	0.900	1.000	0.035	0.039
b	0.300	0.500	0.012	0.020
c	0.080	0.150	0.003	0.006
D	2.800	3.000	0.110	0.118
E	1.200	1.400	0.047	0.055
E1	2.250	2.550	0.089	0.100
e	0.950TYP		0.037TYP	
e1	1.800	2.000	0.071	0.079
L	0.550REF		0.022REF	
L1	0.300	0.500	0.012	0.020
θ	0°	8°	0°	8°

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