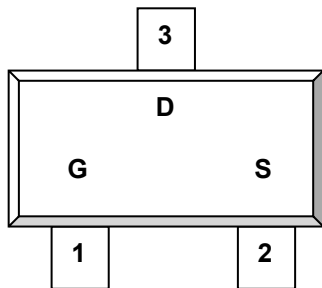


DESCRIPTION

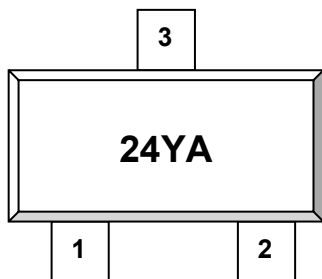
The ST3424 is the N-Channel logic enhancement mode power field effect transistor is produced using high cell density, DMOS trench technology. This high-density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high side switching.

**PIN CONFIGURATION
SOT-23**


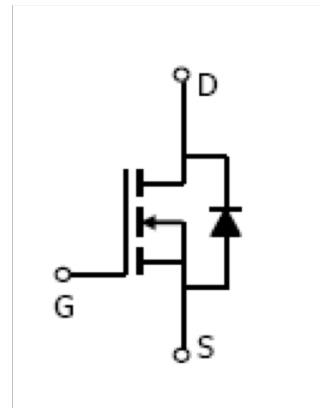
1.Gate 2.Source 3.Drain

FEATURE


- 60V/4.0A, $R_{DS(ON)} = 55m\Omega$
@ $V_{GS} = 10V$
- 60V/3.0A, $R_{DS(ON)} = 60m\Omega$
@ $V_{GS} = 4.5V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- SOT-23 package design

**PART MARKING
SOT-23**


Y: Year Code A: Process Code





ST3424 

N Channel Enhancement Mode MOSFET

4.0A

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C Unless otherwise noted)

Parameter	Symbol	Typical	Unit
Drain-Source Voltage	V _{DSS}	60	V
Gate-Source Voltage	V _{GSS}	±20	V
Continuous Drain Current (T _J =150°C)	I _D	T _A =25°C 4.0	A
		T _A =70°C 2.6	
Pulsed Drain Current	I _{DM}	26	A
Continuous Source Current (Diode Conduction)	I _S	1.8	A
Power Dissipation	P _D	T _A =25°C 1.8	W
		T _A =70°C 1.0	
Operation Junction Temperature	T _J	-55/150	°C
Storage Temperature Range	T _{STG}	-55/150	°C
Thermal Resistance-Junction to Ambient	R _{θJA}	75	°C/W



ELECTRICAL CHARACTERISTICS (Ta = 25°C Unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit	
Static							
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=250\mu A$	60			V	
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1		2.5	V	
Gate Leakage Current	I_{GSS}	$V_{DS}=0V, V_{GS}=\pm 20V$			± 100	nA	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=48V, V_{GS}=0V$			1	uA	
		$V_{DS}=48V, V_{GS}=0V$ $T_J=55^\circ C$			10		
Drain-source On-Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=4.0A$		50	55	mΩ	
		$V_{GS}=4.5V, I_D=3.0A$		56	62		
Forward Transconductance	g_{fs}	$V_{DS}=4.5V, I_D=5.8A$		11		S	
Diode Forward Voltage	V_{SD}	$I_S=1.7A, V_{GS}=0V$			1.1	V	
Dynamic							
Total Gate Charge	Q_g	$V_{DS}=15V$ $V_{GS}=10V$ $I_D=6.7A$		8		nC	
Gate-Source Charge	Q_{gs}			1.4			
Gate-Drain Charge	Q_{gd}			3.0			
Input Capacitance	C_{iss}	$V_{DS}=15V$ $V_{GS}=0V$ $F=1MHz$		400		pF	
Output Capacitance	C_{oss}			240			
Reverse Transfer Capacitance	C_{rss}			30			
Turn-On Time	$t_{d(on)tr}$	$V_{DD}=15V$ $R_L=15\Omega$ $I_D=1.0A$ $V_{GEN}=10V$ $R_G=6\Omega$		6.6	14	nS	
					10		20
Turn-Off Time	$t_{d(off)tf}$				19		39
					10		20

TYPICAL CHARACTERISTICS (25°C Unless noted)

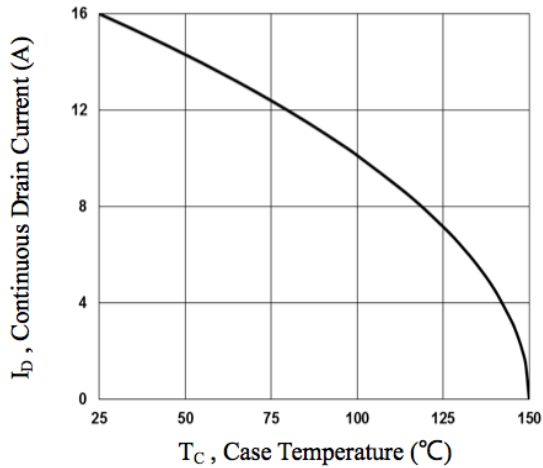


Fig.1 Continuous Drain Current vs. T_c

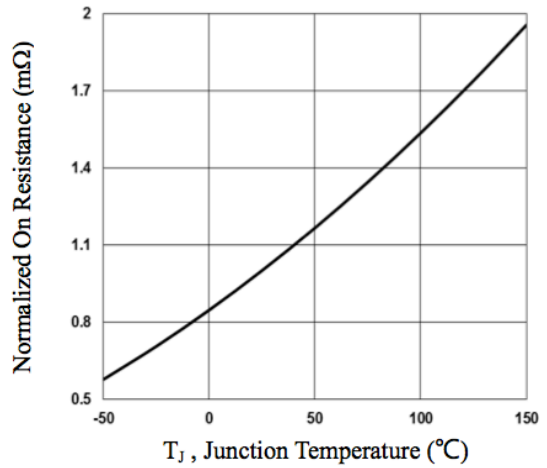


Fig.2 Normalized R_{DSon} vs. T_j

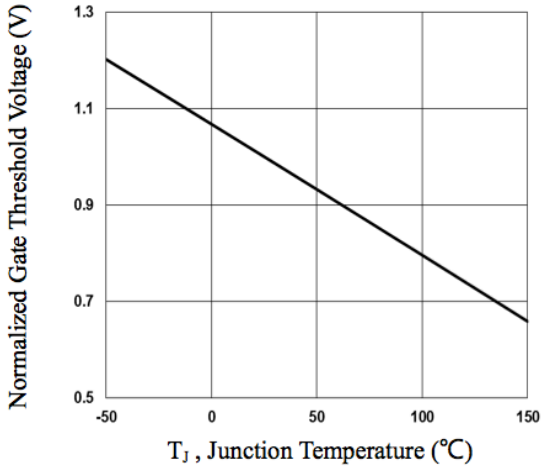


Fig.3 Normalized V_{th} vs. T_j

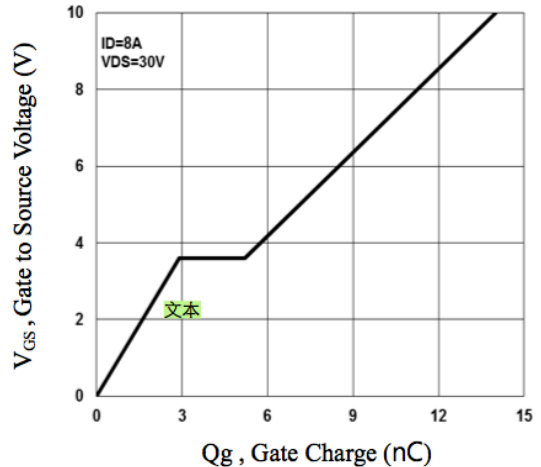


Fig.4 Gate Charge Waveform

TYPICAL CHARACTERISTICS (25°C Unless noted)

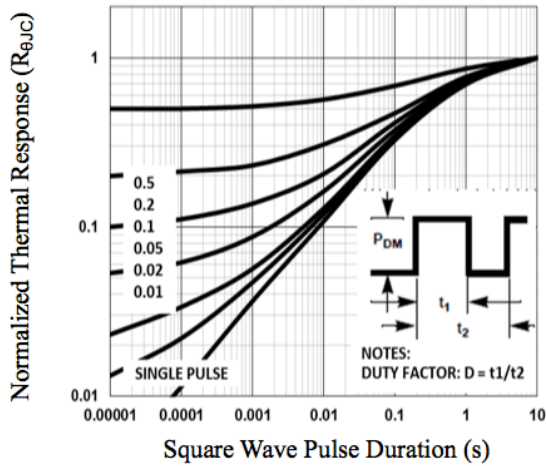


Fig.5 Normalized Transient Impedance

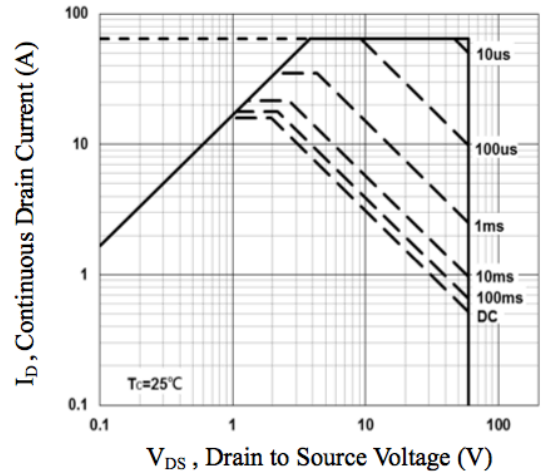


Fig.6 Maximum Safe Operation Area

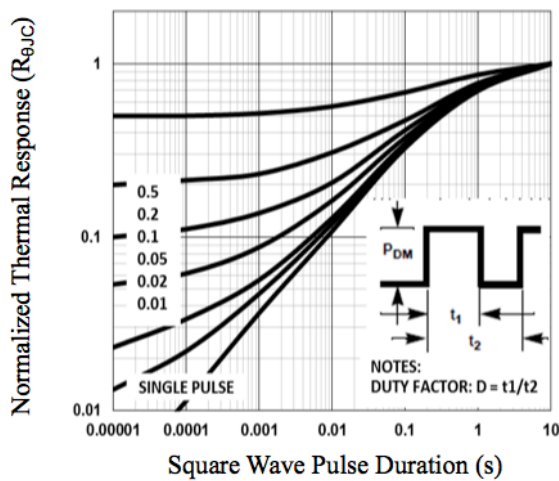


Fig.5 Normalized Transient Impedance

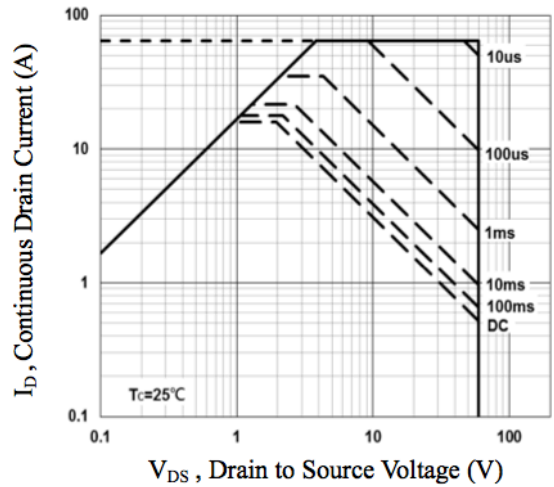
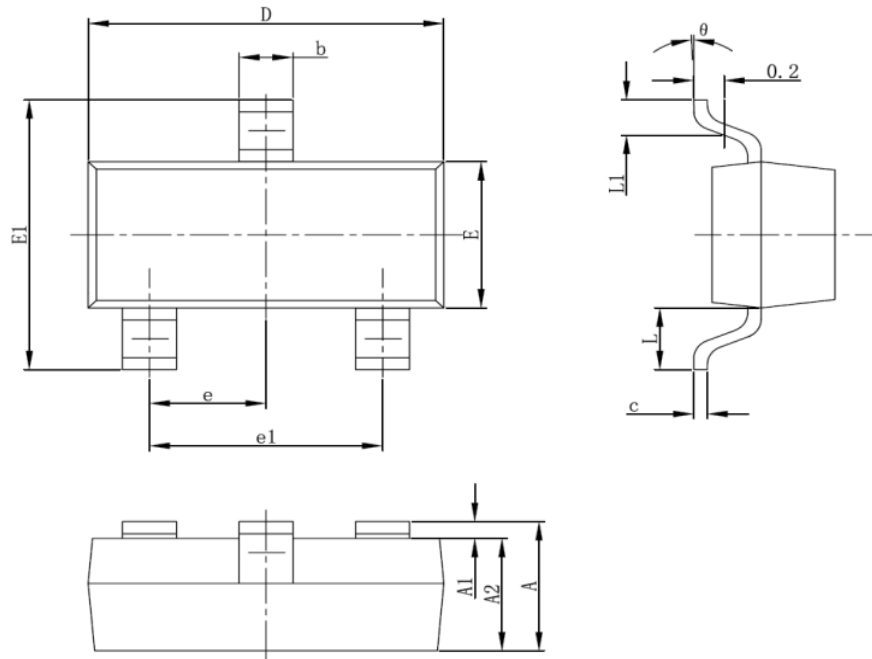


Fig.6 Maximum Safe Operation Area

SOT-23 PACKAGE OUTLINE


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.900	1.100	0.035	0.043
A1	0.000	0.100	0.000	0.004
A2	0.900	1.000	0.035	0.039
b	0.300	0.500	0.012	0.020
c	0.080	0.150	0.003	0.006
D	2.800	3.000	0.110	0.118
E	1.200	1.400	0.047	0.055
E1	2.250	2.550	0.089	0.100
e	0.950TYP		0.037TYP	
e1	1.800	2.000	0.071	0.079
L	0.550REF		0.022REF	
L1	0.300	0.500	0.012	0.020
theta	0°	8°	0°	8°

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