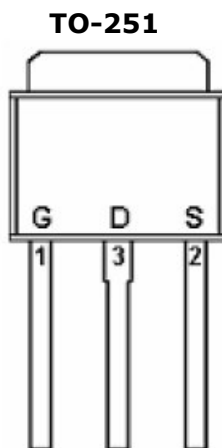
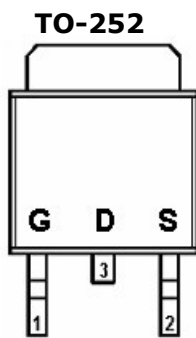


DESCRIPTION

STN36N10D is used trench technology to provide excellent RDS(on) and gate charge. Those devices are suitable for use as load switch or in PWM applications.

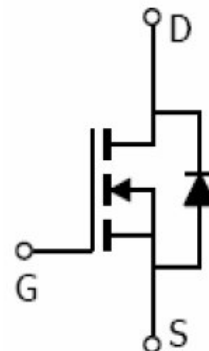
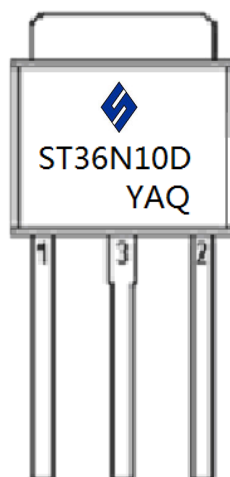
PIN CONFIGURATION (D-PAK)



FEATURE

- 100V/20.0A, $R_{DS(ON)} = 40m\Omega$ (Typ.) @ $V_{GS} = 10V$
- 100V/20.0A, $R_{DS(ON)} = 42m\Omega$ @ $V_{GS} = 4.5V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- TO-252, TO-251 package design

PART MARKING



Y: Year Code
A: Week Code
Q: Process Code

**ST36N10D**

N Channel Enhancement Mode MOSFET

36.0A

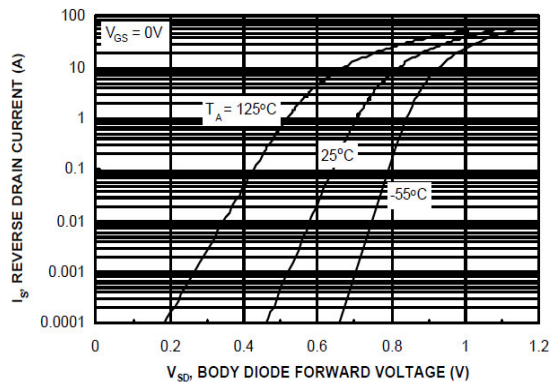
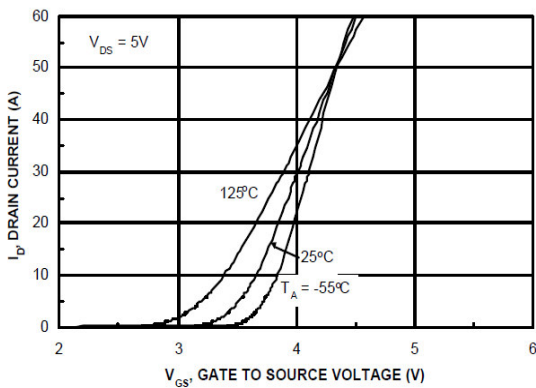
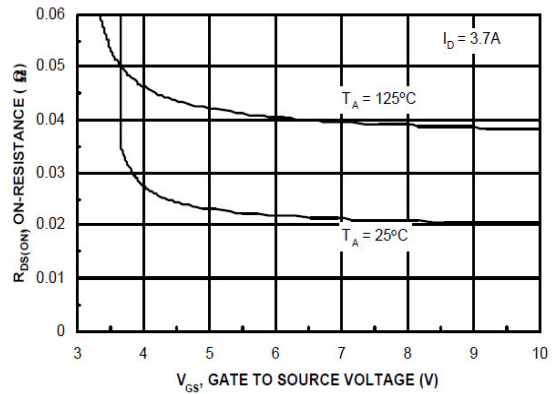
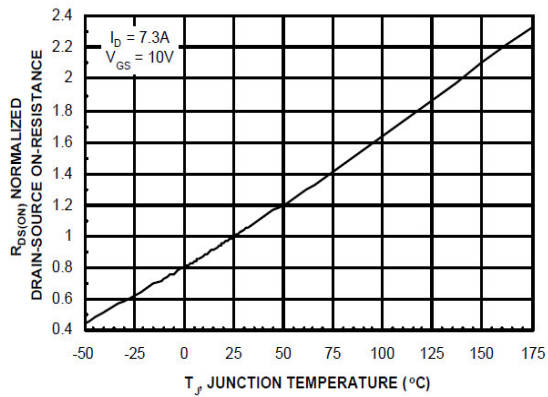
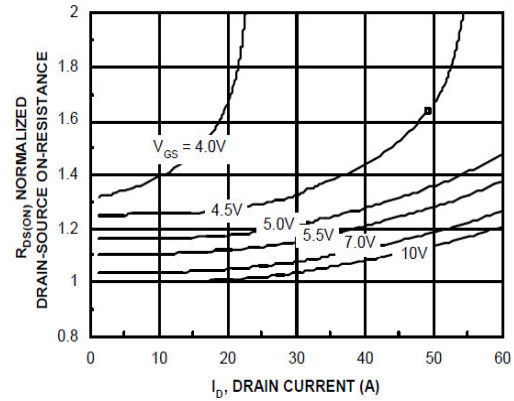
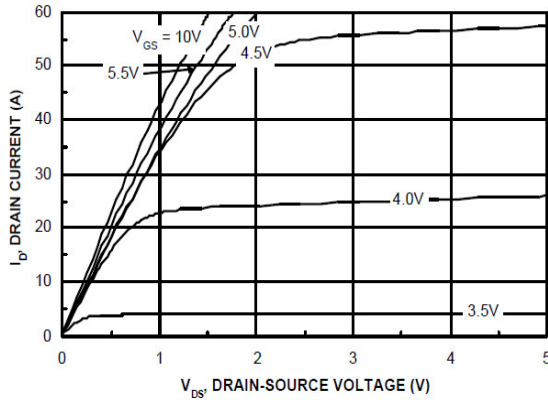
ABSOLUTE MAXIMUM RATINGS (Ta = 25°C Unless otherwise noted)

Parameter	Symbol	Typical	Unit
Drain-Source Voltage	VDSS	100	V
Gate-Source Voltage	VGSS	±20	V
Continuous Drain Current (TJ=150°C)	ID	36.0 14.0	A
Pulsed Drain Current	IDM	100	A
Continuous Source Current (Diode Conduction)	IS	2.7	A
Power Dissipation	PD	83 30	W
Operation Junction Temperature	TJ	175	°C
Storage Temperature Range	TSTG	-55/175	°C
Thermal Resistance-Junction to Ambient	RθJA	95	°C/W

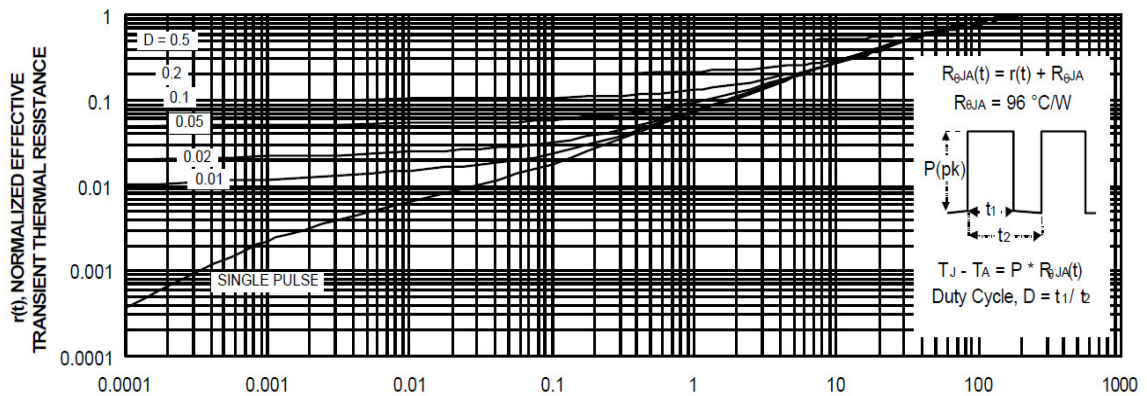
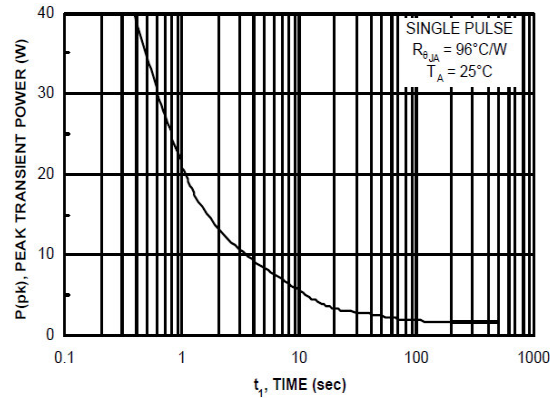
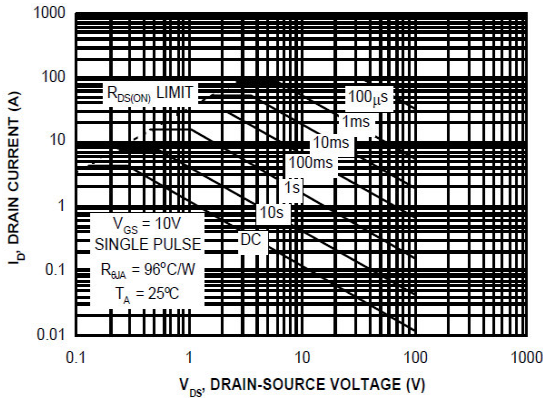
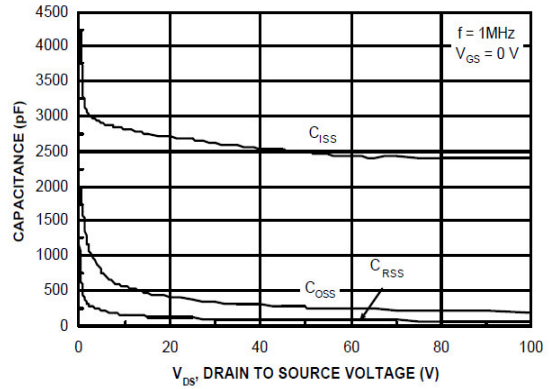
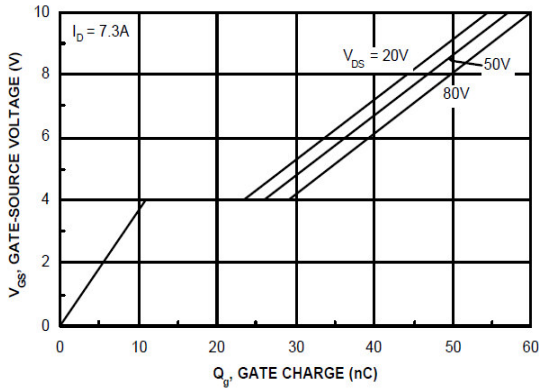
ELECTRICAL CHARACTERISTICS (Ta = 25°C Unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=250mA$	100			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1		3	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=80V, V_{GS}=0V$			10	nA
Gate leakage Current	I_{GSS}	$V_{DS}=0V, V_{GS}=20V$			100	uA
		$V_{DS}=0V, V_{GS}=-20V$			-100	
On-State Drain Current	$I_{D(on)}$	$V_{DS} \geq 5V, V_{GS}=10V$	36			A
Drain-source On-Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=20A$		40	48	mΩ
		$V_{GS}=4.5V, I_D=20A$		42	52	
Forward Transconductance	g_{fs}	$V_{DS}=5V, I_D=20A$		35		S
Diode Forward Voltage	V_{SD}	$I_S=1.0A, V_{GS}=0V$			1.2	V
Dynamic						
Total Gate Charge	Q_g	$V_{DS}=10V, V_{DS}=30V$ $I_D=20A$		61	80	nC
Gate-Source Charge	Q_{gs}			12		
Gate-Drain Charge	Q_{gd}			16		
Input Capacitance	C_{iss}	$V_{DS} = 20V, V_{GS}=0V$ $F=1MHz$		2580		pF
Output Capacitance	C_{oss}			270		
Reverse Transfer Capacitance	C_{rss}			88		
Turn-On Time	$t_{d(on)}$ t_r	$V_{DD}=20V, R_L= 4\Omega$ $I_D=5.0A, V_{GEN}=10V$ $R_G=1\Omega$		20		nS
				19		
Turn-Off Time	$t_{d(off)}$ t_f			80		
				42		

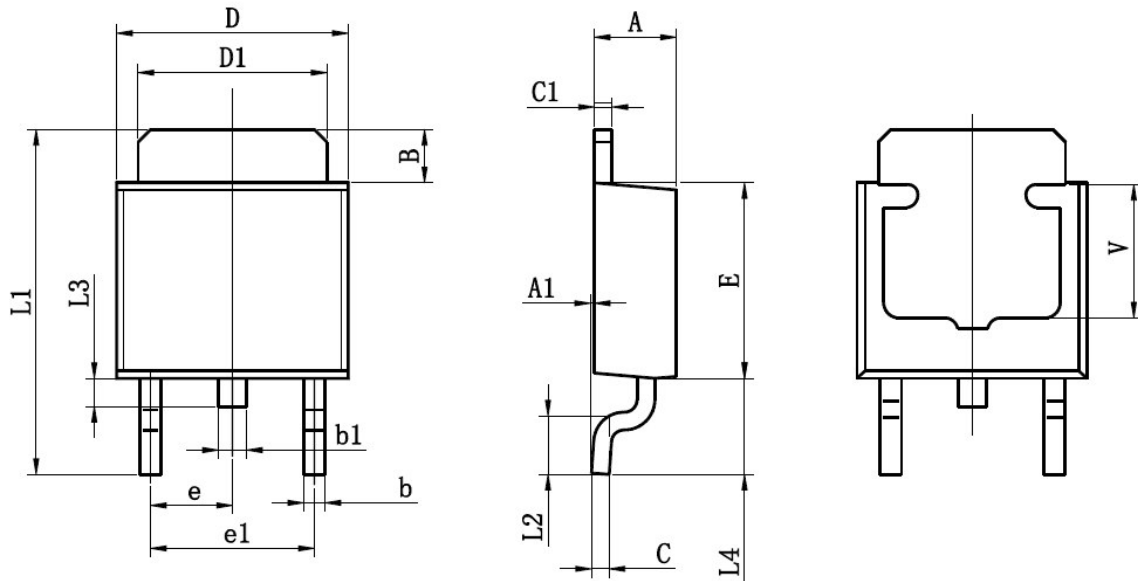
TYPICAL CHARACTERISTICS



TYPICAL CHARACTERISTICS

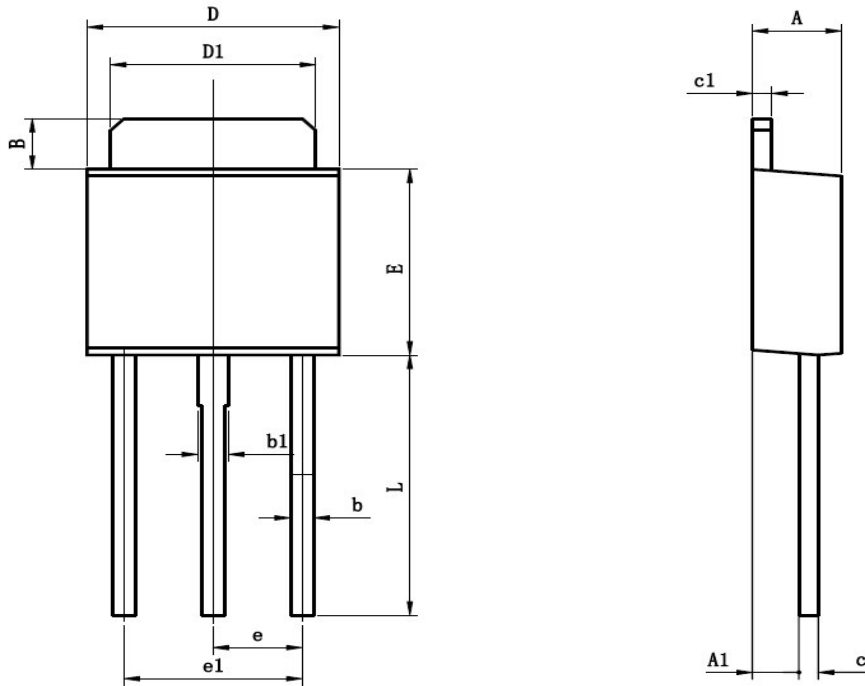


TO-252-2L PACKAGE OUTLINE SOP-8P



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	2.200	2.400	0.087	0.094
A1	0.000	0.127	0.000	0.005
B	1.350	1.650	0.053	0.065
b	0.500	0.700	0.020	0.028
b1	0.700	0.900	0.028	0.035
c	0.430	0.580	0.017	0.023
c1	0.430	0.580	0.017	0.023
D	6.350	6.650	0.250	0.262
D1	5.200	5.400	0.205	0.213
E	5.400	5.700	0.213	0.224
e	2.300TYP		0.091TYP	
e1	4.500	4.700	0.177	0.185
L1	9.500	9.900	0.374	0.390
L2	1.400	1.780	0.055	0.070
L3	0.650	0.950	0.026	0.037
L4	2.550	2.900	0.100	0.114
V	3.80REF		0.150REF	

TO-251 PACKAGE OUTLINE SOP-8P



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	2.200	2.400	0.087	0.094
A1	1.020	1.270	0.040	0.050
B	1.350	1.650	0.053	0.065
b	0.500	0.700	0.020	0.028
b1	0.700	0.900	0.028	0.035
c	0.430	0.580	0.017	0.023
c1	0.430	0.580	0.017	0.023
D	6.350	6.650	0.250	0.262
D1	5.200	5.400	0.205	0.213
E	5.400	5.700	0.213	0.224
e	2.300TYP		0.091TYP	
e1	4.500	4.700	0.177	0.185
L	7.500	7.900	0.295	0.311

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