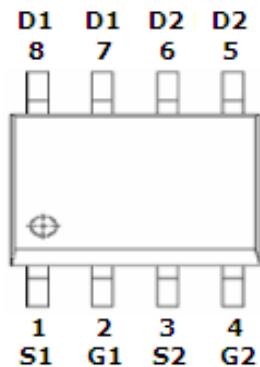
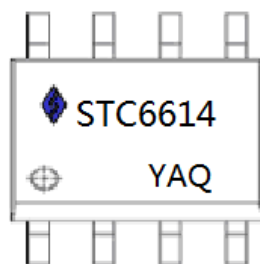


DESCRIPTION

The STC6614 is the N & P-Channel enhancement mode power field effect transistor using high cell density DMOS trench technology. This high density process is especially tailored to minimize on-state resistance and provide superior switching performance. This device is particularly suited for low voltage application such as notebook computer power management and other battery powered circuits, where high-side switching, low in-line power loss and resistance to transient are needed.

**PIN CONFIGURATION
SOP-8**

PART MARKING


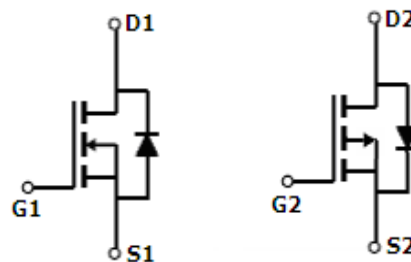
Y : Year
A : Product Code
Q : Process Code

FEATURE
N-Channel

- 60V/7.0A, $R_{DS(ON)} = 35m\Omega$ (Typ.)
@ $V_{GS} = 10V$
- 60V/4.0A, $R_{DS(ON)} = 40m\Omega$
@ $V_{GS} = 4.5V$

P-Channel

- -60V/-5.0A, $R_{DS(ON)} = 60m\Omega$ (Typ.)
@ $V_{GS} = -10V$
- -60V/-3.0A, $R_{DS(ON)} = 80m\Omega$
@ $V_{GS} = -4.5V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- SOP-8 package





STC6614 

N&P Pair Enhancement Mode MOSFET

7.0A / -5.0A

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C Unless otherwise noted)

Parameter	Symbol	Typical		Unit	
		N	P		
Drain-Source Voltage	V _{DSS}	60	-60	V	
Gate-Source Voltage	V _{GSS}	±20	±20	V	
Continuous Drain Current (T _J =150°C)	I _D	T _A =25°C	7.0	-5.0	A
		T _A =70°C	5.2	-4.0	
Pulsed Drain Current	I _{DM}	40	-30	A	
Continuous Source Current (Diode Conduction)	I _S	3	-3	A	
Power Dissipation	P _D	T _A =25°C	2.3	2.3	W
		T _A =70°C	1.3	1.3	
Operation Junction Temperature	T _J	150		°C	
Storage Temperature Range	T _{STG}	-55/150		°C	
Thermal Resistance-Junction to Ambient	R _{θJA}	T ≤ 10Sec	62.5	62.5	°C/W
		Steady State	110	110	



STC6614 

N&P Pair Enhancement Mode MOSFET

7.0A / -5.0A

ELECTRICAL CHARACTERISTICS (Ta = 25°C Unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit	
Static							
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=250\mu A$ $V_{GS}=0V, I_D=-250\mu A$	N P	60 -60		V	
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$ $V_{DS}=V_{GS}, I_D=-250\mu A$	N P	1.0 -1.0	3.0 -3.0	V	
Gate Leakage Current	I_{GSS}	$V_{DS}=0V, V_{GS}=\pm 20V$ $V_{DS}=0V, V_{GS}=\pm 20V$	N P		± 100 ± 100	nA	
Zero Gate Voltage Drain Current	I_{DSS} $T_J=55^\circ C$	$V_{DS}=48V, V_{GS}=0V$ $V_{DS}=-48V, V_{GS}=0V$ $V_{DS}=48V, V_{GS}=0V$ $V_{DS}=-48V, V_{GS}=0V$	N P N P		1 -1 5 -5	μA	
On-State Drain Current	$I_{D(on)}$	$V_{DS} \geq 5V, V_{GS}=10V$ $V_{DS} \leq -5V, V_{GS}=-10V$	N P	20 -20		A	
Drain-source On-Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=10.0A$ $V_{GS}=-10V, I_D=-10.0A$ $V_{GS}=4.5V, I_D=6.0A$ $V_{GS}=-4.5V, I_D=-5.0A$	N P N P		0.035 0.060 0.040 0.080	0.040 0.072 0.048 0.093	Ω
Forward Tran Conductance	g_{fs}	$V_{DS}=5V, I_D=6.3A$ $V_{DS}=-5V, I_D=-5.9A$	N P		27 18	S	
Diode Forward Voltage	V_{SD}	$I_S=1.0A, V_{GS}=0V$ $I_S=-1.7A, V_{GS}=0V$	N P		1.2 -1.2	V	
Dynamic							
Total Gate Charge	Q_g	N-Channel $V_{DS}=30V, V_{GS}=10V$ $I_D=6.3A$ P-Channel $V_{DS}=-30V, V_{GS}=-10V$ $I_D=-5.0A$	N P		47.7 45.2	nC	
Gate-Source Charge	Q_{gs}		N P		6 5.8		
Gate-Drain Charge	Q_{gd}		N P		14.5 9.6		
Turn-On Time	$t_{d(on)}$ t_r	N-Channel $V_{DS}=30V, R_L=4.7\Omega$ $V_{GS}=10V, R_{GEN}=3\Omega$ P-Channel $V_{DS}=-30V, R_L=6.2\Omega$ $V_{GS}=-10V, R_{GEN}=3\Omega$	N P N P		8 9 9 6.2	nS	
Turn-Off Time	$t_{d(off)}$ t_f		N P		25 44		
			N P		10 13.2		

TYPICAL CHARACTERISTICS (N MOS)

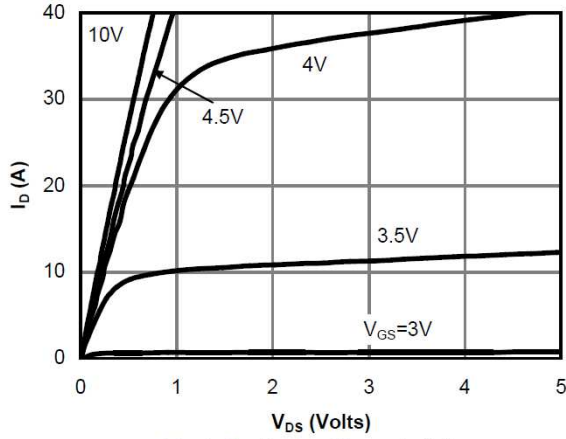


Fig 1: On-Region Characteristics

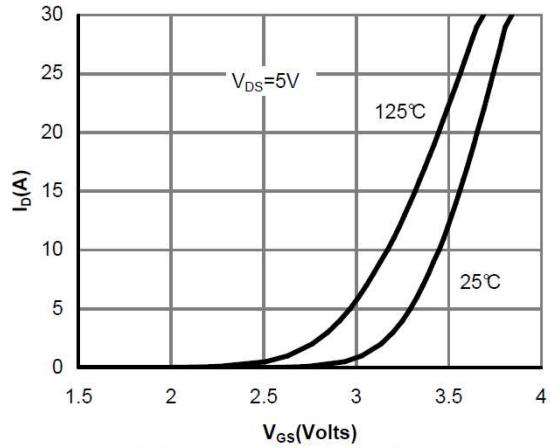


Figure 2: Transfer Characteristics

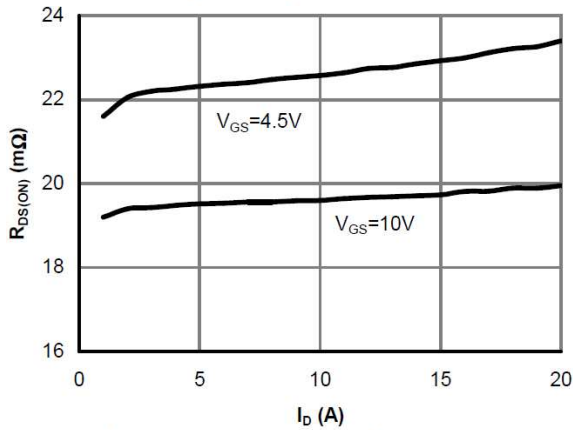


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

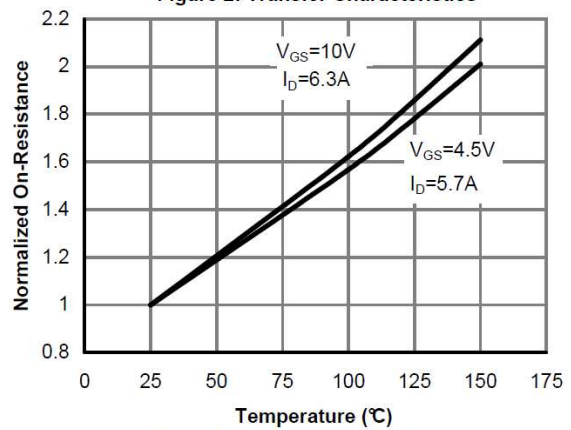


Figure 4: On-Resistance vs. Junction Temperature

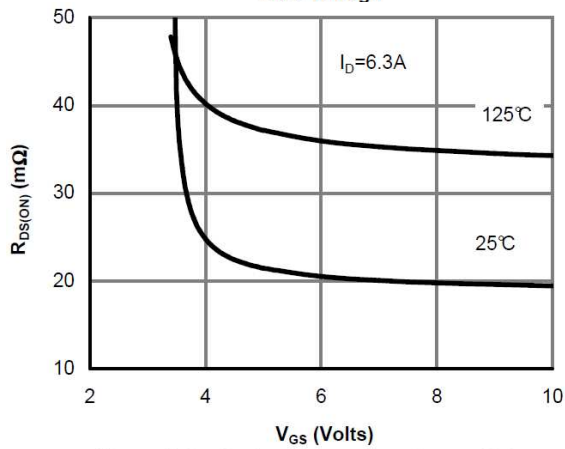


Figure 5: On-Resistance vs. Gate-Source Voltage

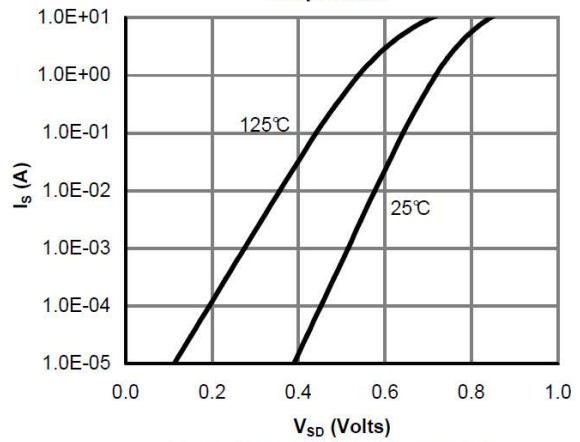


Figure 6: Body-Diode Characteristics

TYPICAL CHARACTERISTICS (N MOS)

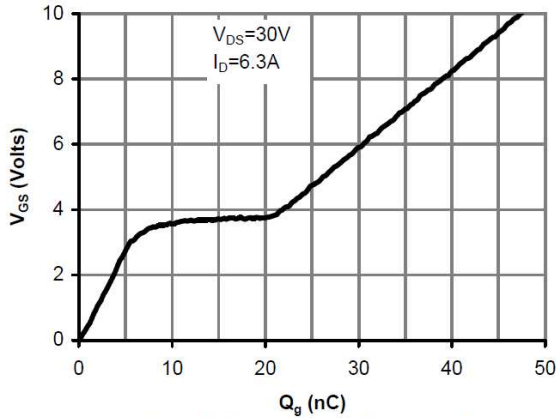


Figure 7: Gate-Charge Characteristics

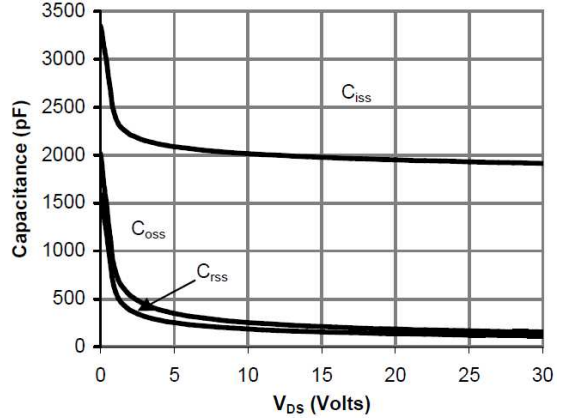


Figure 8: Capacitance Characteristics

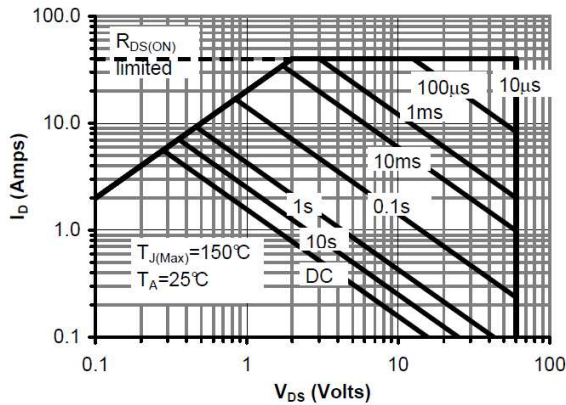


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

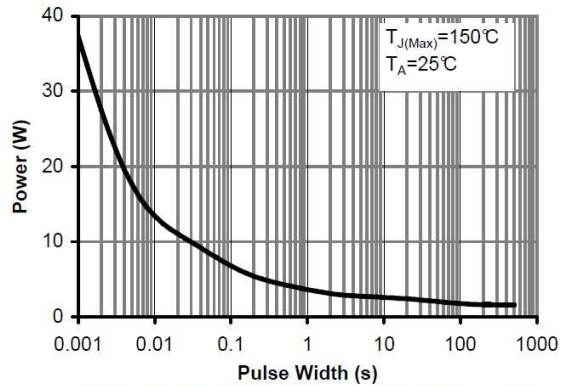


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

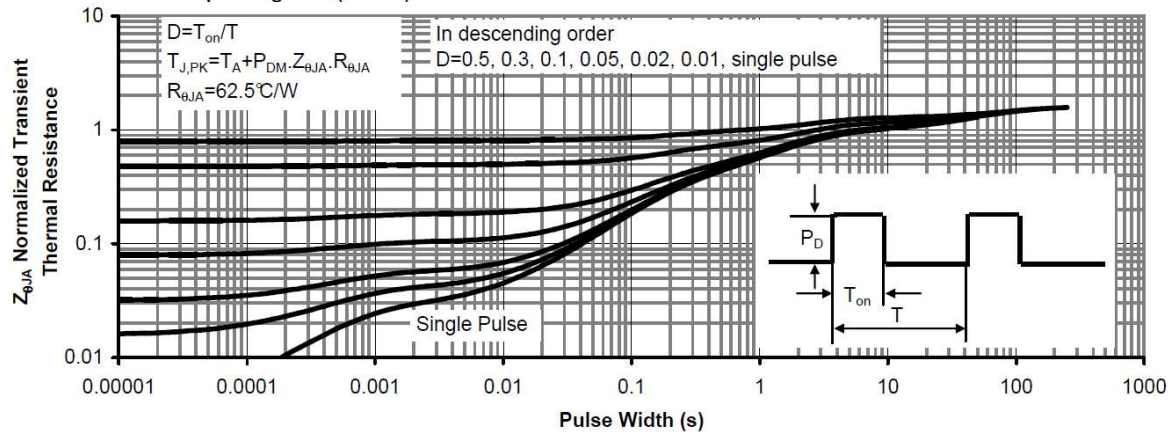


Figure 11: Normalized Maximum Transient Thermal Impedance

YPICAL CHARACTERISTICS (P MOS)

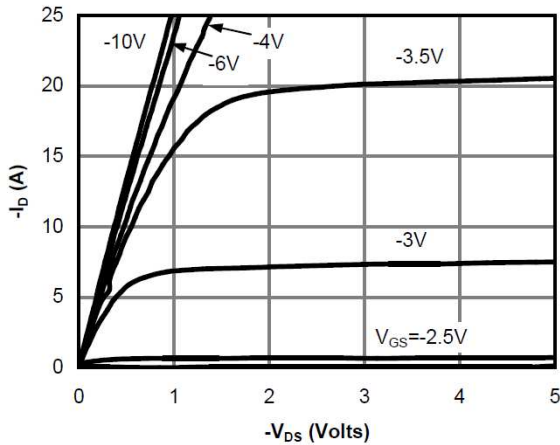


Figure 1: On-Region Characteristics

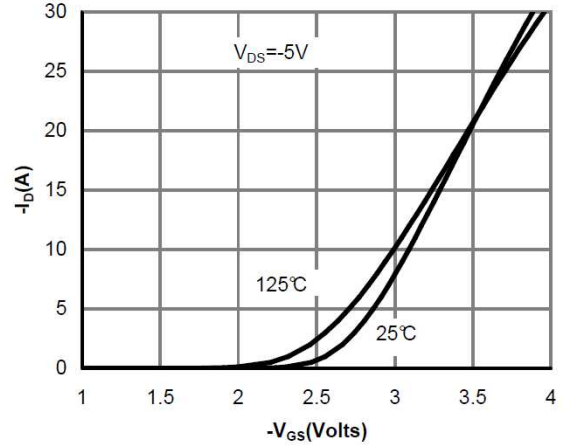


Figure 2: Transfer Characteristics

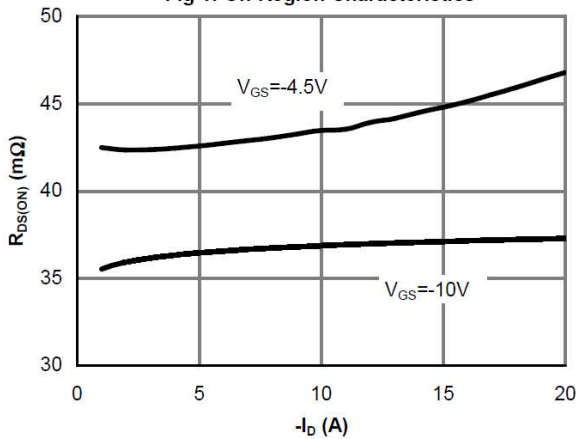


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

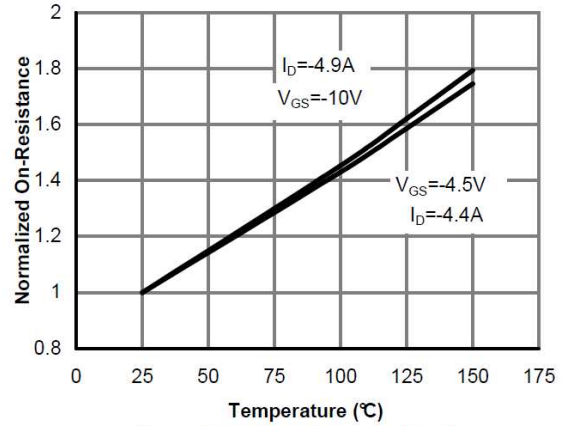


Figure 4: On-Resistance vs. Junction Temperature

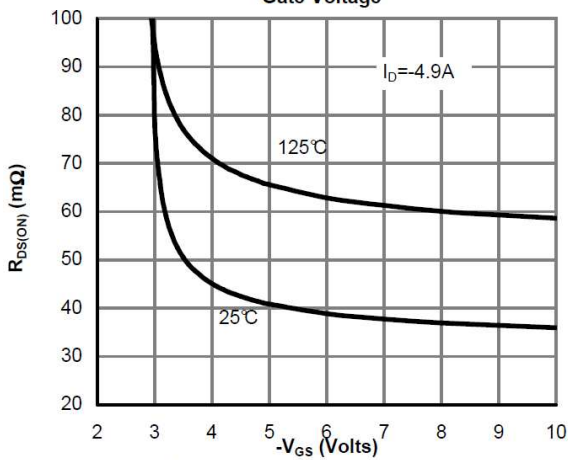


Figure 5: On-Resistance vs. Gate-Source Voltage

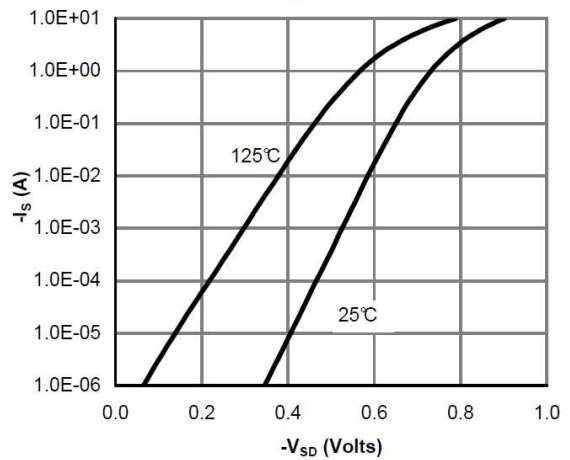


Figure 6: Body-Diode Characteristics

TYPICAL CHARACTERISTICS (P MOS)

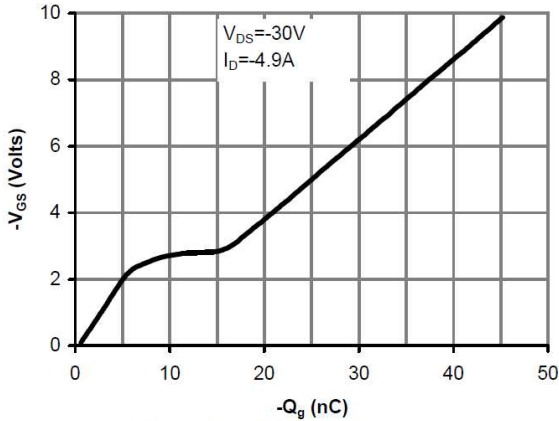


Figure 7: Gate-Charge Characteristics

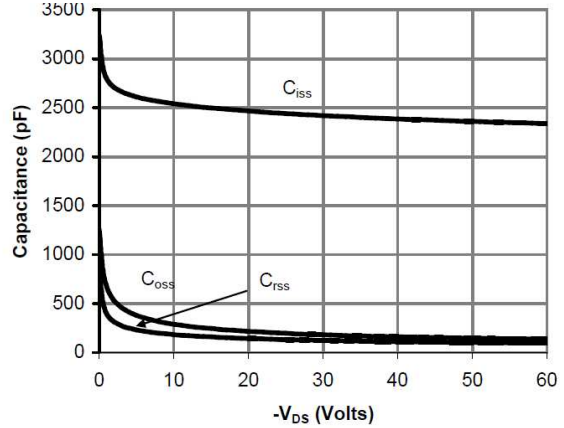


Figure 8: Capacitance Characteristics

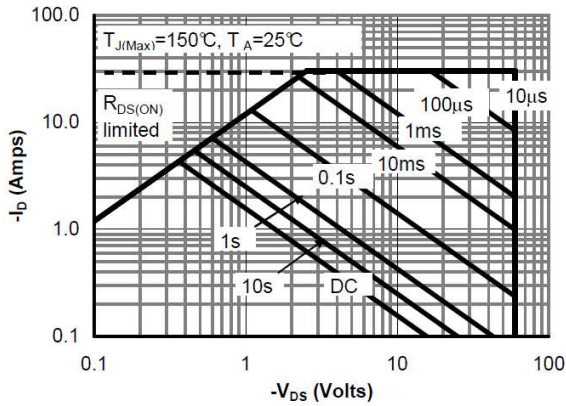


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

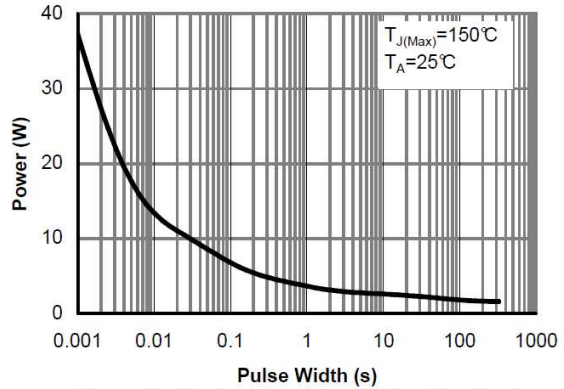


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

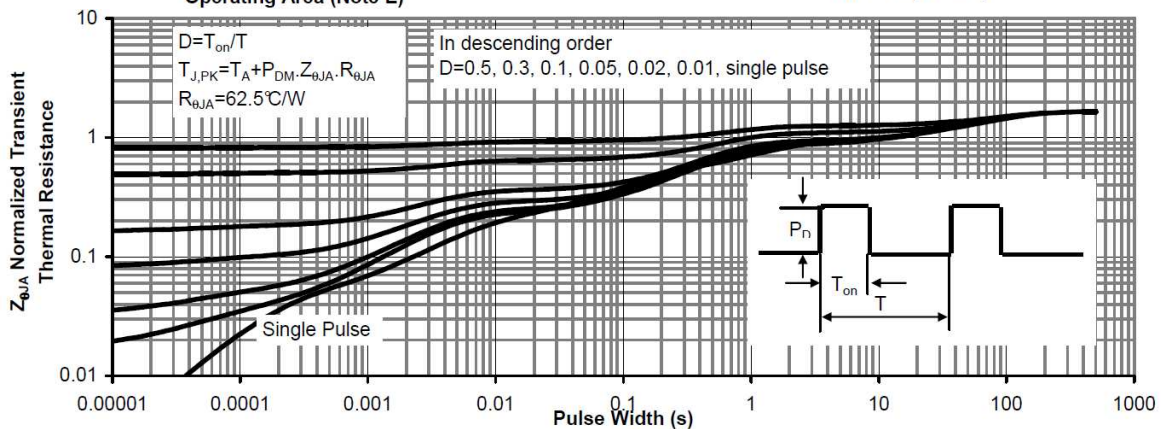
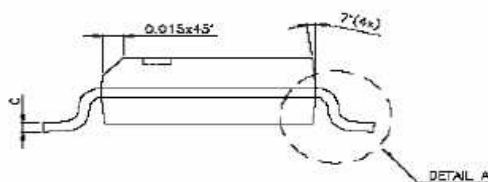
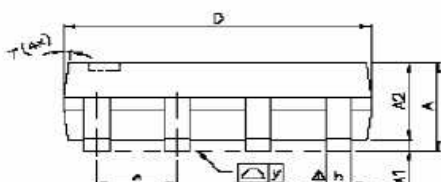
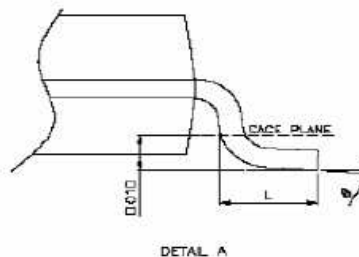
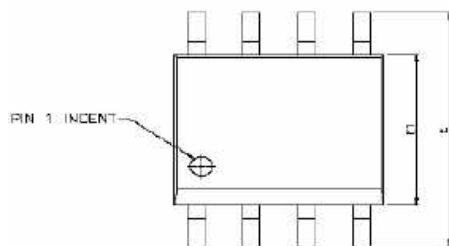


Figure 11: Normalized Maximum Transient Thermal Impedance

SOP-8 PACKAGE OUTLINE


SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.47	1.60	1.73	0.058	0.063	0.068
A1	0.10	—	0.25	0.004	—	0.010
A2	—	1.45	—	—	0.057	—
b	0.33	0.41	0.51	0.013	0.016	0.020
C	0.19	0.20	0.25	0.0075	0.008	0.0098
D	4.80	4.85	4.95	0.189	0.191	0.195
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e	—	1.27	—	—	0.050	—
L	0.38	0.71	1.27	0.015	0.028	0.050
Δ y	—	—	0.076	—	—	0.003
ϕ	0°	—	8°	0°	—	8°

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