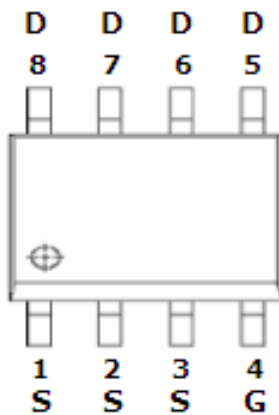
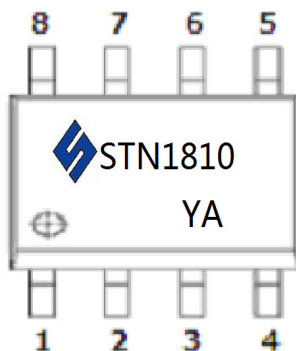


DESCRIPTION

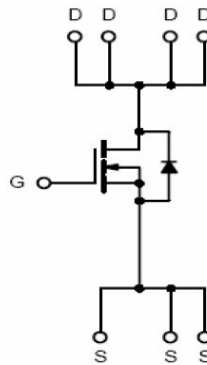
STN1810 is the N-Channel logic enhancement mode power field effect transistor which is produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance and provide superior switching performance. These applications such as notebook computer power management and other battery powered circuits where high-side switching, low in-line power loss and resistance to transients are melded.

**PIN CONFIGURATION
SOP-8**

PART MARKING


Y: Year Code
A: Process Code

FEATURE

- 100V/8.0A, $R_{DS(ON)} = 140m\Omega$ (Typ.) @ $V_{GS} = 10V$
- 100V/6.5.0A, $R_{DS(ON)} = 150m\Omega$ @ $V_{GS} = 7.0V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- SOP-8 package design



**STN1810**


N Channel Enhancement Mode MOSFET

8.0A

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C Unless otherwise noted)

Parameter	Symbol	Typical	Unit
Drain-Source Voltage	VDSS	100	V
Gate-Source Voltage	VGSS	±20	V
Continuous Drain Current (TJ=150°C)	ID	TA=25°C 8.0	A
		TA=70°C 6.0	
Pulsed Drain Current	IDM	12	A
Continuous Source Current (Diode Conduction)	IS	2.3	A
Power Dissipation	PD	TA=25°C 2.8	W
		TA=70°C 1.8	
Operation Junction Temperature	TJ	150	°C
Storage Temperature Range	TSTG	-55/150	°C
Thermal Resistance-Junction to Ambient	RθJA	80	°C/W



STN1810 

N Channel Enhancement Mode MOSFET

8.0A

ELECTRICAL CHARACTERISTICS (Ta = 25°C Unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=250\mu A$	100			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1.0		3.0	V
Gate Leakage Current	I_{GSS}	$V_{DS}=0V, V_{GS}=\pm 20V$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=80V, V_{GS}=0V$			250	uA
		$V_{DS}=80V, V_{GS}=0V$ $T_J=5^\circ C$			5	
On-State Drain Current	$I_{D(on)}$	$V_{DS} \geq 5V, V_{GS}=10V$	8			A
Drain-source On-Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=10A$		140	155	mΩ
		$V_{GS}=7.0V, I_D=6.5A$		150	170	
Forward Transconductance	g_{fs}	$V_{DS}=5V, I_D=6.2A$		5.6		S
Diode Forward Voltage	V_{SD}	$I_S=1A, V_{GS}=0V$			1.3	V
Dynamic						
Total Gate Charge	Q_g	$V_{DS}=80V, V_{GS}=5V$ $I_D=5A$		20		nC
Gate-Source Charge	Q_{gs}			3.5		
Gate-Drain Charge	Q_{gd}			5.2		
Input Capacitance	C_{iss}	$V_{DS} = 25V, V_{GS}=0V$ $F=1MHz$		630		pF
Output Capacitance	C_{oss}			68		
Reverse Transfer Capacitance	C_{rss}			43		
Turn-On Time	$t_{d(on)}$ t_r	$V_{DD}=50V, R_D=10\Omega$ $V_{DS}=30V, R_G=3.3\Omega$ $I_D=5A$		6.5		nS
				10		
Turn-Off Time	$t_{d(off)}$ t_f			13		
				3.4		

TYPICAL CHARACTERISTICS

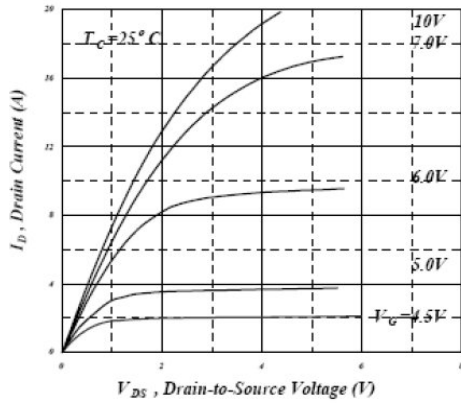


Fig 1. Typical Output Characteristics

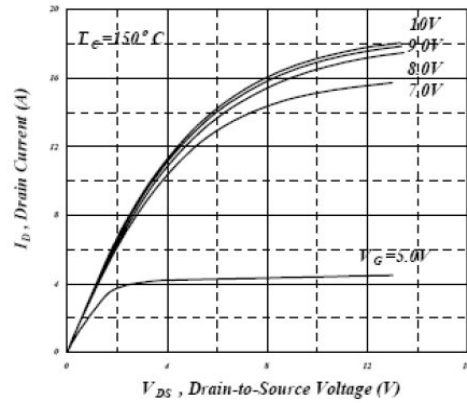


Fig 2. Typical Output Characteristics

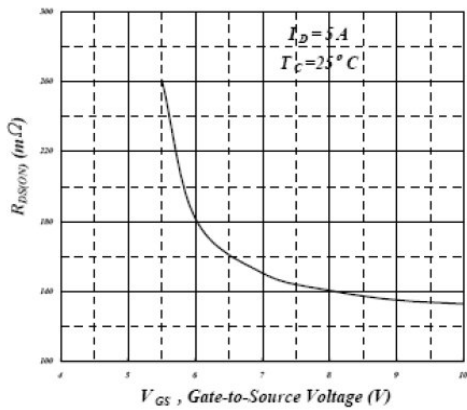


Fig 3. On-Resistance v.s. Gate Voltage

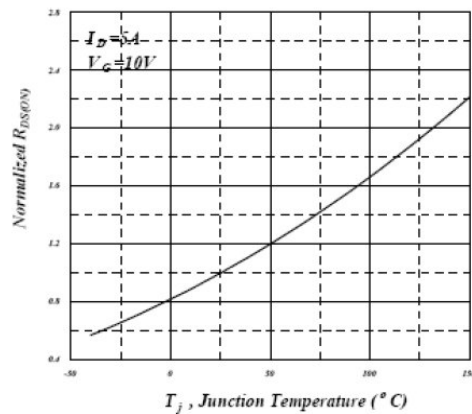


Fig 4. Normalized On-Resistance v.s. Junction Temperature

TYPICAL CHARACTERISTICS

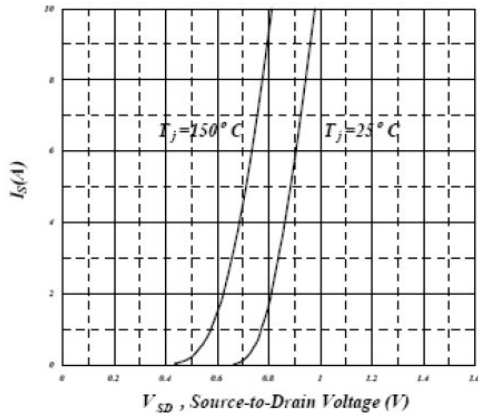


Fig 5. Forward Characteristic of Reverse Diode

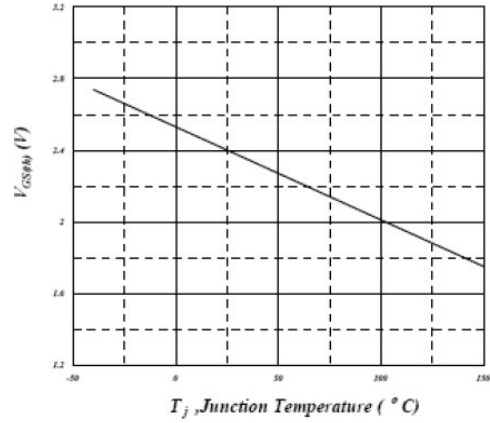


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

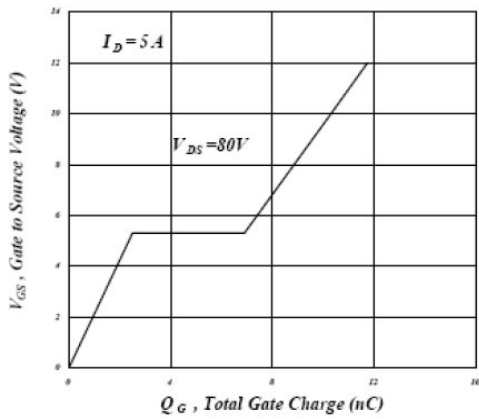


Fig 7. Gate Charge Characteristics

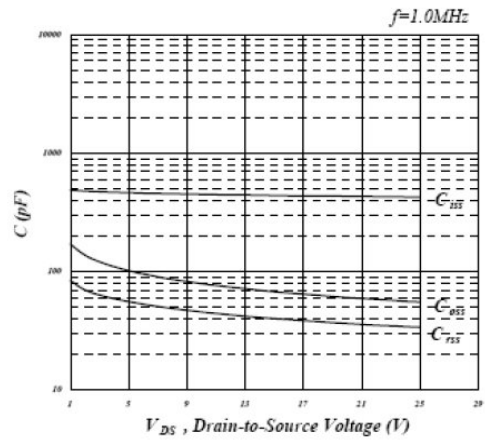


Fig 8. Typical Capacitance Characteristics

TYPICAL CHARACTERISTICS

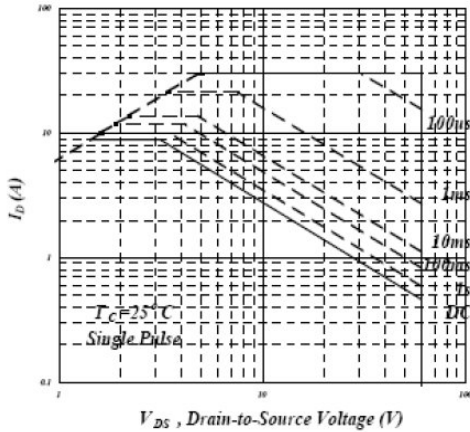


Fig 9. Maximum Safe Operating Area

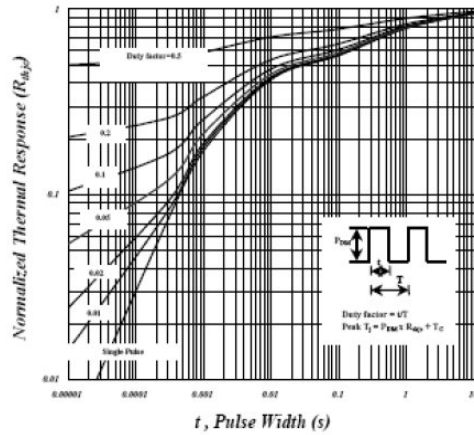


Fig 10. Effective Transient Thermal Impedance

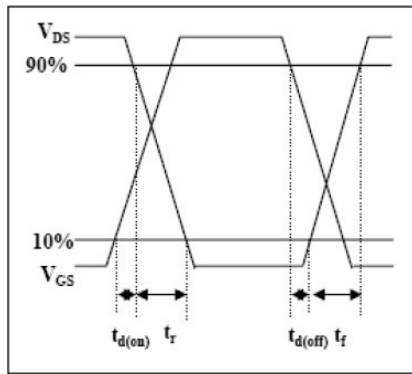


Fig 11. Switching Time Waveform

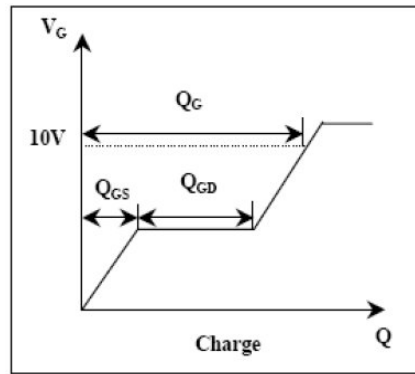
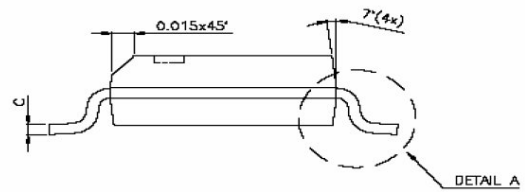
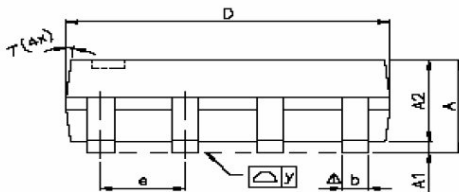
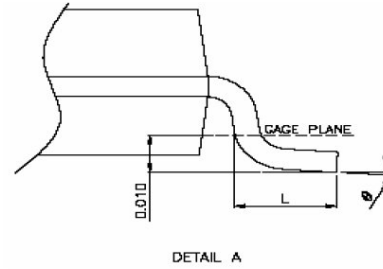
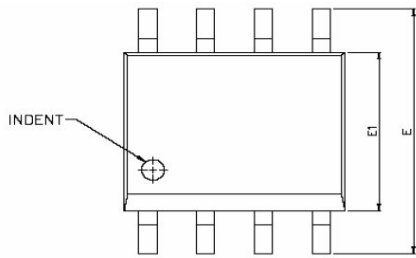


Fig 12. Gate Charge Waveform

PACKAGE OUTLINE SOP-8P


SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.47	1.60	1.73	0.058	0.063	0.068
A1	0.10	—	0.25	0.004	—	0.010
A2	—	1.45	—	—	0.057	—
b	0.33	0.41	0.51	0.013	0.016	0.020
C	0.19	0.20	0.25	0.0075	0.008	0.0098
D	4.80	4.85	4.95	0.189	0.191	0.195
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e	—	1.27	—	—	0.050	—
L	0.38	0.71	1.27	0.015	0.028	0.050
Δ y	—	—	0.076	—	—	0.003
\varnothing	0°	—	8°	0°	—	8°

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