![ST logo]

74LCX373

OCTAL D-TYPE LATCH NON-INVERTING (3-STATE) WITH 5V TOLERANT INPUTS AND OUTPUTS

- 5V TOLERANT INPUTS AND OUTPUTS
- HIGH SPEED:
  $t_{PD} = 8.0$ ns (MAX.) at $V_{CC} = 3V$
- POWER DOWN PROTECTION ON INPUTS AND OUTPUTS
- SYMMETRICAL OUTPUT IMPEDANCE:
  $|I_{OH}| = I_{OL} = 24mA$ (MIN) at $V_{CC} = 3V$
- PCI BUS LEVELS GUARANTEED AT 24 mA
- BALANCED PROPAGATION DELAYS:
  $t_{PLH} \cong t_{PHL}$
- OPERATING VOLTAGE RANGE:
  $V_{CC}(OPR) = 2.0V$ to $3.6V$ (1.5V Data Retention)
- PIN AND FUNCTION COMPATIBLE WITH 74 SERIES 373
- LATCH-UP PERFORMANCE EXCEEDS 500mA (JESD 17)
- ESD PERFORMANCE:
  HBM > 2000V (MIL STD 883 method 3015);
  MM > 200V

DESCRIPTION

The 74LCX373 is a low voltage CMOS OCTAL D-TYPE LATCH with 3 STATE OUTPUT NON-INVERTING fabricated with sub-micron silicon gate and double-layer metal wiring C^2MOS technology. It is ideal for low power and high speed 3.3V applications; it can be interfaced to 5V signal environment for both inputs and outputs.

These 8 bit D-Type latch are controlled by a latch

SOP　　**TSSOP**
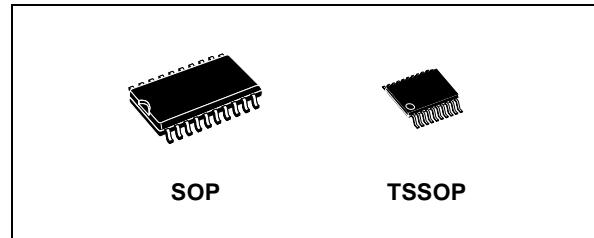
Table 1: Order Codes

PACKAGE	T & R
SOP	74LCX373MTR
TSSOP	74LCX373TTR

enable input (LE) and an output enable input ($\overline{OE}$). While the LE inputs is held at a high level, the Q outputs will follow the data input. When the LE is taken low, the Q outputs will be latched precisely at the logic level of D input data. While the ($\overline{OE}$) input is low, the 8 outputs will be in a normal logic state (high or low logic level) and while ($\overline{OE}$) is in high level, the outputs will be in a high impedance state.

It has same speed performance at 3.3V than 5V AC/ACT family, combined with a lower power consumption.

All inputs and outputs are equipped with protection circuits against static discharge, giving them 2KV ESD immunity and transient excess voltage.

Figure 1: Pin Connection And IEC Logic Symbols
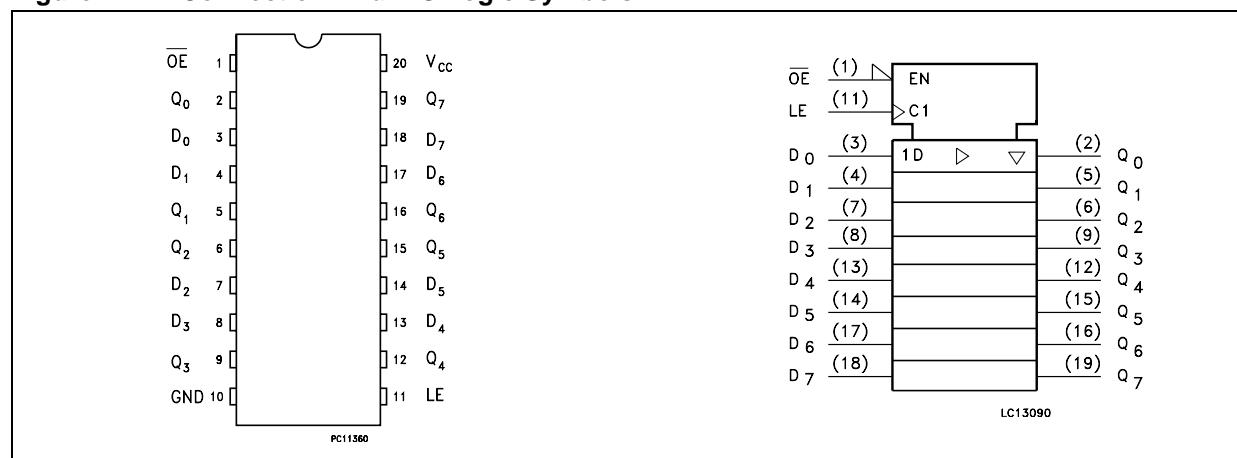
Figure 2: Input And Output Equivalent Circuit

SC13540
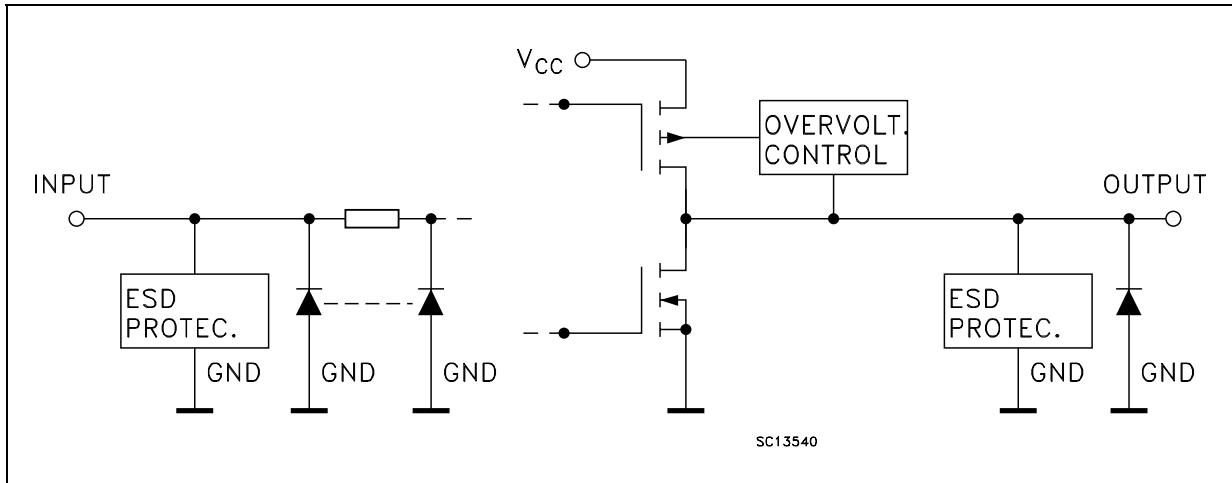
Table 2: Pin Description

PIN N°	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}$	3 State Output Enable Input (Active LOW)
2, 5, 6, 9, 12, 15, 16,19	D0 to D7	Data Inputs
3, 4, 7, 8, 13, 14, 17, 18	Q0 to Q7	3-State Outputs
11	LE	Latch Enable Input
10	GND	Ground (0V)
20	V_{CC}	Positive Supply Voltage

Table 3: Truth Table

INPUT			OUTPUT
$\overline{OE}$	LE	D	Q
H	X	X	Z
L	L	X	NO CHANGE*
L	H	L	L
L	H	H	H

X : Don't Care
Z : High Impedance
* : Q Outputs are latched at the time when the LE input is taken LOW.

Figure 3: Logic Diagram

LC13510
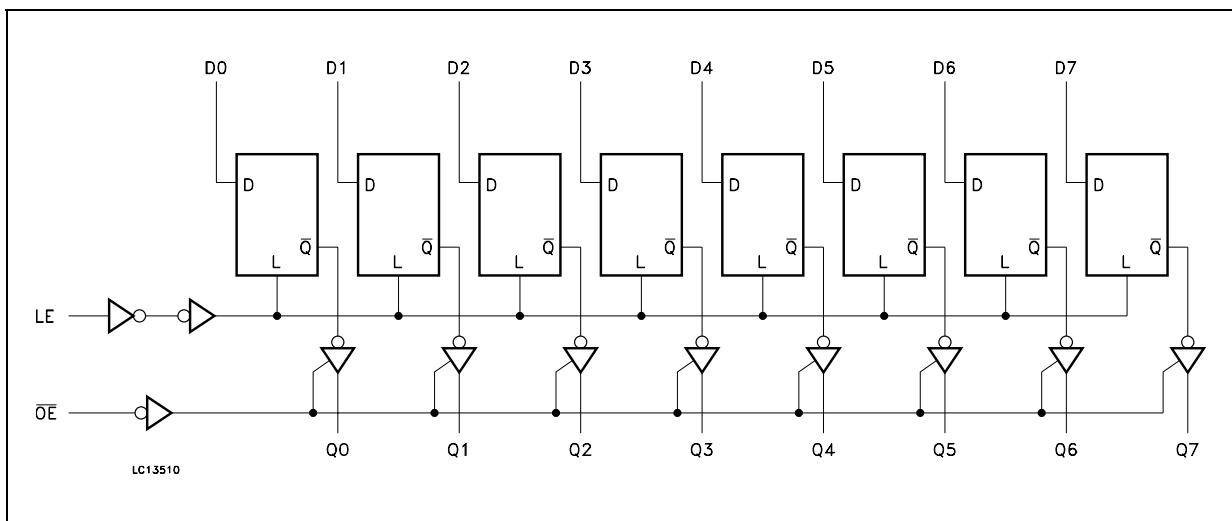
This logic diagram has not be used to estimate propagation delays

Table 4: Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7.0	V
V_I	DC Input Voltage	-0.5 to +7.0	V
V_O	DC Output Voltage (OFF State)	-0.5 to +7.0	V
V_O	DC Output Voltage (High or Low State) (note 1)	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	- 50	mA
I_{OK}	DC Output Diode Current (note 2)	- 50	mA
I_O	DC Output Current	$\pm$ 50	mA
I_{CC}	DC Supply Current per Supply Pin	$\pm$ 100	mA
I_{GND}	DC Ground Current per Supply Pin	$\pm$ 100	mA
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied
1) I_O absolute maximum rating must be observed
2) V_O < GND

Table 5: Recommended Operating Conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage (note 1)	2.0 to 3.6	V
V_I	Input Voltage	0 to 5.5	V
V_O	Output Voltage (OFF State)	0 to 5.5	V
V_O	Output Voltage (High or Low State)	0 to V_{CC}	V
I_{OH}, I_{OL}	High or Low Level Output Current (V_{CC} = 3.0 to 3.6V)	$\pm$ 24	mA
I_{OH}, I_{OL}	High or Low Level Output Current (V_{CC} = 2.7V)	$\pm$ 12	mA
T_{op}	Operating Temperature	-55 to 125	°C
dt/dv	Input Rise and Fall Time (note 2)	0 to 10	ns/V

1) Truth Table guaranteed: 1.5V to 3.6V
2) V_{IN} from 0.8V to 2V at V_{CC} = 3.0V

Table 6: DC Specifications

Symbol	Parameter	Test Condition		Value				Unit
		V_{CC} (V)		-40 to 85 °C		-55 to 125 °C		
				Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.7 to 3.6		2.0		2.0		V
V_{IL}	Low Level Input Voltage				0.8		0.8	V
V_{OH}	High Level Output Voltage	2.7 to 3.6	I_O=-100 µA	V_{CC}-0.2		V_{CC}-0.2		V
		2.7	I_O=-12 mA	2.2		2.2		
		3.0	I_O=-18 mA	2.4		2.4		
			I_O=-24 mA	2.2		2.2		
V_{OL}	Low Level Output Voltage	2.7 to 3.6	I_O=100 µA		0.2		0.2	V
		2.7	I_O=12 mA		0.4		0.4	
		3.0	I_O=16 mA		0.4		0.4	
			I_O=24 mA		0.55		0.55	
I_I	Input Leakage Current	2.7 to 3.6	V_I = 0 to 5.5V		± 5		± 5	µA
I_{off}	Power Off Leakage Current	0	V_I or V_O = 5.5V		10		10	µA
I_{OZ}	High Impedance Output Leakage Current	2.7 to 3.6	V_I = V_{IH} or V_{IL} V_O = 0 to V_{CC}		± 5		± 5	µA
I_{CC}	Quiescent Supply Current	2.7 to 3.6	V_I = V_{CC} or GND		10		10	µA
			V_I or V_O= 3.6 to 5.5V		± 10		± 10	
ΔI_{CC}	I_{CC} incr. per Input	2.7 to 3.6	V_{IH} = V_{CC} - 0.6V		500		500	µA

Table 7: Dynamic Switching Characteristics

Symbol	Parameter	Test Condition		Value			Unit
		V_{CC} (V)		T_A = 25 °C			
				Min.	Typ.	Max.	
V_{OLP}	Dynamic Low Level Quiet Output (note 1)	3.3	C_L = 50pF V_{IL} = 0V, V_{IH} = 3.3V		0.8		V
V_{OLV}					-0.8		

1) Number of outputs defined as "n". Measured with "n-1" outputs switching from HIGH to LOW or LOW to HIGH. The remaining output is measured in the LOW state.

Table 8: AC Electrical Characteristics

Symbol	Parameter	Test Condition				Value				Unit
		V_{CC} (V)	C_L (pF)	R_L (Ω)	$t_s = t_r$ (ns)	-40 to 85 °C		-55 to 125 °C		
						Min.	Max.	Min.	Max.	
t_{PLH} t_{PHL}	Propagation Delay Time (Dn to Qn)	2.7	50	500	2.5	1.5	9.0	1.5	9.0	ns
		3.0 to 3.6				1.5	8.0	1.5	8.0	
t_{PLH} t_{PHL}	Propagation Delay Time (LE to Qn)	2.7	50	500	2.5	1.5	9.5	1.5	9.5	ns
		3.0 to 3.6				1.5	8.5	1.5	8.5	
t_{PZL} t_{PZH}	Output Enable Time to HIGH and LOW level	2.7	50	500	2.5	1.5	9.5	1.5	9.5	ns
		3.0 to 3.6				1.5	8.5	1.5	8.5	
t_{PLZ} t_{PHZ}	Output Disable Time from HIGH to LOW level	2.7	50	500	2.5	1.5	8.5	1.5	8.5	ns
		3.0 to 3.6				1.5	7.5	1.5	7.5	
t_S	Set-Up Time, HIGH or LOW level (Dn to LE)	2.7	50	500	2.5	2.5		2.5		ns
		3.0 to 3.6				2.5		2.5		
t_h	Hold Time, HIGH or LOW level (Dn to LE)	2.7	50	500	2.5	1.5		1.5		ns
		3.0 to 3.6				1.5		1.5		
t_W	LE Pulse Width, HIGH	2.7	50	500	2.5	3.3		3.3		ns
		3.0 to 3.6				3.3		3.3		
t_{OSLH} t_{OSHL}	Output To Output Skew Time (note1, 2)	3.0 to 3.6	50	500	2.5		1.0		1.0	ns

1) Skew is defined as the absolute value of the difference between the actual propagation delay for any two outputs of the same device switching in the same direction, either HIGH or LOW ($t_{OSLH} = | t_{PLHm} - t_{PLHn}|$, $t_{OSHL} = | t_{PHLm} - t_{PHLn}|$)
2) Parameter guaranteed by design

Table 9: Capacitive Characteristics

Symbol	Parameter	Test Condition		Value			Unit
		V_{CC} (V)		T_A = 25 °C			
				Min.	Typ.	Max.	
C_{IN}	Input Capacitance	3.3	V_{IN} = 0 to V_{CC}		6		pF
C_{OUT}	Output Capacitance	3.3	V_{IN} = 0 to V_{CC}		12		pF
C_{PD}	Power Dissipation Capacitance (note 1)	3.3	f_{IN} = 10MHz V_{IN} = 0 or V_{CC}		50		pF

1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. $I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/8$ (per latch)

Figure 4: Test Circuit

SC08900
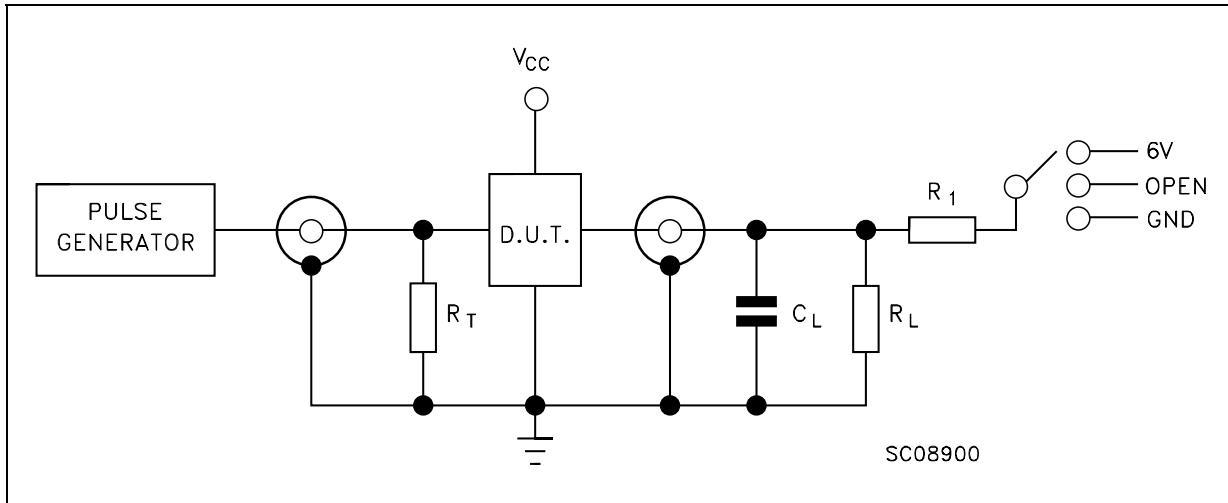
TEST	SWITCH
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	6V
t_{PZH}, t_{PHZ}	GND

C_L = 50 pF or equivalent (includes jig and probe capacitance)
R_L = R1 = 500Ω or equivalent
R_T = Z_{OUT} of pulse generator (typically 50Ω)

**Figure 5: Waveform - LE To Qn Propagation Delays, LE Minimum Pulse Width, Dn To LE Setup And Hold Times** (f=1MHz; 50% duty cycle)


SC10390
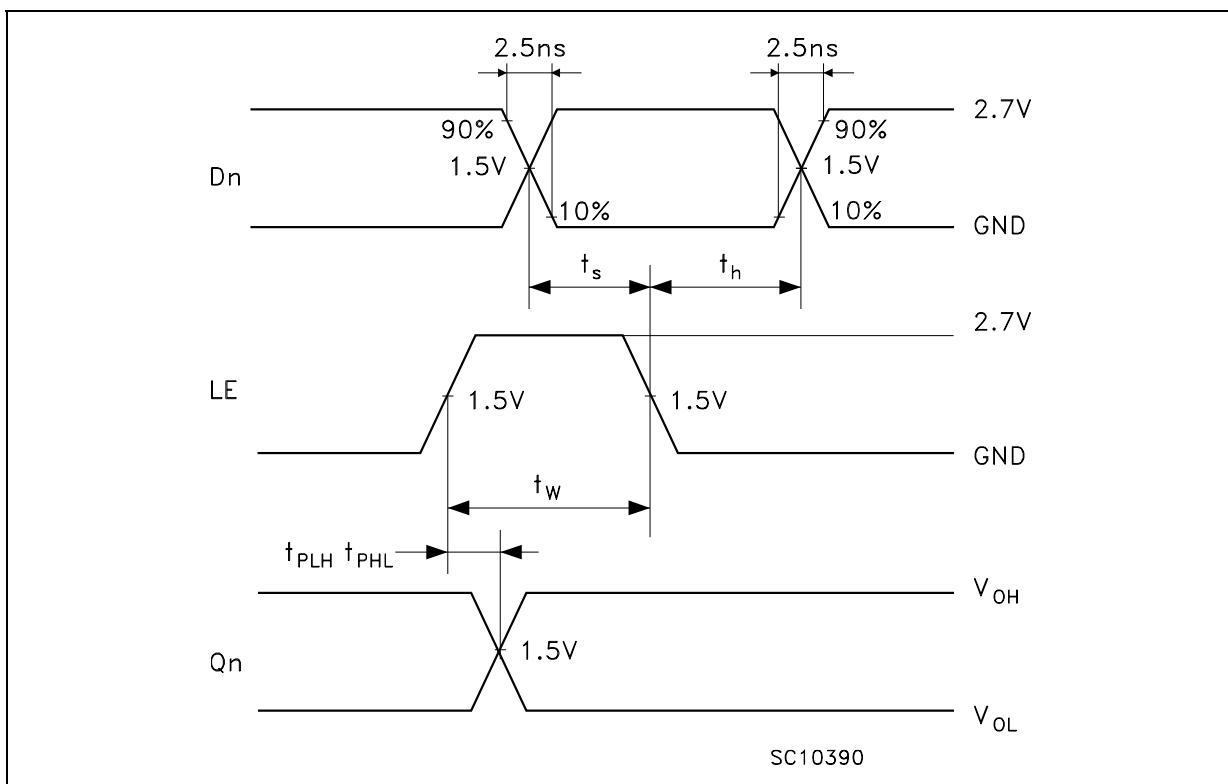
Figure 6: Waveform - Output Enable And Disable Times (f=1MHz; 50% duty cycle)

SC10370
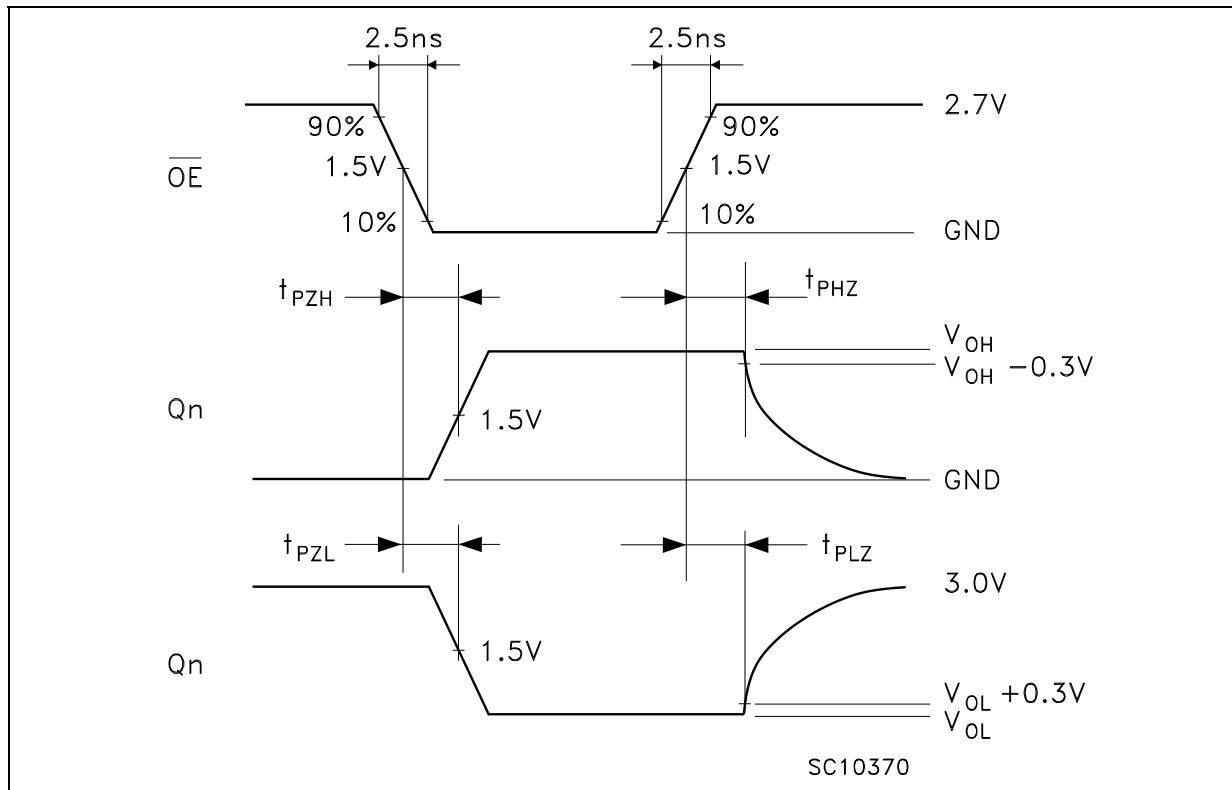
Figure 7: Waveform - Propagation Delay Time (f=1MHz; 50% duty cycle)

SC10401
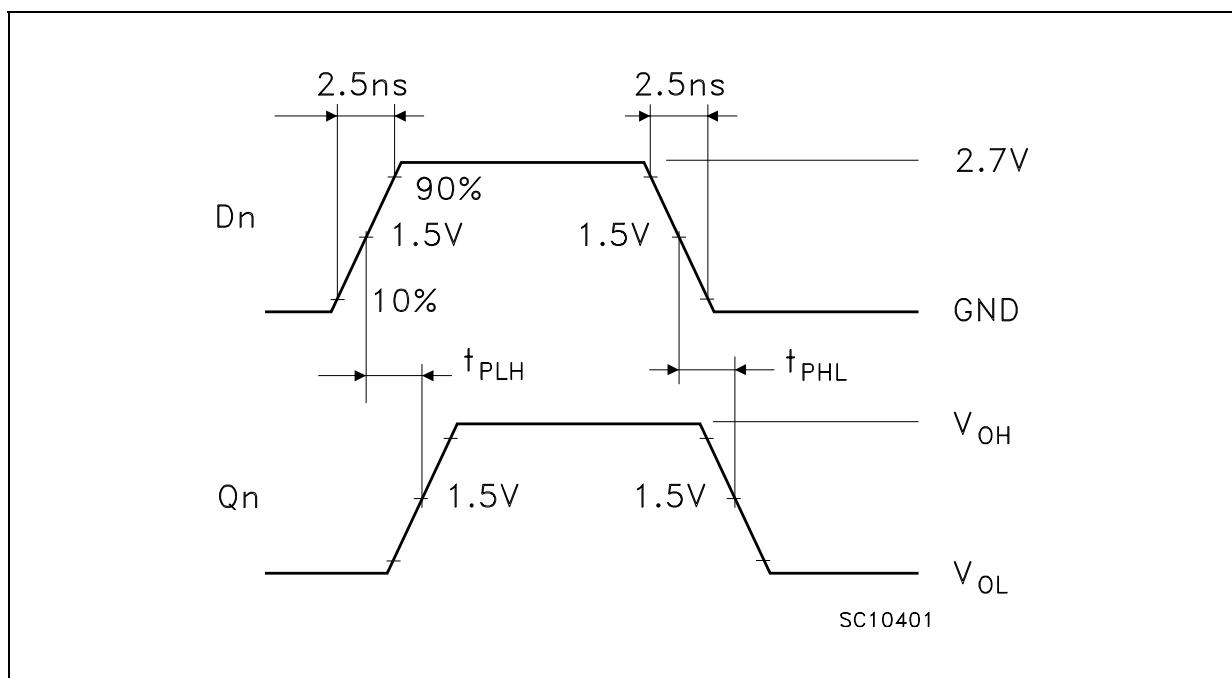
SO-20 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	2.35		2.65	0.093		0.104
A1	0.1		0.30	0.004		0.012
B	0.33		0.51	0.013		0.020
C	0.23		0.32	0.009		0.013
D	12.60		13.00	0.496		0.512
E	7.4		7.6	0.291		0.299
e		1.27			0.050	
H	10.00		10.65	0.394		0.419
h	0.25		0.75	0.010		0.030
L	0.4		1.27	0.016		0.050
k	0°		8°	0°		8°
ddd			0.100			0.004

0016022D
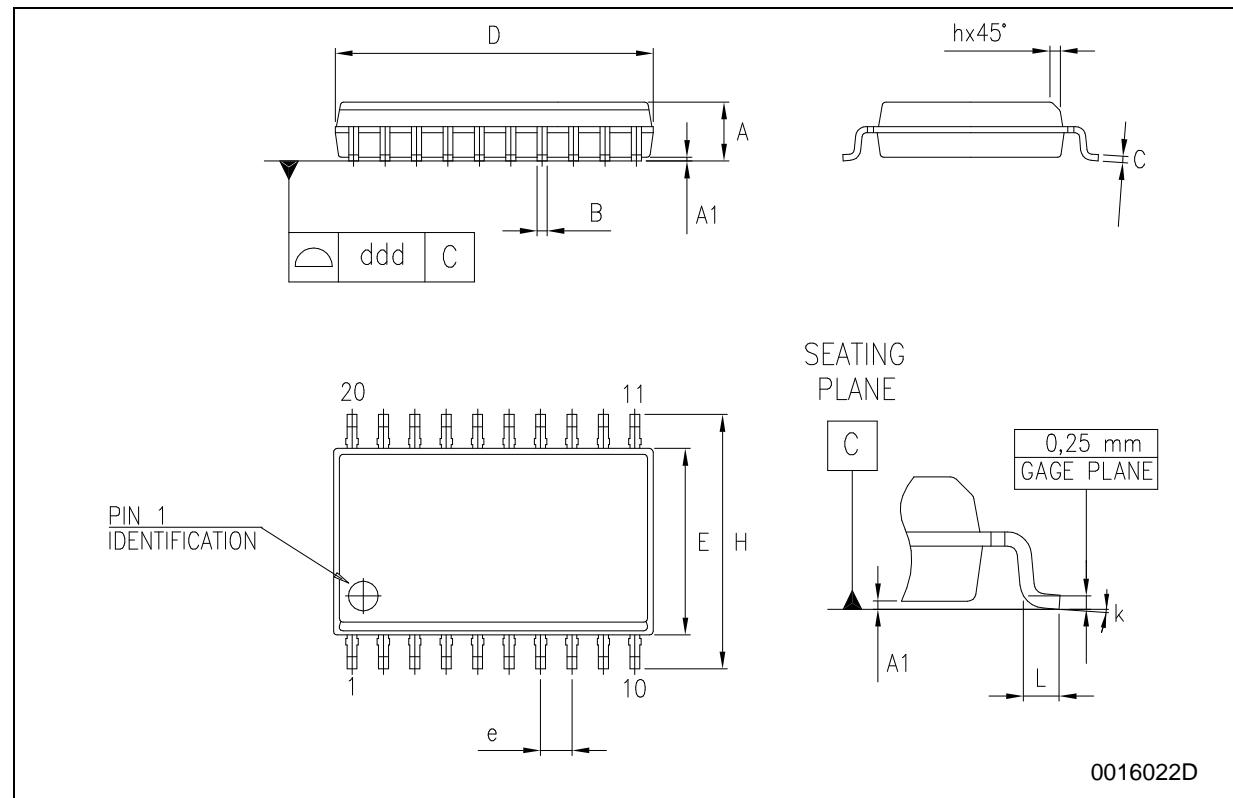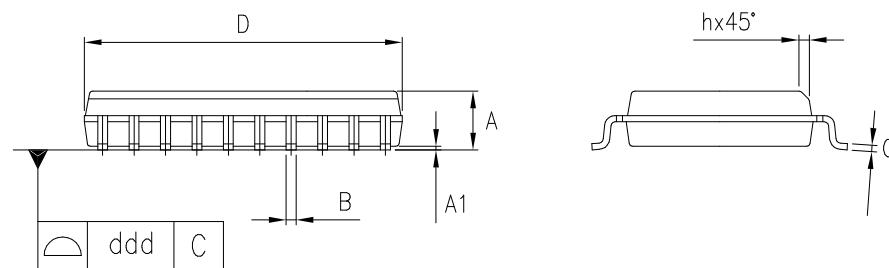
TSSOP20 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.2			0.047
A1	0.05		0.15	0.002	0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0079
D	6.4	6.5	6.6	0.252	0.256	0.260
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030

PIN 1 IDENTIFICATION

1

0087225C
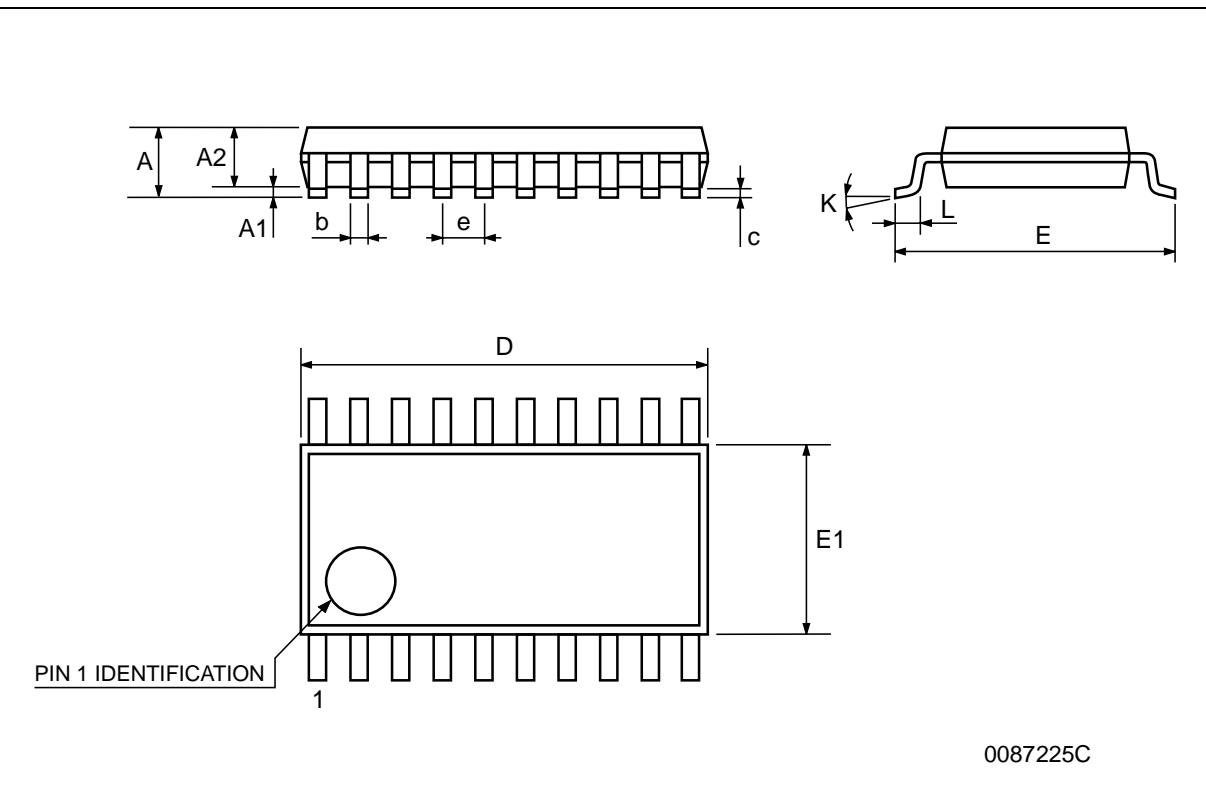
Tape & Reel SO-20 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	**TYP**	**MAX.**	**MIN.**	**TYP.**	**MAX.**
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			30.4			1.197
Ao	10.8		11	0.425		0.433
Bo	13.2		13.4	0.520		0.528
Ko	3.1		3.3	0.122		0.130
Po	3.9		4.1	0.153		0.161
P	11.9		12.1	0.468		0.476

Note: Drawing not in scale
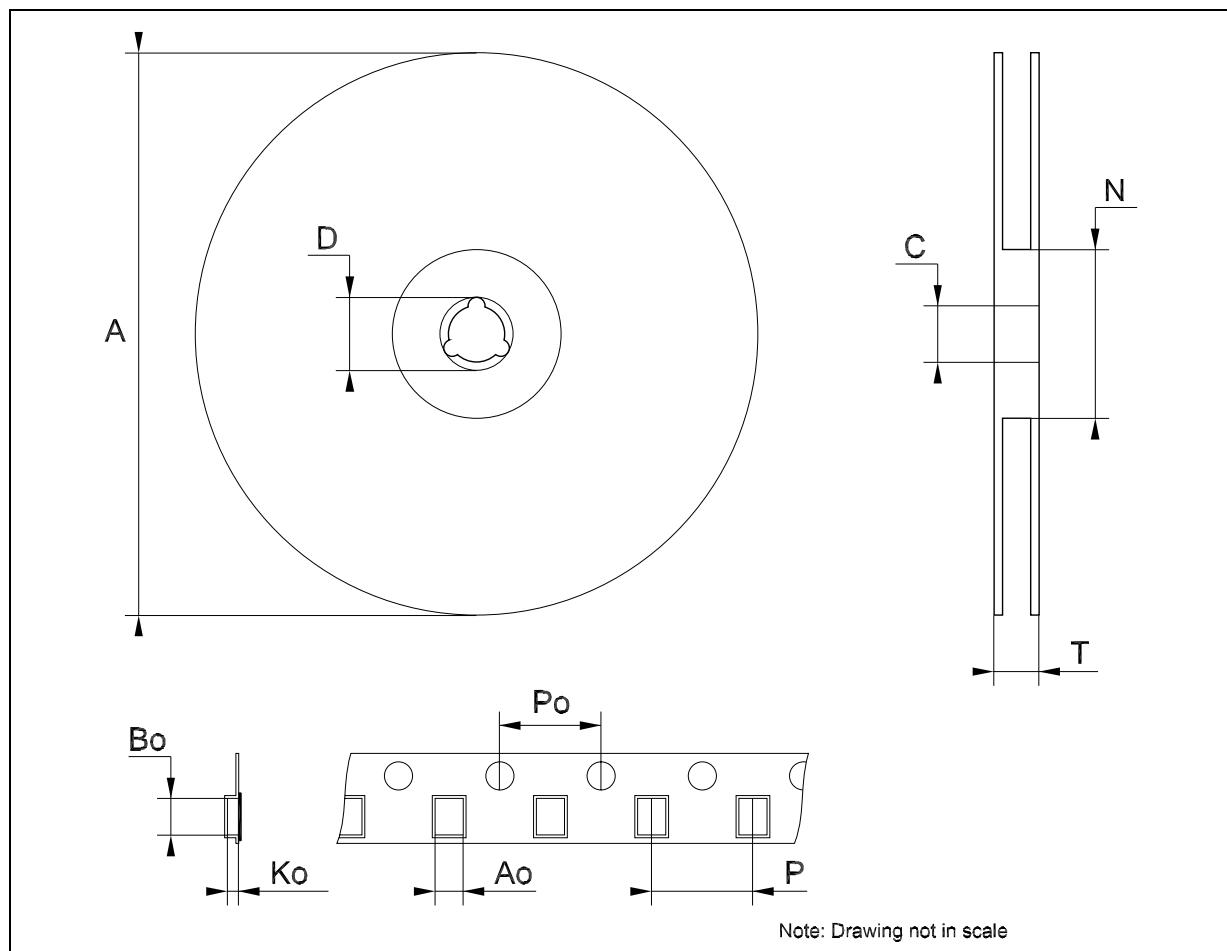
Tape & Reel TSSOP20 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			22.4			0.882
Ao	6.8		7	0.268		0.276
Bo	6.9		7.1	0.272		0.280
Ko	1.7		1.9	0.067		0.075
Po	3.9		4.1	0.153		0.161
P	11.9		12.1	0.468		0.476

Note: Drawing not in scale
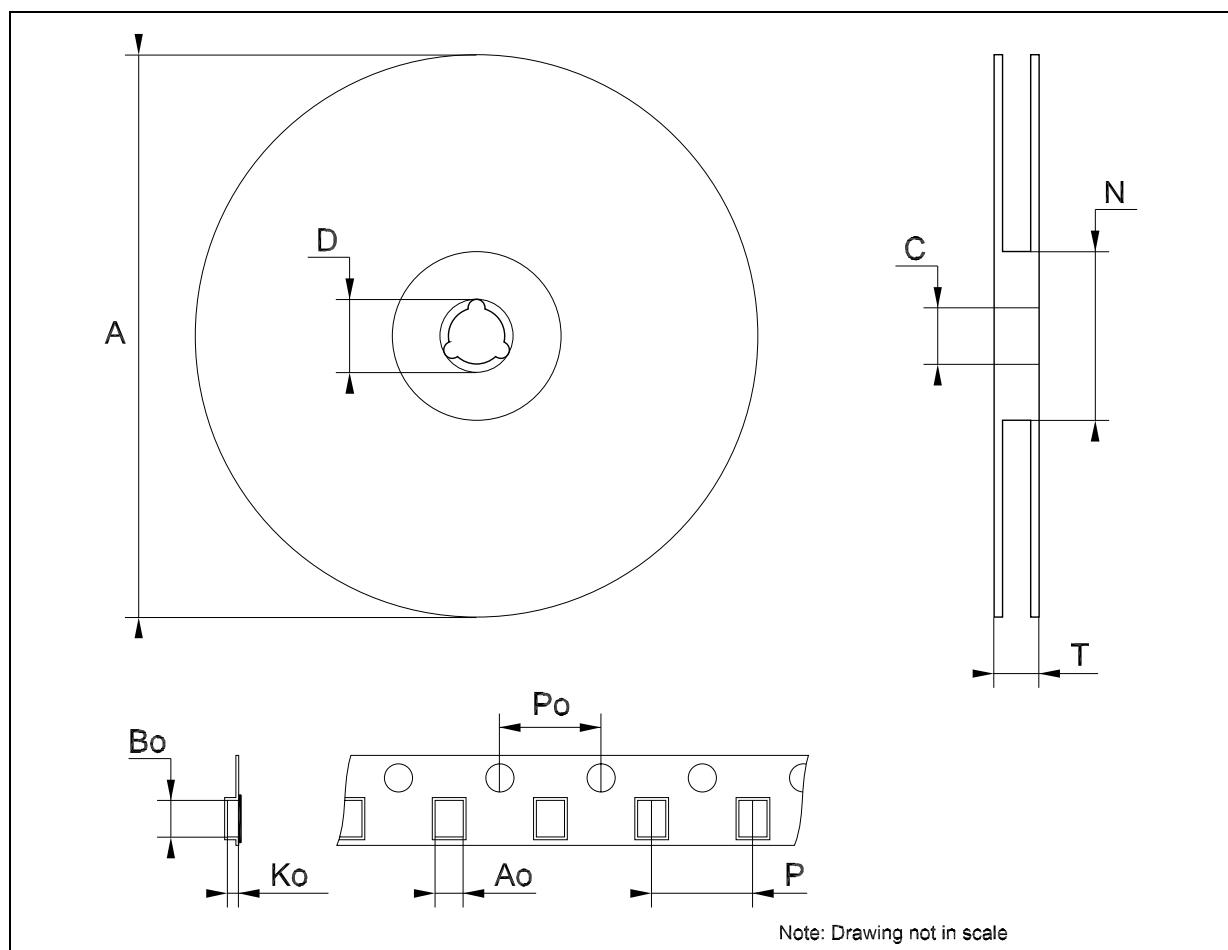
Table 10: Revision History

Date	Revision	Description of Changes
15-Sep-2004	5	Ordering Codes Revision - pag. 1.

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