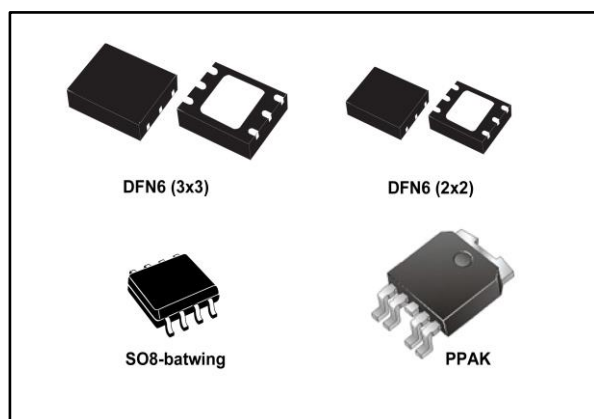


## 1.2 A low quiescent current LDO with reverse current protection

Datasheet - production data



### Features

- Input voltage from 1.6 to 5.5 V
- Very low-dropout voltage (300 mV typ. at 1 A load)
- Low quiescent current (35  $\mu$ A typ. at no-load, 1  $\mu$ A max. in off mode)
- Output voltage tolerance:  $\pm 2.0\%$  at 25  $^{\circ}$ C
- 1.2 A guaranteed output current
- Wide range of output voltages available on request: 0.8 V to 5 V with 50 mV step and adjustable
- Logic-controlled electronic shutdown
- Compatible with ceramic capacitor  $C_{OUT} = 1 \mu$ F
- Internal current and thermal limit
- Available in DFN6 (2x2), DFN6 (3x3) mm, SO8-batwing and PPAK packages
- Temperature range: -40  $^{\circ}$ C to 125  $^{\circ}$ C
- Reverse current protection
- Output discharge function (optional)

### Applications

- Consumer
- Computer
- Battery-powered systems
- Low voltage point-of-load
- USB-powered devices

### Description

The LDL112 is a low-dropout linear regulator, which can provide a maximum current of 1.2 A, with a typical dropout voltage of 300 mV.

It is stabilized with a ceramic capacitor on the output.

The very low drop voltage, low quiescent current and reverse current protection features make it suitable for low power battery-powered applications.

The enable logic control function puts the LDL112 in shutdown mode allowing a total current consumption lower than 1  $\mu$ A.

The device is equipped with current limit and thermal protection.

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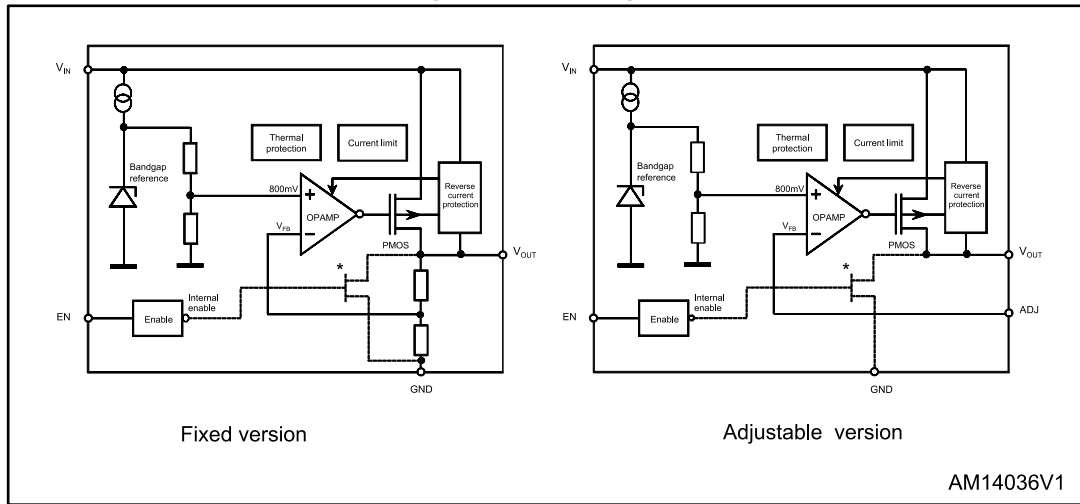
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# 1 Diagram

Figure 1: Block diagram



(\*) The output discharge function is optional.

## 2 Pin configuration

Figure 2: Pin connection DFN6 (3x3) and DFN6 (2x2) (top view)

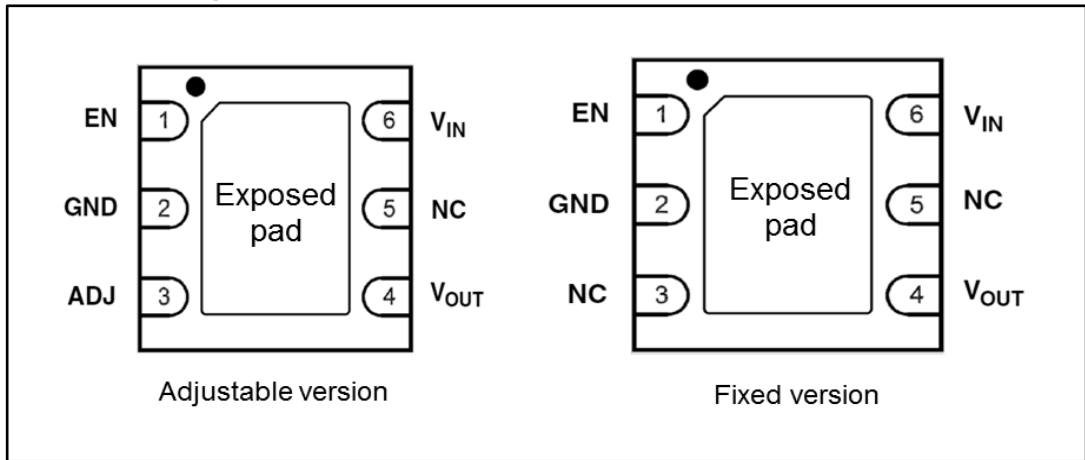
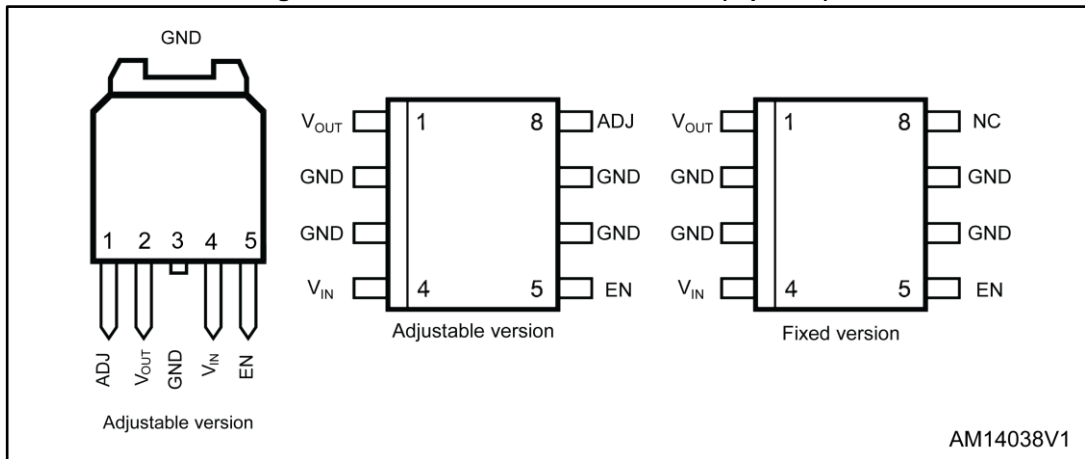


Figure 3: Pin connection PPAK and SO8 (top view)



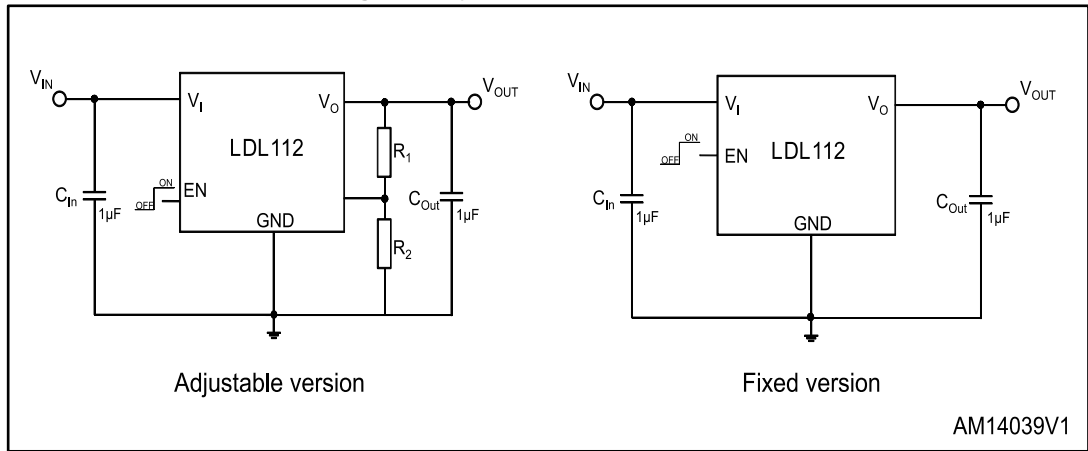
AM14038V1

Table 1: Pin description

Symbol	Function
V <sub>IN</sub>	LDO input voltage
GND	Common ground
EN	Enable pin logic input: low = shutdown, high = active
ADJ	Adjustable pin (on adjustable version)
V <sub>OUT</sub>	LDO output voltage
Exposed pad	Must be connected to GND
NC	Not connected

### 3 Typical application

Figure 4: Typical application circuits



## 4 Maximum ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V <sub>IN</sub>	DC input voltage	- 0.3 to 7	V
V <sub>OUT</sub>	DC output voltage	- 0.3 to V <sub>I</sub> + 0.3	V
V <sub>EN</sub>	Enable input voltage	- 0.3 to V <sub>I</sub> + 0.3	V
V <sub>ADJ</sub>	ADJ pin voltage	2	V
I <sub>OUT</sub>	Output current	Internally limited	mA
P <sub>D</sub>	Power dissipation	Internally limited	mW
T <sub>STG</sub>	Storage temperature range	- 65 to 150	°C
T <sub>OP</sub>	Operating junction temperature range	- 40 to 125	°C



Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. All values are referred to GND.

Table 3: Thermal data

Symbol	Parameter	DFN6 (3x3)	DFN6 (2x2)	SO8	PPAK	Unit
R <sub>thJA</sub>	Thermal resistance junction-ambient	55	65	55 <sup>(1)</sup>	100	°C/W
R <sub>thJC</sub>	Thermal resistance junction-case	10	15	20	8	°C/W

**Notes:**

<sup>(1)</sup>Considering 6 cm<sup>2</sup> of copper board heatsink.

## 5 Electrical characteristics

$T_J = 25\text{ °C}$ ,  $V_{IN} = V_{OUT(NOM)} + 0.5\text{ V}$  (for  $V_{OUT(NOM)} \leq 1\text{ V}$ ,  $V_{IN} = 2.1\text{ V}$ ),  $C_{IN} = C_{OUT} = 1\text{ }\mu\text{F}$ ,  
 $I_{OUT} = 5\text{ mA}$ ,  $V_{EN} = V_{IN}$ , unless otherwise specified.

**Table 4: LDL112 electrical characteristics (fixed version)**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{IN}$	Operating input voltage		1.6		5.5	V
$V_{OUT}$	$V_{OUT}$ accuracy	$I_{OUT} = 5\text{ mA}$ , $T_J = 25\text{ °C}$	-2.0		2.0	%
		$I_{OUT} = 5\text{ mA}$ , $-40\text{ °C} < T_J < 125\text{ °C}$	-3.0		3.0	%
$\Delta V_{OUT}$	Static line regulation <sup>(1)</sup>	$V_{OUT(NOM)} + 0.5\text{ V} < V_{IN} \leq 5.5\text{ V}$ <sup>(2)</sup>		0.05	0.1	%/V
$\Delta V_{OUT}$	Static load regulation	$I_{OUT} = 0\text{ mA}$ to $1.2\text{ A}$ , $V_{IN} > 2.1\text{ V}$		15	30	mV
$V_{DROP}$	Dropout voltage <sup>(3)</sup>	$I_{OUT} = 1\text{ A}$ , $V_{OUT} = 3.3\text{ V}$		300		mV
		$I_{OUT} = 1.2\text{ A}$ , $V_{OUT} = 3.3\text{ V}$ $40\text{ °C} < T_J < 125\text{ °C}$		350	600	
$e_N$	Output noise voltage	10 Hz to 100 kHz, $I_{OUT} = 10\text{ mA}$		135		$\mu\text{V}_{RMS}$
SVR	Supply voltage rejection	$V_{IN} = V_{OUT(NOM)} + 0.5\text{ V}$ <sup>(2)</sup> +/- $V_{RIPPLE}$ $V_{RIPPLE} = 0.2\text{ V}$ frequency = 1 kHz, $I_{OUT} = 10\text{ mA}$		57		dB
$I_Q$	Quiescent current	$I_{OUT} = 0\text{ mA}$ , $-40\text{ °C} < T_J < 125\text{ °C}$		35	70	$\mu\text{A}$
		$I_{OUT} = 1.2\text{ A}$ , $V_{OUT(NOM)} + 1\text{ V}$ <sup>(2)</sup> $40\text{ °C} < T_J < 125\text{ °C}$		250	400	
		$V_{IN}$ input current in off mode: $V_{EN} = \text{GND}$		0.1	1	
$I_{SC}$	Short-circuit current	$R_L = 0$ , $V_{IN} > 2.1\text{ V}$	1.4	2		A
$V_{EN}$	Enable input logic low	$V_{IN} = V_{OUT(NOM)} + 0.5\text{ V}$ <sup>(2)</sup> to $5.5\text{ V}$ , $-40\text{ °C} < T_J < 125\text{ °C}$			0.35	V
	Enable input logic high	$V_{IN} = V_{OUT(NOM)} + 0.5\text{ V}$ <sup>(2)</sup> to $5.5\text{ V}$ $-40\text{ °C} < T_J < 125\text{ °C}$	1.4			
$I_{EN}$	Enable pin input current	$V_{EN} = V_{IN}$			100	nA
$T_{SHDN}$	Thermal shutdown			165		°C
	Hysteresis			20		
$C_{OUT}$	Output capacitor	Capacitance (see <a href="#">Section 7: "Typical performance characteristics"</a> )	1		10	$\mu\text{F}$

**Notes:**

<sup>(1)</sup>Not applicable for  $V_{out(nom)} > 4.5\text{ V}$ .

<sup>(2)</sup>For  $V_{OUTNOM}$  lower than or equal to  $1\text{ V}$ ,  $V_{IN} = 2.1\text{ V}$ .

<sup>(3)</sup>Dropout voltage is the input-to-output voltage difference at which the output voltage is 100 mV below its nominal value.

$T_J = 25\text{ °C}$ ,  $V_{IN} = 2.1\text{ V}$ ,  $C_{IN} = C_{OUT} = 1\text{ }\mu\text{F}$ ,  $I_{OUT} = 5\text{ mA}$ ,  $V_{EN} = V_{IN}$ , unless otherwise specified.

Table 5: LDL112 electrical characteristics (adjustable version)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{IN}$	Operating input voltage		1.6		5.5	V
$V_{ADJ}$	$V_{ADJ}$ accuracy	$I_{OUT} = 5\text{ mA}$ , $T_J = 25\text{ °C}$	784	800	816	mV
		$I_{OUT} = 5\text{ mA}$ , $-40\text{ °C} < T_J < 125\text{ °C}$	-3.0		3.0	%
$\Delta V_{OUT}$	Static line regulation <sup>(1)</sup>	$2.1\text{ V}^{(2)} \leq V_{IN} \leq 5.5\text{ V}$ , $I_{OUT} = 1\text{ mA}$		0.05	0.1	%/V
$\Delta V_{OUT}$	Static load regulation	$I_{OUT} = 0\text{ mA}$ to $1.2\text{ A}$ , $V_{IN} > 2.1\text{ V}$		6	20	mV
$V_{DROP}$	Dropout voltage <sup>(3)</sup>	$I_{OUT} = 1\text{ A}$ , $V_{OUT} = 3.3\text{ V}$		300		mV
		$I_{OUT} = 1.2\text{ A}$ , $V_{OUT} = 3.3\text{ V}$ $40\text{ °C} < T_J < 125\text{ °C}$		350	600	
$e_N$	Output noise voltage	10 Hz to 100 kHz, $I_{OUT} = 10\text{ mA}$		60		$\mu\text{V}_{RMS}$
$I_{ADJ}$	Adjust pin current			0.130	1	$\mu\text{A}$
SVR	Supply voltage rejection	$V_{IN} = V_{OUTNOM} + 0.5\text{ V}^{(2)}$ +/- $V_{RIPPLE}$ $V_{RIPPLE} = 0.2\text{ V}$ frequency = 1 kHz $I_{OUT} = 10\text{ mA}$		53		dB
$I_Q$	Quiescent current	$I_{OUT} = 0\text{ mA}$ , $-40\text{ °C} < T_J < 125\text{ °C}$		35	70	$\mu\text{A}$
		$I_{OUT} = 1.2\text{ A}$ , $2.1\text{ V} < V_{IN} < 5.5\text{ V}$ , $-40\text{ °C} < T_J < 125\text{ °C}$		240	400	
		$V_{IN}$ input current in off mode: $V_{EN} = \text{GND}$		0.1	1	
$I_{SC}$	Short-circuit current	$R_L = 0$ , $V_{IN} > 2.1\text{ V}$	1.4	2		A
$V_{EN}$	Enable input logic low	$V_{IN} = 2\text{ V}^{(2)}$ to $5.5\text{ V}$ , $-40\text{ °C} < T_J < 125\text{ °C}$		0	0.35	V
	Enable input logic high	$V_{IN} = 2\text{ V}^{(2)}$ to $5.5\text{ V}$ , $-40\text{ °C} < T_J < 125\text{ °C}$	1.4			
$I_{EN}$	Enable pin input current	$V_{EN} = V_{IN}$			100	nA
$T_{SHDN}$	Thermal shutdown			165		$^{\circ}\text{C}$
	Hysteresis			20		
$C_{OUT}$	Output capacitor	Capacitance (see <a href="#">Section 7: "Typical performance characteristics"</a> )	1		10	$\mu\text{F}$

**Notes:**

<sup>(1)</sup>Not applicable for  $V_{out(nom)} > 4.5\text{ V}$ .

<sup>(2)</sup>For  $V_{OUT}$  lower than or equal to  $1\text{ V}$ ,  $V_{IN} = 2.1\text{ V}$ .

<sup>(3)</sup>Dropout voltage is the input-to-output voltage difference at which the output voltage is  $100\text{ mV}$  below its nominal value.



## 6 Application information

### 6.1 Thermal and short-circuit protections

The LDL112 is self-protected from short-circuit condition and overtemperature. When the output load is higher than the one supported by the device, the output current increases until the limit of typically 2 A is reached, at this point the current is kept constant even when the load impedance is zero.

Thermal protection acts when the junction temperature reaches 165 °C, therefore the IC shuts down. As soon as the junction temperature falls again below the thermal hysteresis value the device starts working again.

In order to calculate the maximum power that the device can dissipate, keeping the junction temperature below the  $T_{OP}$ , the following formula is used:

#### Equation 1

$$P_{DMAX} = (125 - T_{AMB}) / R_{THJA}$$

### 6.2 Output voltage setting for ADJ version

In the adjustable version, the output voltage can be set from 0.8 V up to the input voltage minus the voltage drop across the pass transistor (dropout voltage), by connecting a resistor divider between the ADJ pin and the output, thus allowing remote voltage sensing.

The resistor divider could be selected by the following equation:

#### Equation 2

$$V_{OUT} = V_{ADJ} (1 + R1 / R2), \text{ with } V_{ADJ} = 0.8 \text{ V (typ.)}$$

It is recommended to use resistors with values in the range of 10 kΩ to 50 kΩ. Lower values can also be suitable, but current consumption increases.

### 6.3 Reverse current protection

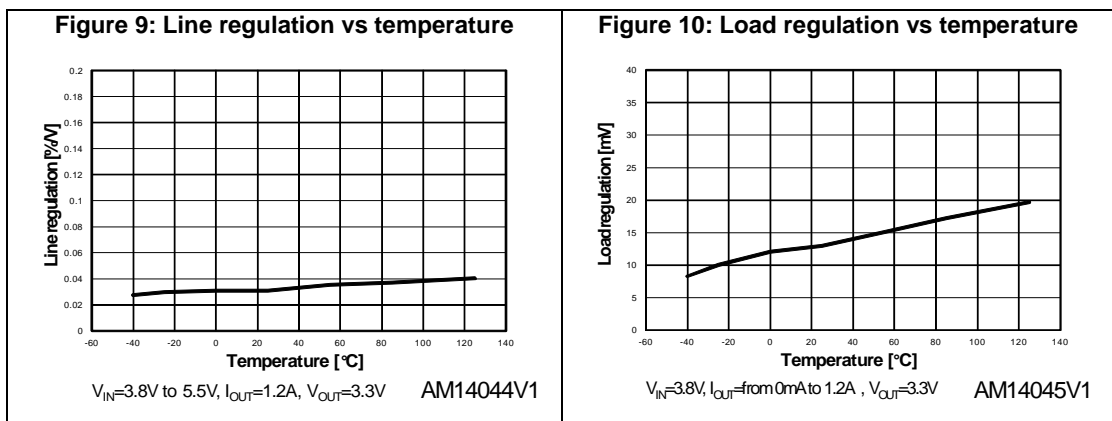
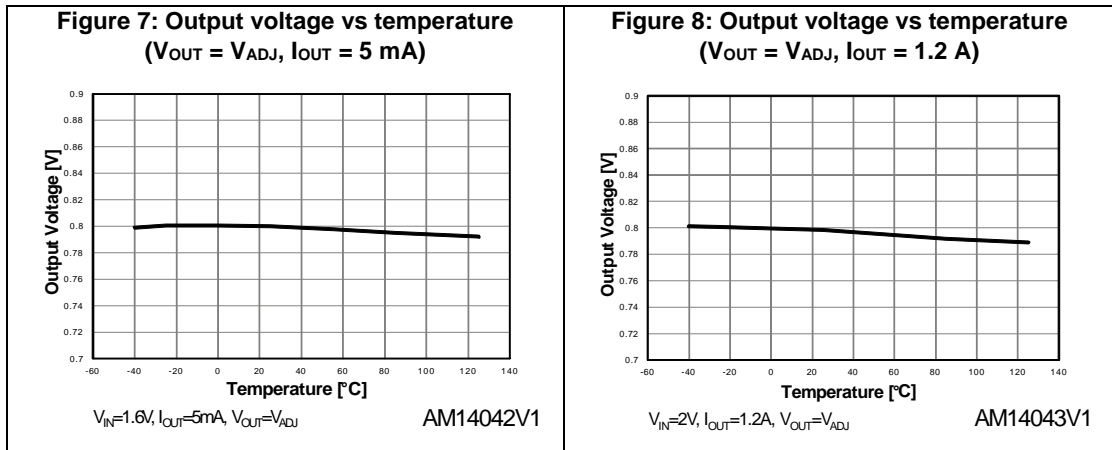
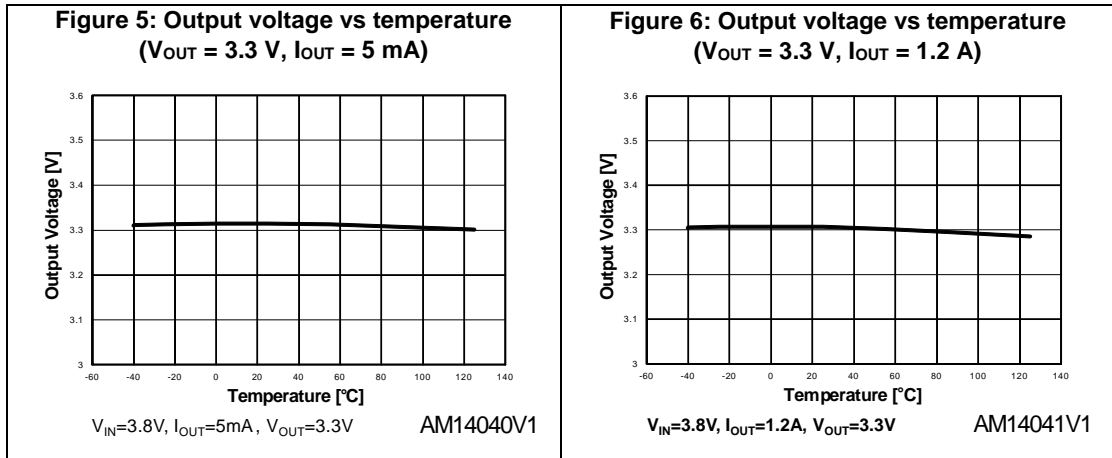
The device avoids the reverse current to flow from output to input during any operating condition (with enable pin in high or low status). The reverse current protection acts in particular during fast turning on/off operations or when another power supply (with higher voltage than the input one) is connected to the output port. If a power supply with lower voltage than the LDO output voltage is connected to  $V_{OUT}$  pin, LDO enters the current protection status, causing high power dissipation.

In the application, the LDL112 reverse current protection acts in the following cases:

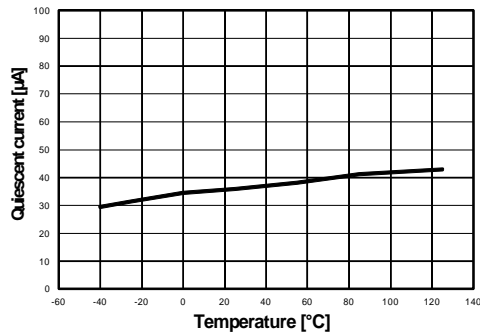
1. **Off-state, EN pin is at GND level,  $V_{OUT} > [V_{IN} + 100 \text{ mV}]$ .** In this case the device power pass element (MOSFET) is off, the bulk and gate are switched to  $V_{OUT}$  and therefore all possible current paths from  $V_{OUT}$  to  $V_{IN}$  are interrupted.
2. **On-state, EN pin is at high level and  $V_{OUT} > V_{OUT(nominal)}$ .** In this condition,  $V_{OUT}$  is higher than the nominal level, so the device op-amp works in open loop and the power element is off.  $V_{GS}$  is zero, the bulk and gate are switched to  $V_{OUT}$  (where  $V_{OUT} > [V_{IN} + 100 \text{ mV}]$ ) therefore all possible current paths from  $V_{OUT}$  to  $V_{IN}$  are interrupted.
3. **On-state, EN pin is at high level and  $V_{OUT} < V_{OUT(nominal)}$ .** In this condition  $V_{OUT}$  is lower than the nominal level, so the op-amp works in open loop with the power MOSFET on.  $V_{GS}$  is maximal so the power channel conducts with very low  $R_{DS(on)}$ . When  $V_{OUT} > V_{IN}$  the current can flow from  $V_{OUT}$  to  $V_{IN}$  until the condition  $V_{OUT} > (V_{IN} + 100 \text{ mV})$  is reached.

# 7 Typical performance characteristics

( $C_{IN} = C_{OUT} = 1 \mu F$ ,  $V_{EN}$  to  $V_{IN}$ ,  $T = 25 \text{ }^\circ\text{C}$  unless otherwise specified)

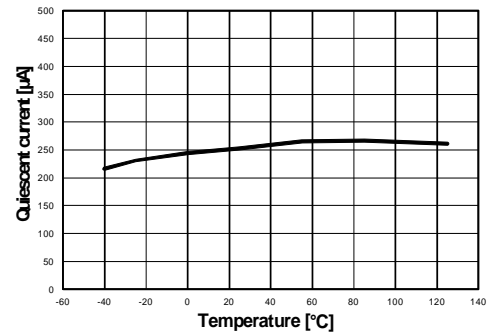


**Figure 11: Quiescent current vs temperature**  
( $I_{OUT} = 0 \text{ mA}$ )



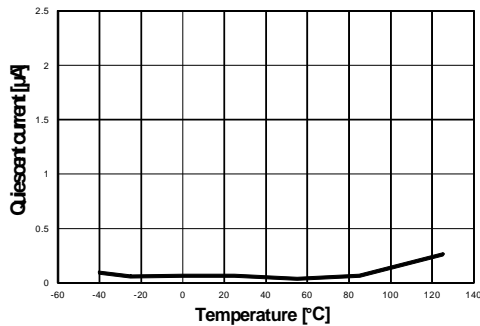
$V_{IN}=3.8\text{V}$ ,  $I_{OUT}=0\text{mA}$ ,  $V_{OUT}=3.3\text{V}$  AM14046V1

**Figure 12: Quiescent current vs temperature**  
( $I_{OUT} = 1.2 \text{ A}$ )



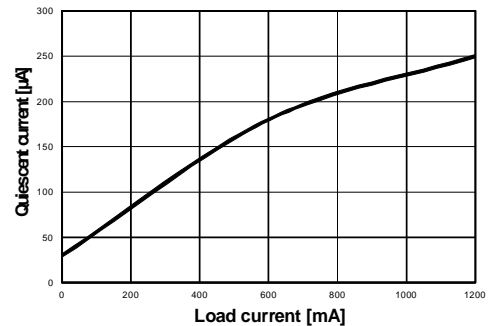
$V_{IN}=3.8\text{V}$ ,  $I_{OUT}=1.2\text{A}$ ,  $V_{OUT}=3.3\text{V}$  AM14047V1

**Figure 13: Shutdown current vs temperature**



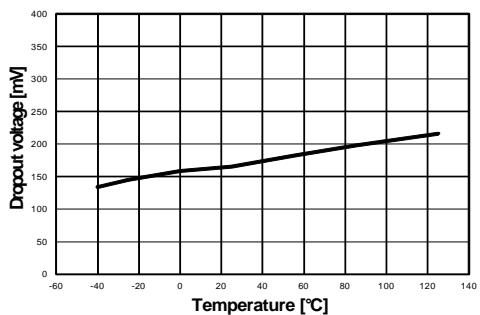
$V_{IN}=2\text{V}$ ,  $V_{EN}=\text{GND}$ ,  $V_{OUT}=V_{ADJ}$  AM14048V1

**Figure 14: Quiescent current vs load current**



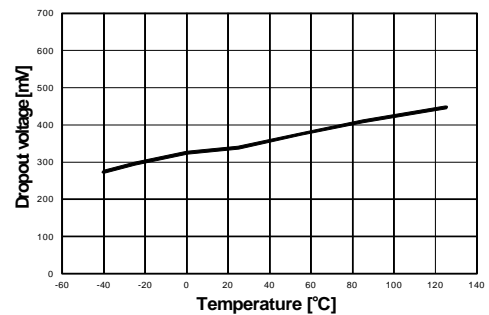
$V_{IN}=2\text{V}$ ,  $V_{OUT}=V_{ADJ}$ ,  $T=25^\circ\text{C}$  AM14049V1

**Figure 15: Dropout voltage vs temperature**  
( $I_{OUT} = 600 \text{ mA}$ )



$I_{OUT}=0.6\text{A}$ ,  $V_{OUT}=3.3\text{V}$  AM14050V1

**Figure 16: Dropout voltage vs temperature**  
( $I_{OUT} = 1.2 \text{ A}$ )



$I_{OUT}=1.2\text{A}$ ,  $V_{OUT}=3.3\text{V}$  AM14051V1

Figure 17: Dropout voltage vs load current

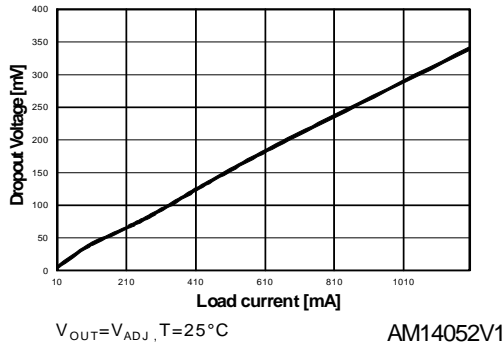


Figure 18: Short-circuit current vs input voltage

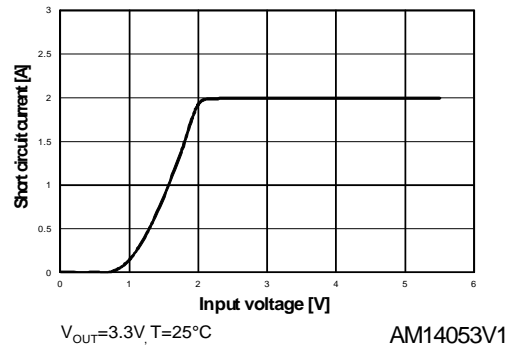


Figure 19: Enable thresholds vs temperature

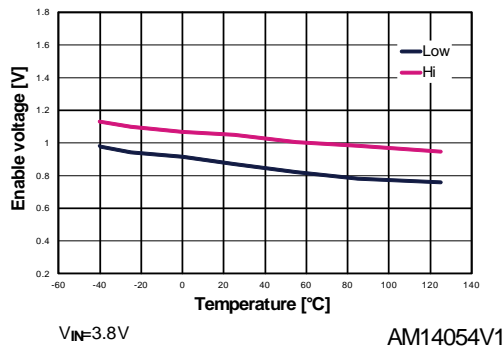


Figure 20: SVR vs frequency

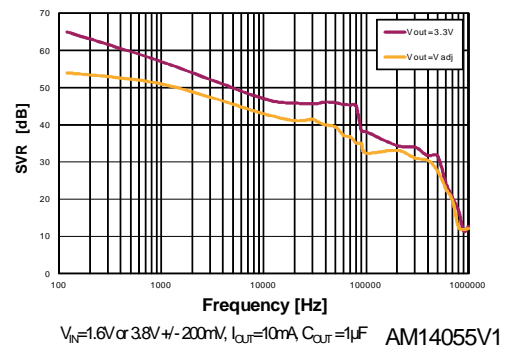


Figure 21: Output noise spectral density

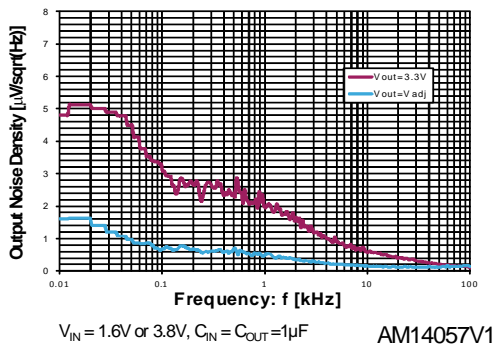


Figure 22: Stability plan vs C<sub>out</sub>, ESR

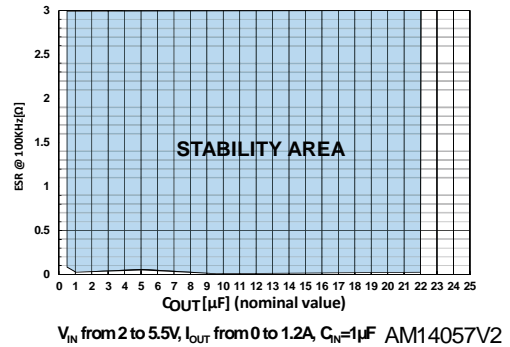
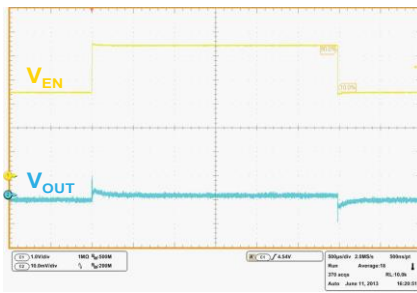
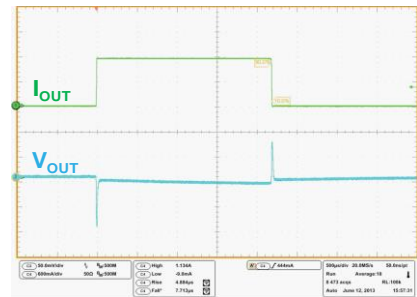


Figure 23: Line transient



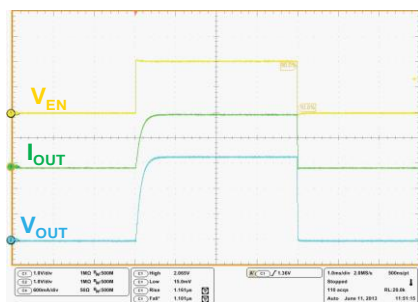
$V_{IN}$ =from 3.5V to 5.5V,  $V_{EN}$ =2V,  $I_{OUT}$ =10mA,  $V_{OUT}$ =3.3V,  $C_{OUT}$ =1 $\mu$ F,  $t_r$ =1 $\mu$ s  
AM14058V1

Figure 24: Load transient



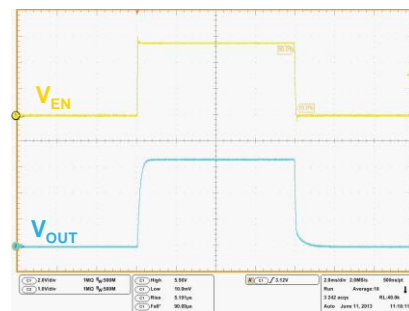
$V_{IN}$ = $V_{EN}$ =4V,  $I_{OUT}$ =from 5mA to 1.2A,  $V_{OUT}$ =3.3V,  $t_r$ =5 $\mu$ s  
AM14059V1

Figure 25: Enable transient



$V_{IN}$ =4V,  $V_{EN}$ =0V to 2V,  $I_{OUT}$ =1.2A,  $V_{OUT}$ =3.3V,  $t_r$ =1 $\mu$ s  
AM14060V1

Figure 26: Turn-on time



$V_{IN}$ = $V_{EN}$ =from 0V to 5.5V,  $I_{OUT}$ =5mA,  $V_{OUT}$ =3.3V,  $t_r$ =5 $\mu$ s  
AM14061V1

## 8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

### 8.1 DFN6 (3x3) package information

Figure 27: DFN6 (3x3) package outline

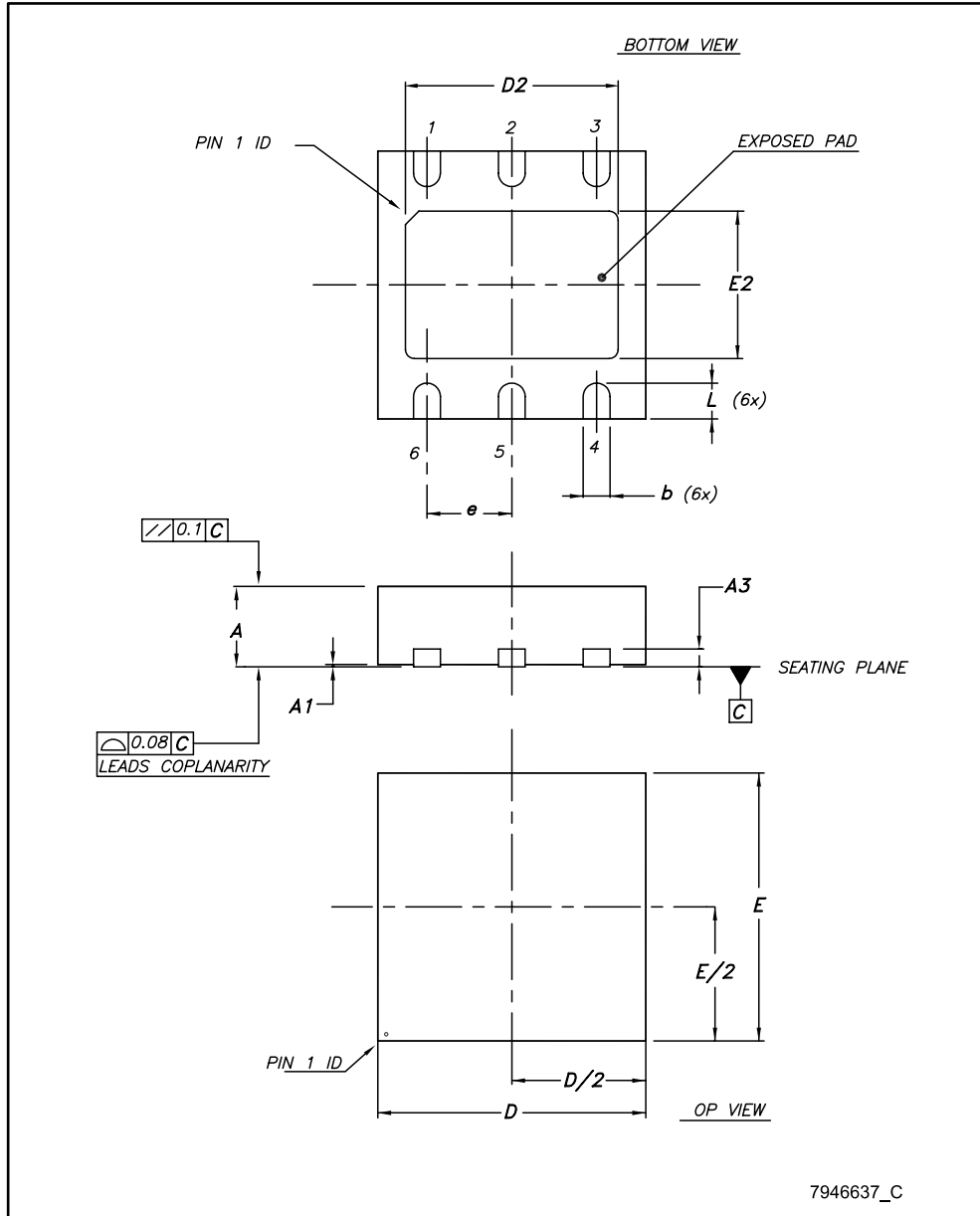
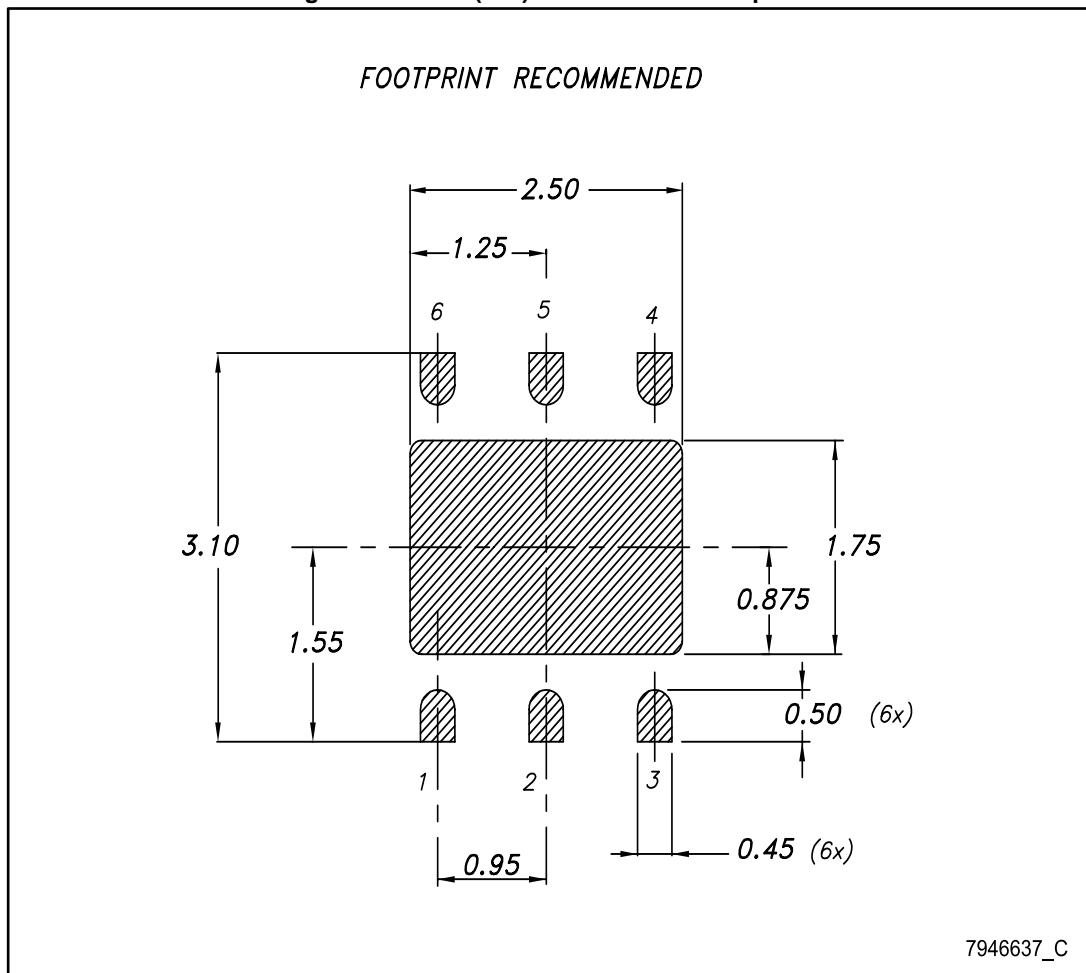


Table 6: DFN6 (3x3) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1
A1	0	0.02	0.05
A3		0.20	
b	0.23		0.45
D	2.90	3	3.10
D2	2.23		2.50
E	2.90	3	3.10
E2	1.50		1.75
e		0.95	
L	0.30	0.40	0.50

Figure 28: DFN6 (3x3) recommended footprint





## 8.2 DFN6 (3x3) packing information

Figure 29: DFN6 (3x3) tape outline

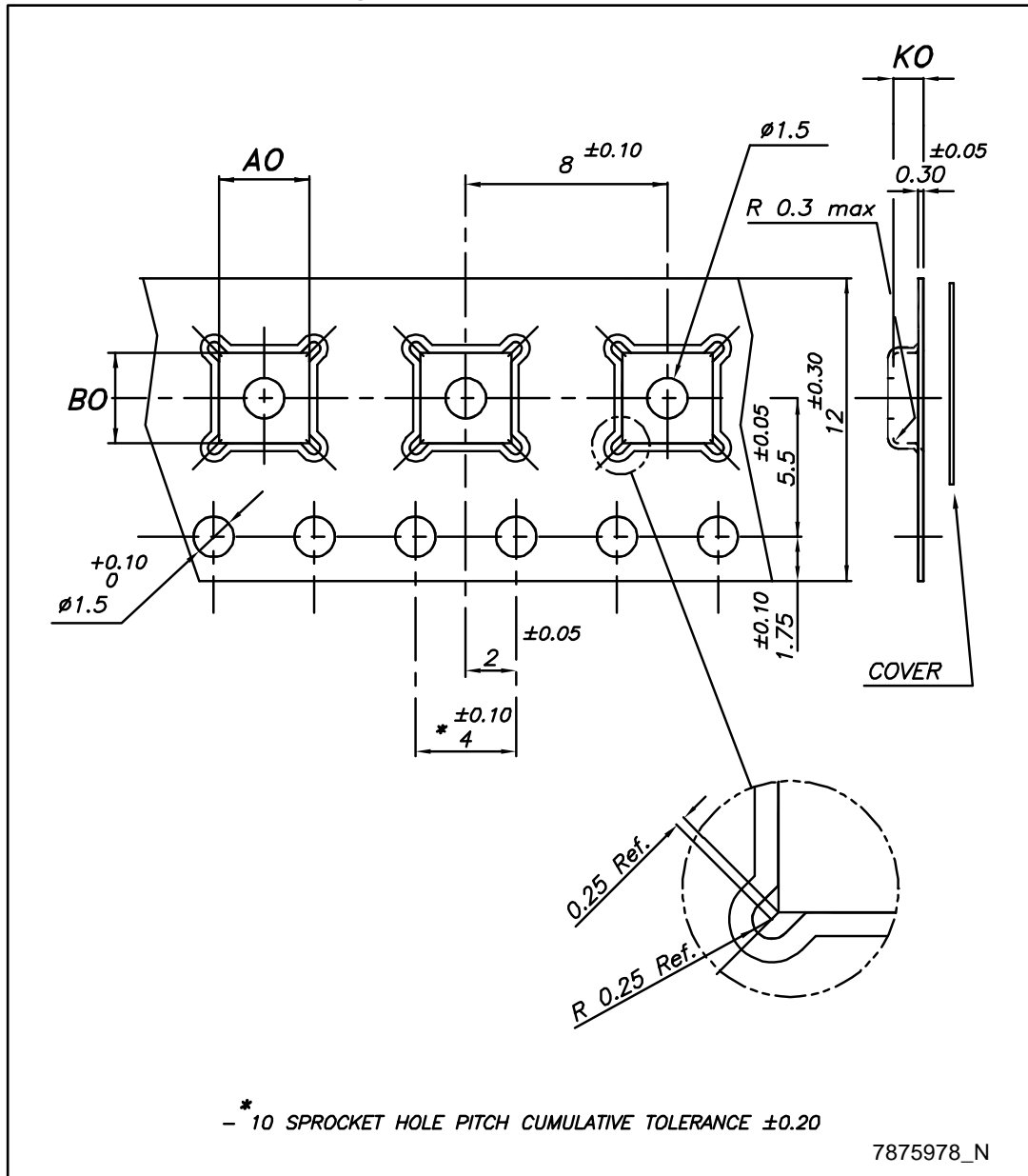
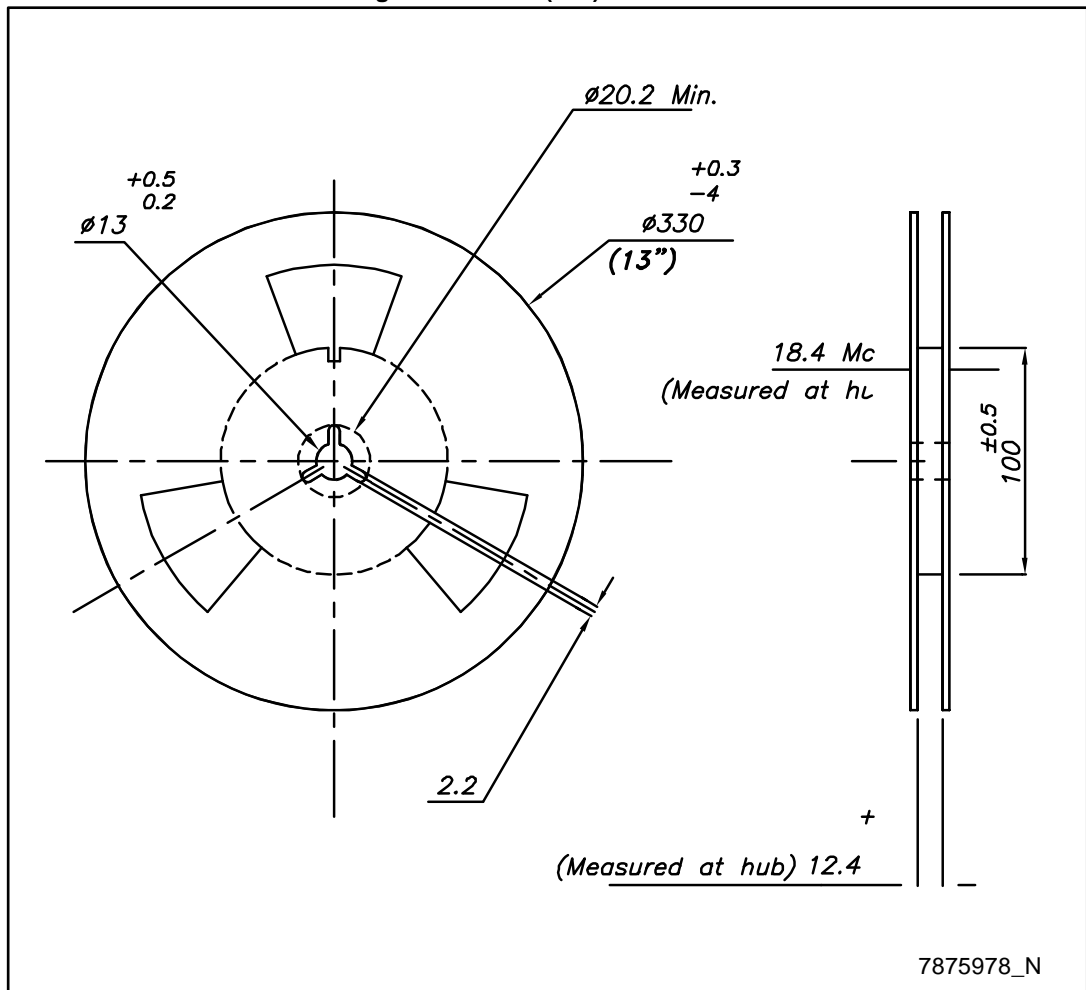


Figure 30: DFN6 (3x3) reel outline



7875978\_N

Table 7: DFN6 (3x3) tape and reel mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A0	3.20	3.30	3.40
B0	3.20	3.30	3.40
K0	1	1.10	1.20

### 8.3 DFN6 (2x2) package information

Figure 31: DFN6 (2x2) package outline

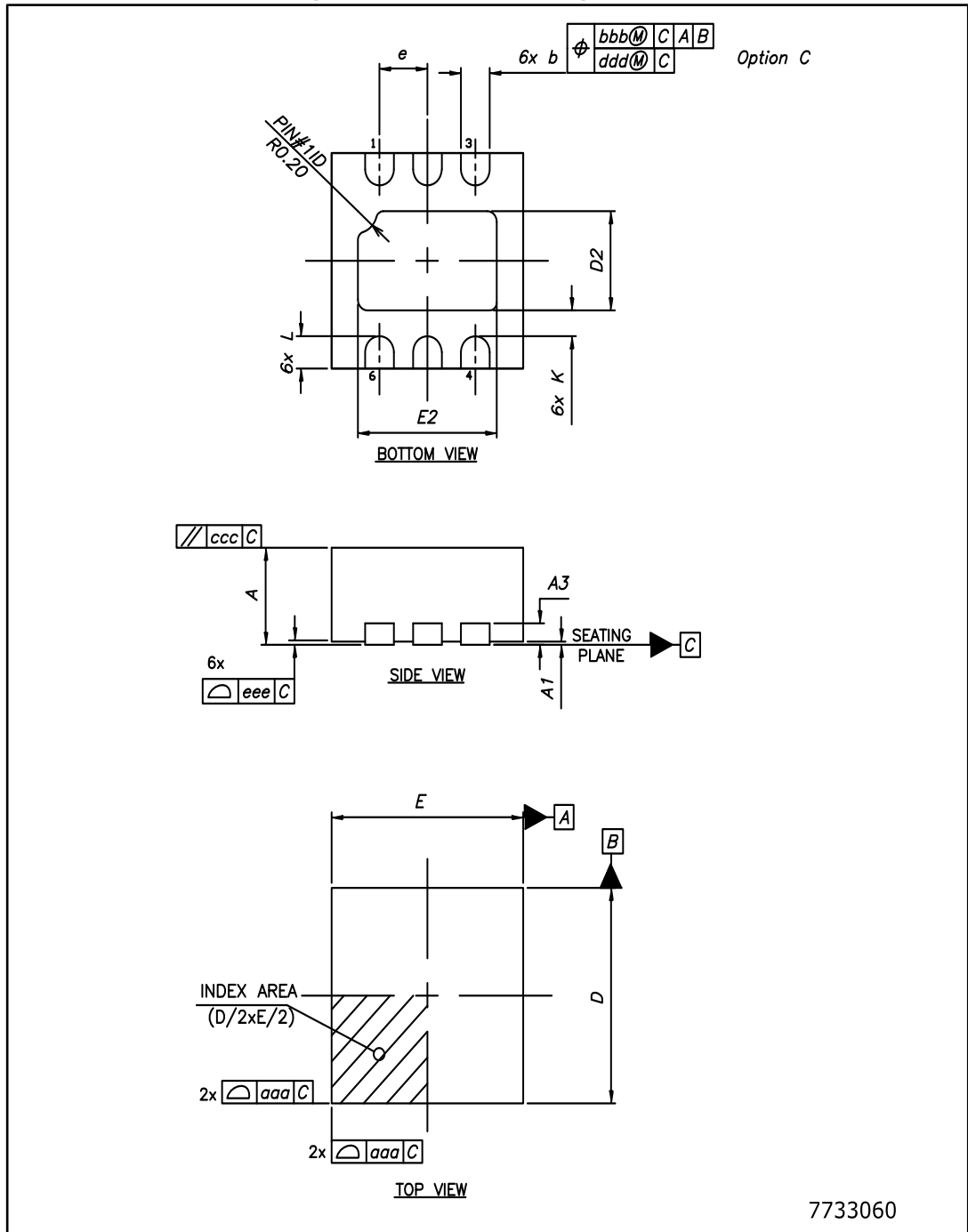
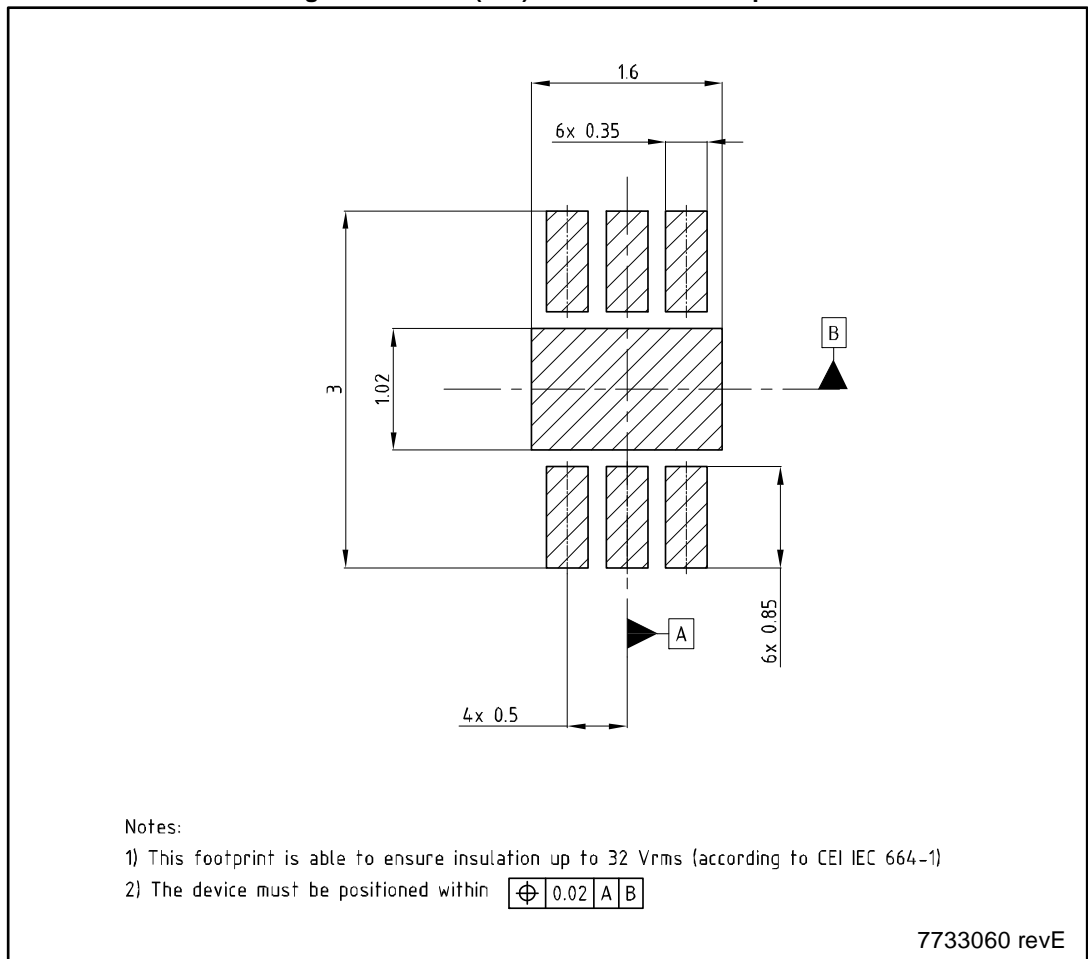


Table 8: DFN6 (2x2) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	-	0.203 ref	-
b	0.25	0.30	0.35
D	-	2.00	-
E	-	2.00	-
e	-	0.50	-
D2	0.77	0.92	1.02
E2	1.30	1.45	1.55
K	0.15	-	-
L	0.20	0.30	0.40
aaa	-	0.05	-
bbb	-	0.10	-
ccc	-	0.10	-
ddd	-	0.05	-
eee	-	0.08	-

Figure 32: DFN6 (2x2) recommended footprint



### 8.4 DFN6 (2x2) packing information

Figure 33: DFN6 (2x2) reel outline

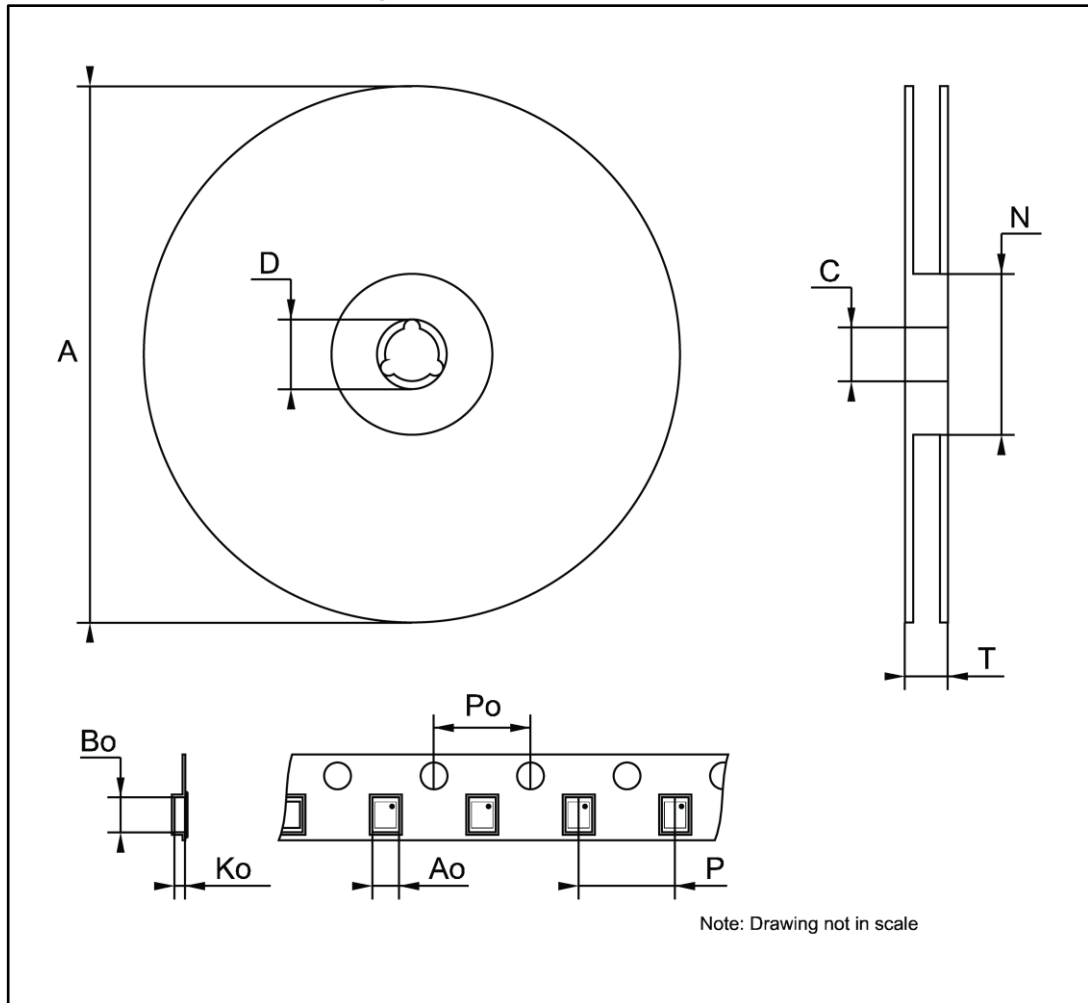


Table 9: DFN6 (2x2) tape and reel mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			180
C	12.8		13.2
D	20.2		
N	60		
T			14.4
A0		2.4	
B0		2.4	
K0		1.3	
P0		4	
P		4	

## 8.5 SO8-batwing package information

Figure 34: SO-8 batwing package outline

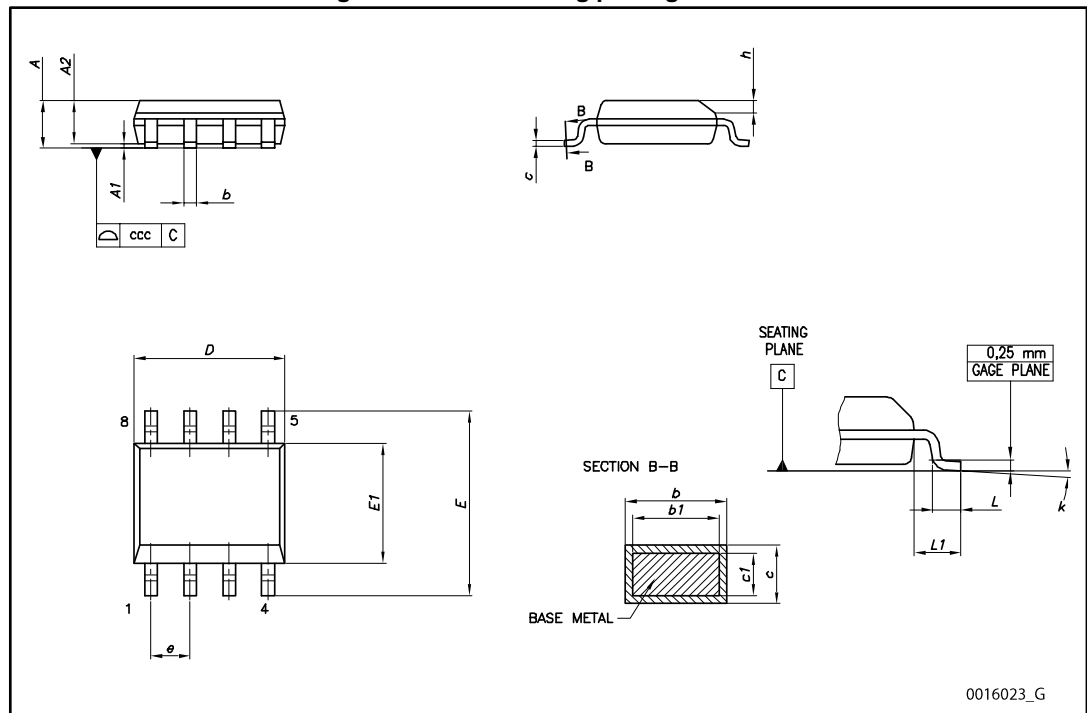
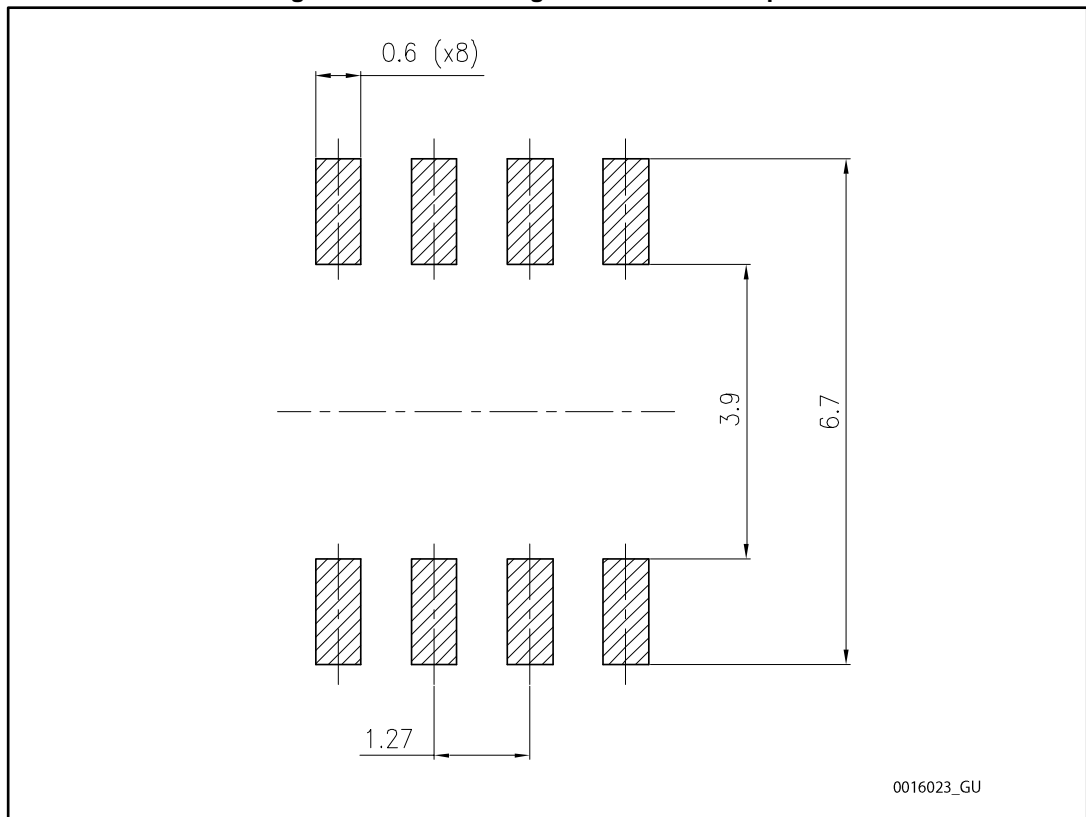


Table 10: SO-8 batwing mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			1.75
A1	0.10		0.25
A2	1.25		
b	0.31		0.51
b1	0.28		0.48
c	0.10		0.25
c1	0.10		0.23
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e		1.27	
h	0.25		0.50
L	0.40		1.27
L1		1.04	
L2		0.25	
k	0°		8°
ccc			0.10

Figure 35: SO-8 batwing recommended footprint





### 8.6 SO8-batwing packing information

Figure 36: SO8-batwing tape and reel outline

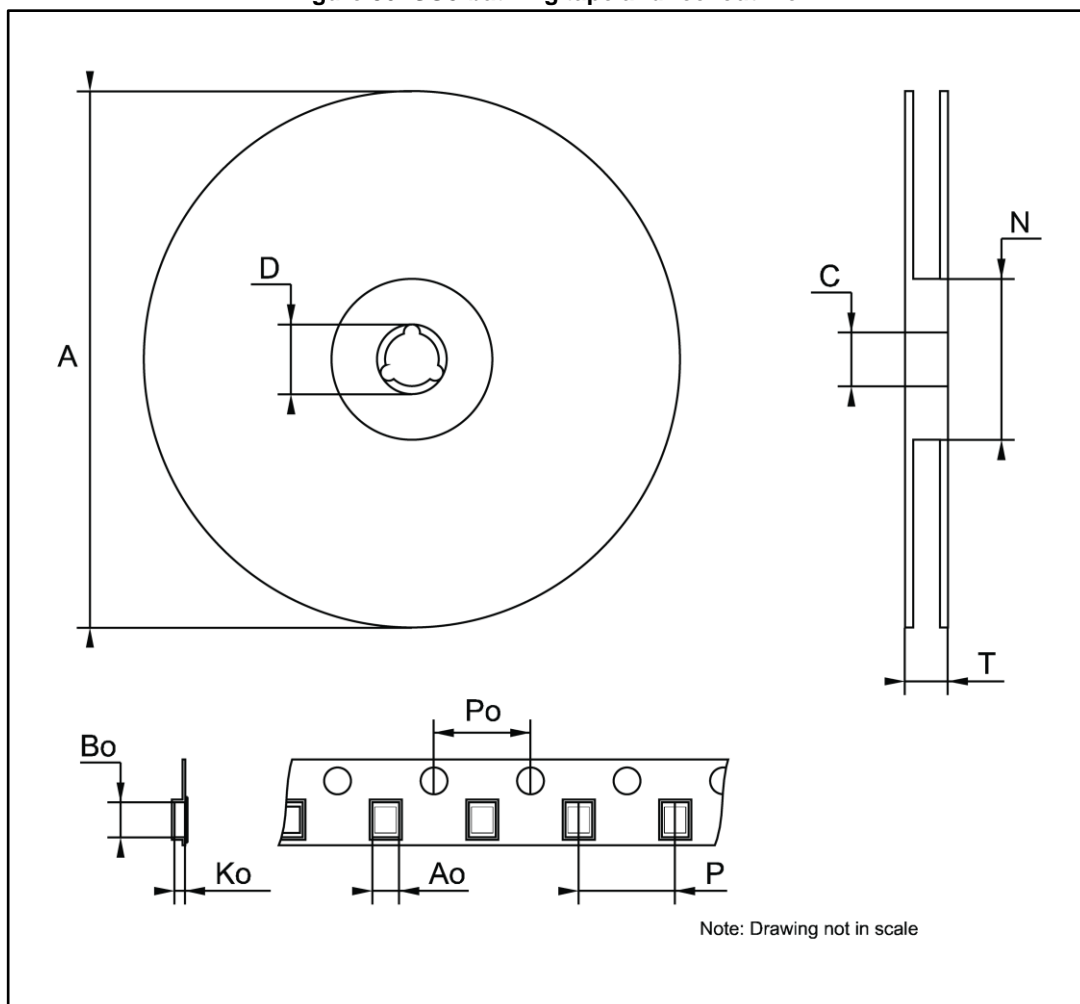
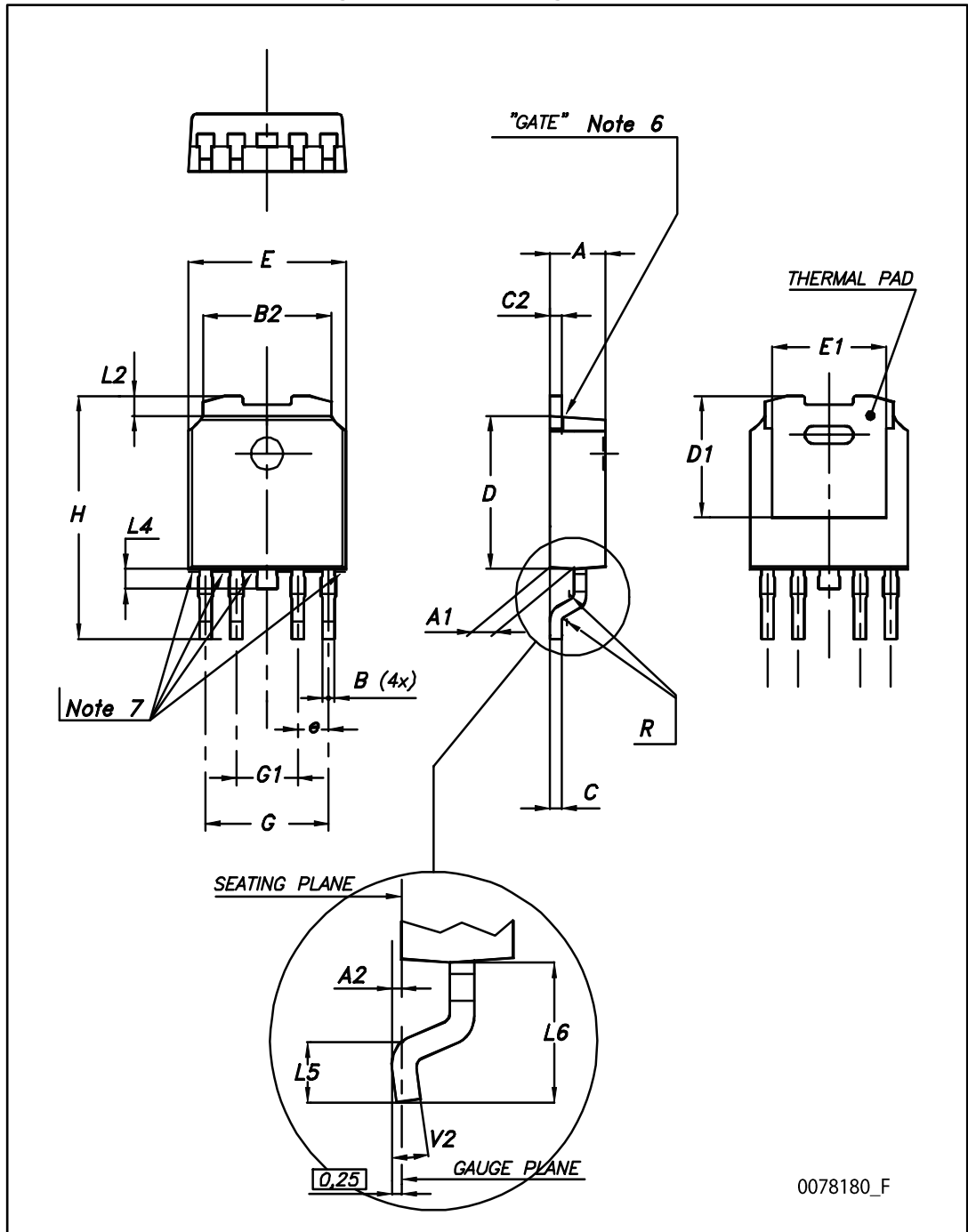


Table 11: SO8-batwing mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			330
C	12.8		13.2
D	20.2		
N	60		
T			22.4
A0	8.1		8.5
B0	5.5		5.9
K0	2.1		2.3
P0	3.9		4.1
P	7.9		8.1

### 8.7 PPAK package information

Figure 37: PPAK package outline



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Table 12: PPAK mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.2		2.4
A1	0.9		1.1
A2	0.03		0.23
B	0.4		0.6
B2	5.2		5.4
C	0.45		0.6
C2	0.48		0.6
D	6		6.2
D1		5.1	
E	6.4		6.6
E1		4.7	
e		1.27	
G	4.9		5.25
G1	2.38		2.7
H	9.35		10.1
L2		0.8	1
L4	0.6		1
L5	1		
L6		2.8	
R		0.20	
V2	0°		8°

### 8.8 PPAK packing information

Figure 38: PPAK tape outline

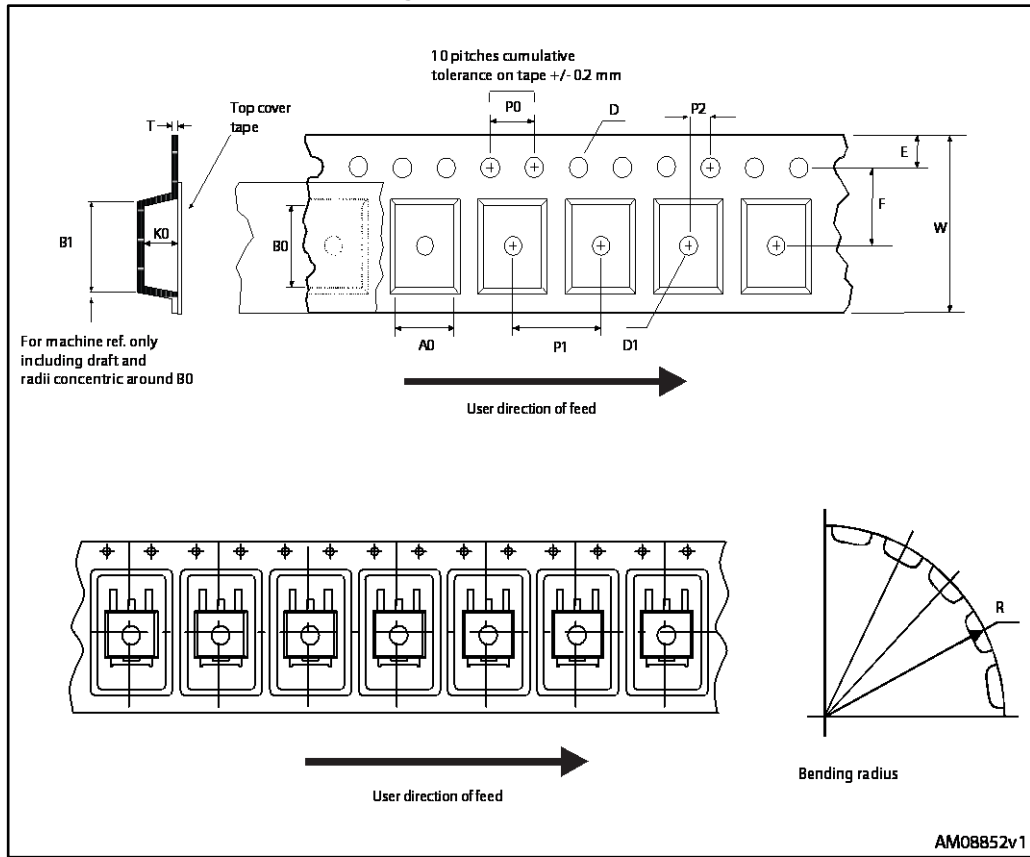


Figure 39: PPAK reel outline

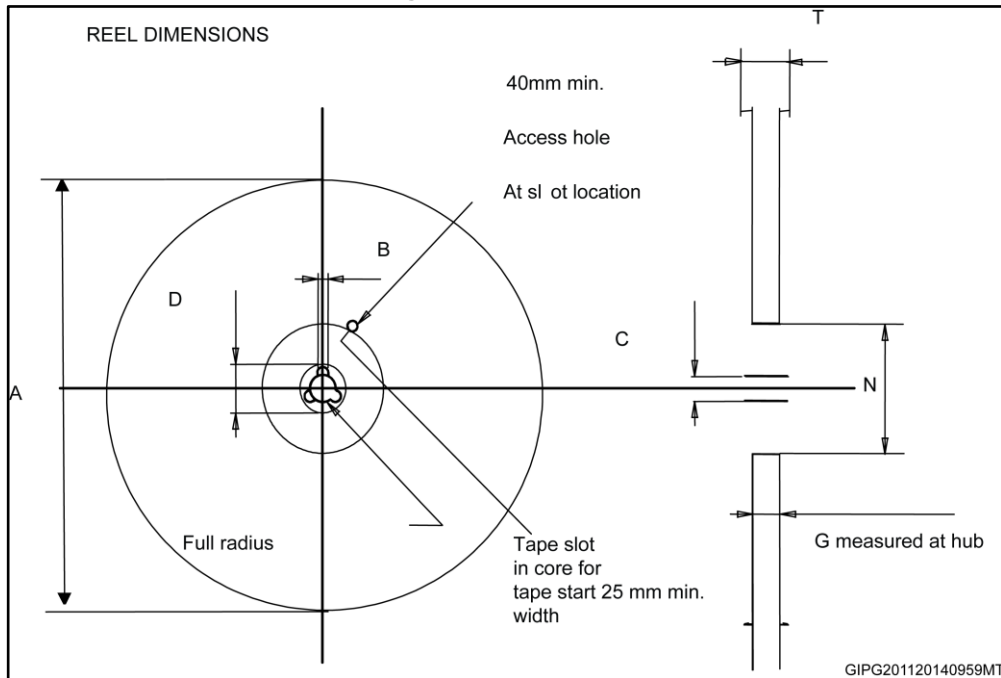


Table 13: PPAK mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Base qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

## 9 Ordering information

Table 14: Order codes

DFN6 (3x3)	DFN6 (2x2)	SO8-batwing	PPAK	Output voltage (V)
LDL112PV10R	LDL112PU10R	LDL112D10R		1.0
LDL112PV12R	LDL112PU12R	LDL112D12R		1.2
LDL112PV15R	LDL112PU15R	LDL112D15R		1.5
LDL112PV18R	LDL112PU18R	LDL112D18R		1.8
LDL112PV25R	LDL112PU25R	LDL112D25R		2.5
LDL112PV30R	LDL112PU30R	LDL112D30R		3.0
LDL112PV33R	LDL112PU33R	LDL112D33R		3.3
LDL112PVR	LDL112PUR	LDL112DR	LDL112PT-TR	Adj

## 10 Revision history

Table 15: Document revision history

Date	Revision	Changes
21-Nov-2014	1	Initial release.
28-Oct-2016	2	Updated <i>Figure 31: "DFN6 (2x2) package outline"</i> . Modified <i>Table 14: "Order codes"</i> . Minor text changes.

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