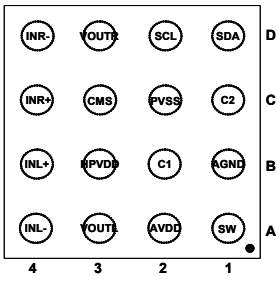
# A22H165M

# High-performance class-G stereo headphone amplifier with I²C volume control

**Datasheet - production data**

**A22H165M - Flip-chip**

**Pinout (top view)**




Balls are underneath

## Features

- Power supply range: 2.3 V to 4.8 V
- 0.6 mA/channel quiescent current
- 2.1 mA current consumption with 100 µW/channel (10 dB crest factor)
- 0.006% typical THD+N at 1 kHz
- 100 dB typical PSRR at 217 Hz
- 100 dB of SNR A-weighted at G = 0 dB
- Zero pop and click
- I²C interface for volume control
- Digital volume control range from -60 dB to +4 dB
- Independent right and left channel shutdown control
- Integrated high-efficiency buck converter
- Low software standby current: 5 µA max
- Output coupling capacitors removed
- Thermal shutdown and short-circuit protection
- Flip-chip package: 1.65 mm x 1.65 mm, 400 µm pitch, 16 bumps

## Applications

- Cellular /smart phones, portable media players
- Wearable
- Fitness and healthcare

## Description

The A22H165M is a class-G stereo headphone driver dedicated to high audio performance, high power efficiency and space-constrained applications such as wearable and fitness.

It is based on the core technology of a low power dissipation amplifier combined with a high efficiency buck converter for supplying this amplifier.

When powered by a battery, the buck converter generates the appropriate voltage to the amplifier depending on the amplitude of the audio signal to supply the headsets. It achieves a total 2.1 mA current consumption at 100 µW output power (10 dB crest factor).

THD+N is 0.02% maximum at 1 kHz and PSRR is 100 dB at 217 Hz, which ensures a high audio quality of the device in a wide range of environments.

The traditionally bulky output coupling capacitors can be removed.

A dedicated common-mode sense pin removes parasitic ground noise.

The A22H165M is designed to be used with an output serial resistor. It ensures unconditional stability over a wide range of capacitive loads. The A22H165M is packaged in a tiny 16-bump flip-chip package with a pitch of 400 µm.

# Contents

# 1 Absolute maximum ratings and operating conditions

**Table 1. Absolute maximum ratings**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{CC}$ | Supply voltage (1) during 1 ms. | 5.5 | V |
| $V_{in+}$,$V_{in-}$ | Input voltage referred to ground | +/- 1.2 | V |
| $T_{stg}$ | Storage temperature | -65 to +150 | °C |
| $T_j$ | Maximum junction temperature (2) | 150 | °C |
| $R_{thja}$ | Thermal resistance junction to ambient (3) | 200 | °C/W |
| $P_d$ | Power dissipation | Internally limited (4) | |
| ESD | Human body model (HBM)(5)<br>All pins<br>VOUTR, VOUTL vs. AGND | <br>2<br>4 | kV |
| | Machine model (MM), min. value (6) | 100 | V |
| | Charge device model (CDM)<br>All pins<br>VOUTR, VOUTL | <br>500<br>750 | V |
| | IEC61000-4-2 level 4, contact (7)<br>IEC61000-4-2 level 4, air discharge (7) | +/- 8<br>+/- 15 | kV |
| Latch-up | Latch-up immunity | 200 | mA |
| | Lead temperature (soldering, 10 sec) | 260 | °C |

1. All voltage values are measured with respect to the ground pin.
2. Thermal shutdown is activated when maximum junction temperature is reached.
3. The device is protected from over-temperature by a thermal shutdown mechanism, active at 150° C.
4. Exceeding the power derating curves for long periods may provoke abnormal operation.
5. Human body model: a 100 pF capacitor is charged to the specified voltage, then discharged through a 1.5 kΩ resistor between two pins of the device. This is done for all couples of connected pin combinations while the other pins are floating.
6. Machine model: a 200 pF capacitor is charged to the specified voltage, then discharged directly between two pins of the device with no external series resistor (internal resistor < 5 Ω). This is done for all couples of connected pin combinations while the other pins are floating.
7. The measurement is performed on an evaluation board, with ESD protection EMIF02-AV01F3.

**Table 2. Operating conditions**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{CC}$ | Supply voltage | 2.3 to 4.8 | V |
| HPVDD | Buck DC output voltages<br>High rail voltage<br>Low rail voltage | <br>1.9<br>1.2 | V |
| SDA, SCL | Input voltage range | GND to $V_{CC}$ | V |
| $R_L$ | Load resistor | ≥ 16 | Ω |
| $C_L$ | Load capacitor<br>Serial resistor of 12 Ω minimum, $R_L \geq 16$ Ω | <br>0.8 to 100 | nF |
| $T_{oper}$ | Operating free air temperature range | -40 to +85 | °C |
| $R_{thja}$ | Flip-chip thermal resistance junction to ambient | 90 | °C/W |

# 2 Typical application schematic

**Figure 1. Typical application schematic for the A22H165M**

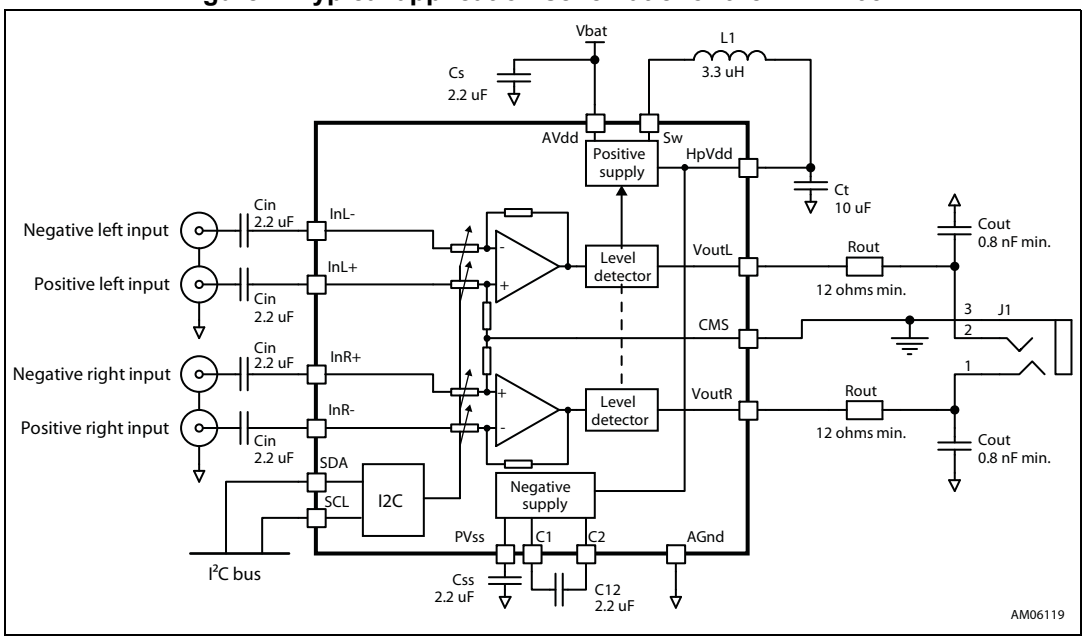



**Table 3. A22H165M pin description**

| Pin n° | Pin name | Pin definition |
|---|---|---|
| A1 | SW | Switching node of the buck converter |
| A2 | AVDD | Analog supply voltage, connect to battery |
| A3 | VOUTL | Output signal for left audio channel |
| A4 | INL- | Negative input signal for left audio channel |
| B1 | AGND | Device ground |
| B2 | C1 | Flying capacitor terminal for internal negative supply generator |
| B3 | HPVDD | Buck converter output, power supply for amplifier |
| B4 | INL+ | Positive input signal for left audio channel |
| C1 | C2 | Flying capacitor terminal for internal negative supply generator |
| C2 | PVSS | Negative supply generator output |
| C3 | CMS | Common mode sense, to be connected as close as possible to the ground of headphone/line out plug |
| C4 | INR+ | Positive input signal for right audio channel |
| D1 | SDA | I²C data signal, up to $V_{CC}$ tolerant input |
| D2 | SCL | I²C clock signal, up to $V_{CC}$ tolerant input |
| D3 | VOUTR | Output signal for right audio channel |
| D4 | INR- | Negative input signal for right audio channel |

**Table 4. A22H165M component description**

| Component | Value | Description |
|---|---|---|
| Cs | 2.2 µF | Decoupling capacitors for $V_{CC}$. A 2.2 µF capacitor is sufficient for proper decoupling of the A22H165M. An X5R dielectric and 10 V rating voltage is recommended to minimize $\Delta C/\Delta V$ when $V_{CC}$ = 4.8 V.<br>Must be placed as close as possible to the A22H165M to minimize parasitic inductance and resistance. |
| C12 | 2.2 µF | Capacitor for internal negative power supply operation. An X5R dielectric and 6.3 V rating voltage is recommended to minimize $\Delta C/\Delta V$ when HPVDD = 1.9 V.<br>Must be placed as close as possible to the A22H165M to minimize parasitic inductance and resistance. |
| $C_{SS}$ | 2.2 µF | Filtering capacitor for internal negative power supply. An X5R dielectric and 6.3 V rating voltage is recommended to minimize $\Delta C/\Delta V$ when HPVDD = 1.9 V. |
| $C_{in}$ | $Cin = \frac{1}{2\pi ZinFc}$ | Input coupling capacitor that forms with $Z_{in}/2$ a first-order high-pass filter with a -3 dB cutoff frequency FC. For example, at maximum gain G = 4 dB, $Z_{in}$ = 12.5 kΩ, $C_{in}$ = 2.2 µF, therefore FC = 6 Hz. |
| $C_{out}$ | 0.8 to 100 nF | Output capacitor of 0.8 nF minimum to 100 nF maximum. This capacitor is mandatory for operation of the A22H165M. |
| $R_{out}$ | 12 Ω min. | Output resistor in-series with the A22H165M output. This 12 Ω minimum resistor is mandatory for operation of the A22H165M. |
| L1 | 3.3 µH | Inductor for the buck converter.<br>References of inductors:<br>FDK: MIPSZ2012D3R3 (DC resistance = 0.19 Ω, rated current = 0.8 A)<br>Murata: LQM2MPN3R3G0 (DC resistance = 0.12 Ω, rated current = 1.2 A) |
| $C_t$ | 10 µF | Tank capacitor for internal buck converter. An X5R dielectric and 6.3 V rating voltage is recommended to minimize $\Delta C/\Delta V$ when HPVDD = 1.9 V.<br>ESR of the $C_t$ capacitor must be as low as possible to obtain the best buck efficiency. |

# 3 Electrical characteristics

$V_{CC}$ = +3.6 V, AGND = 0 V, $T_{amb}$ = 25 °C (unless otherwise specified)

**Table 5. Electrical characteristics of the I²C interface**

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{IL}$ | Low level input voltage on SDA, SCL pins | | | 0.6 | V |
| $V_{IH}$ | High level input voltage on SDA, SCL pins | 1.2 | | | V |
| $V_{OL}$ | Low level output voltage, SDA pin, $I_{sink}$ = 3 mA | | | 0.4 | V |
| $I_{in}$ | Input current on SDA, SCL | | $\frac{V_{SDA, SCL}}{600k\Omega}$ | 10 | µA |

$V_{CC}$ = +3.6 V, AGND = 0 V, $R_L$= 32 Ω + 15 Ω, $T_{amb}$ = 25° C (unless otherwise specified)

**Table 6. Electrical characteristics of the amplifier**

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $I_{CC}$ | Quiescent supply current, no input signal, both channels enabled | | 1.2 | 1.5 | mA |
| $I_s$ | Supply current, with input modulation, both channels enabled, HPVDD = 1.2 V, output power per channel, F=1kHz<br>Pout = 100 µW at 3 dB crest factor<br>Pout = 500 µW at 3 dB crest factor<br>Pout = 1 mW at 3 dB crest factor<br>Pout = 100 µW at 10 dB crest factor<br>Pout = 500 µW at 10 dB crest factor<br>Pout = 1 mW at 10 dB crest factor | | <br>2.3<br>3.7<br>4.7<br>2.1<br>3.1<br>3.9 | <br>3.5<br>5<br>6.5 | mA |
| $I_{STBY}$ | Standby current, no input signal, I²C CR1 = 01h<br>$V_{SDA}$ = 0 V, $V_{SCL}$ = 0 V | | 0.6 | 5 | µA |
| $V_{in}$ | Input differential voltage range(1) | | | 1 | $V_{rms}$ |
| $V_{oo}$ | Output offset voltage<br>No input signal | -500 | | +500 | µV |
| $V_{out}$ | Maximum output voltage, in-phase signals<br>$R_L$ = 16 Ω, THD+N = 1% max, f = 1 kHz<br>$R_L$ = 47 Ω, THD+N = 1% max, f = 1 kHz<br>$R_L$ = 10 kΩ, $P_s$ = 15 Ω, $X_L$ = 1 νΦ, THD+N = 1% max, f = 1 kHz | <br>0.6<br>1.0<br>1.0 | <br>0.8<br>1.1<br>1.3 | | $V_{rms}$ |
| THD+N | Total harmonic distortion + noise, G = 0 dB<br>$V_{out}$ = 700 mVrms, F = 1 kHz<br>$V_{out}$ = 700 mVrms, 20 Hz < F < 20 kHz | | <br>0.006<br>0.05 | <br>0.02 | % |

**Table 6. Electrical characteristics of the amplifier (continued)**

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| PSRR | Power supply rejection ratio(1), $V_{ripple}$ = 200 $mV_{pp}$, grounded inputs<br>F = 217 Hz, G = 0 dB, $R_L$ ≥16 Ω<br>F = 10 kHz, G = 0 dB, $R_L$ ≥16 Ω | <br>90 | <br>100<br>70 | | dB |
| CMRR | Common mode rejection ratio<br>F = 1 kHz, G = 0 dB, $V_{ic}$ = 200 $mV_{pp}$<br>F = 20 Hz to 20 kHz, G = 0 dB, $V_{ic}$ = 200 $mV_{pp}$ | | <br>65<br>45 | | dB |
| Crosstalk | Channel separation<br>$R_L$ = 32 Ω + 15 Ω , G = 0 dB, F = 1 kHz, $P_o$ = 10 mW<br>$R_L$ = 10 kΩ, G = 0 dB, F = 1 kHz, $V_{out}$ = 1 Vrms | <br>60<br>80 | <br>100<br>110 | | dB |
| SNR | Signal-to-noise ratio, A-weighted, $V_{out}$ = 1 $V_{rms}$, THD+N < 1%, F = 1 kHz(1)<br>G = +4 dB<br>G = +0 dB | <br>99<br>100 | | | dB |
| ONoise | Output noise voltage, A-weighted (1)<br>G = +4 dB<br>G = +0 dB | | <br>9 | <br>11<br>9 | µVrms |
| G | Gain range with gain (dB) = 20 x log[($V_{out}$L/R)/(InL/R+ - InL/R-)] | -60 | | +4 | dB |
| Mute | InL/R+ - InL/R- = 1 $V_{rms}$ | | | -80 | dB |
| - | Gain step size error | -0.5 | | +0.5 | step-size |
| - | Gain error (G = +4 dB) | -0.45 | | +0.42 | dB |
| $Z_{in}$ | Differential input impedance | 25 | 34 | | kΩ |
| | Input impedance during wake-up phase (referred to ground) | | 2 | | kΩ |
| $Z_{out}$ | Output impedance when CR1 = 00h (negative supply is ON and amplifier output stages are OFF)(1)<br>F < 40 kHz<br>F = 6 MHz<br>F = 36 MHz | <br>10<br>500<br>75 | | | <br>kΩ<br>Ω<br>Ω |
| $t_{wu}$ | Wake-up time(2) | | 12 | 16 | ms |
| $t_{stby}$ | Standby time | | 100 | | µs |
| $t_{atk}$ | Attack time. Setup time between low rail buck voltage and high rail buck voltage | | 100 | | µs |
| $t_{dcy}$ | Decay time | | 50 | | ms |

1. Guaranteed by design and parameter correlation.
2. Refer to the application information in *Section 4.3 on page 27*.

**Table 7. Timing characteristics of the I²C interface for I²C interface signals over recommended operating conditions (unless otherwise specified)**

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $f_{SCL}$ | Frequency, SCL | | | 400 | kHz |
| $t_{d(H)}$ | Pulse duration, SCL high | 0.6 | | | µs |
| $t_{d(L)}$ | Pulse duration, SCL low | 1.3 | | | µs |
| $t_{st1}$ | Setup time, SDA to SCL | 100 | | | ns |
| $t_{h1}$ | Hold time, SCL to SDA | 0 | | | ns |
| $t_f$ | Bus free time between stop and start condition | 1.3 | | | µs |
| $t_{st2}$ | Setup time, SCL to start condition | 0.6 | | | µs |
| $t_{h2}$ | Hold time, start condition to SCL | 0.6 | | | µs |
| $t_{st3}$ | Setup time, SCL to stop condition | 0.6 | | | µs |

**Figure 2. SCL and SDA timing diagram**

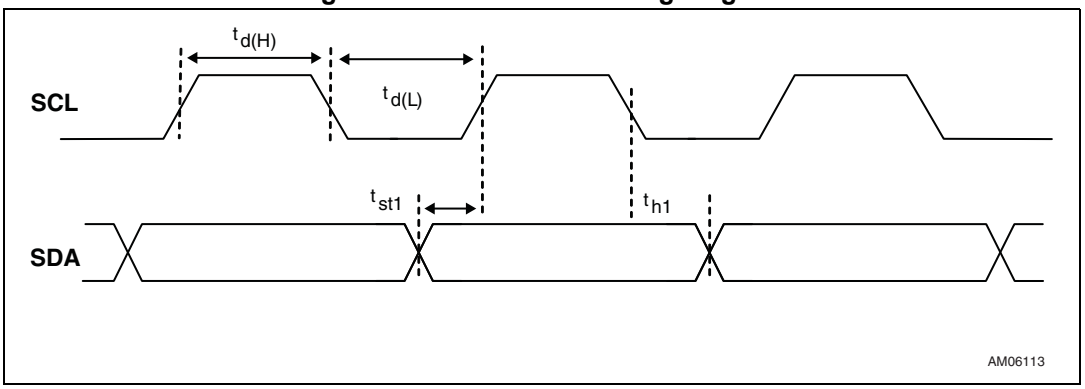



**Figure 3. Start and stop condition timing diagram**

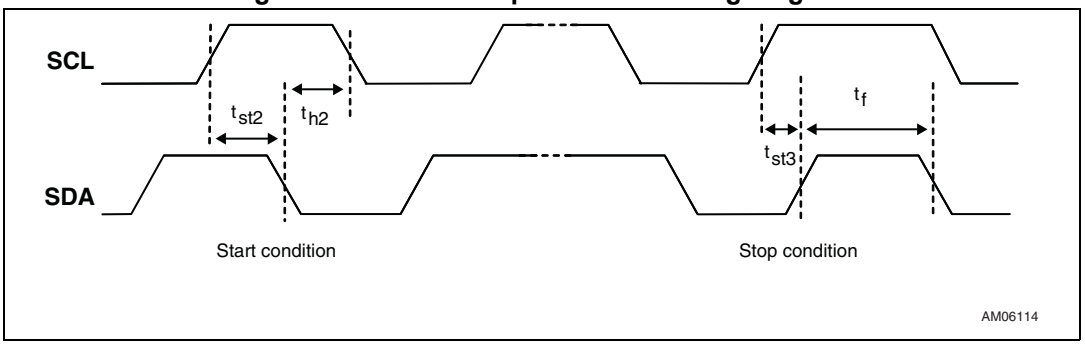


**Figure 4. Current consumption vs. power supply voltage**

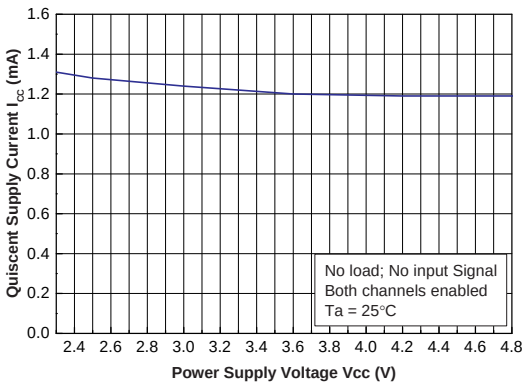



**Figure 5. Standby current consumption vs. power supply voltage**

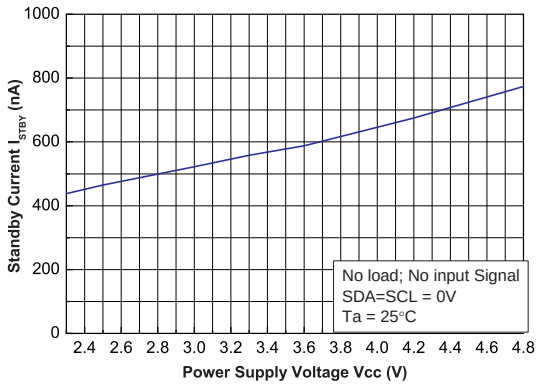



**Figure 6. Maximum output power vs. load**

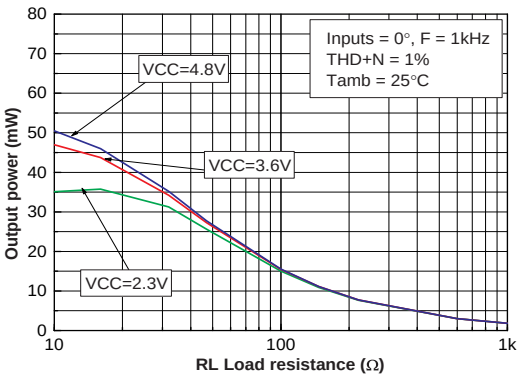



**Figure 7. Maximum output power vs. load**

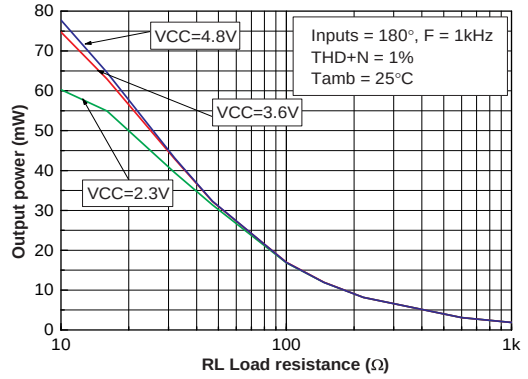



**Figure 8. Maximum output power vs. power supply voltage**

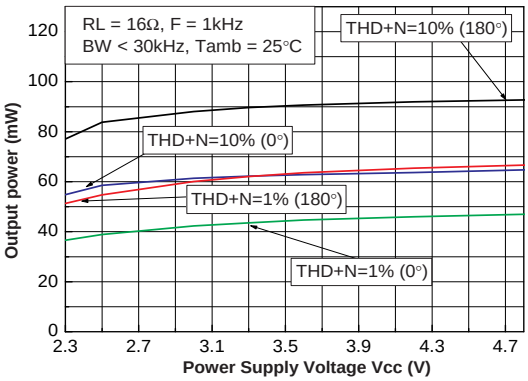



**Figure 9. Maximum output power vs. power supply voltage**

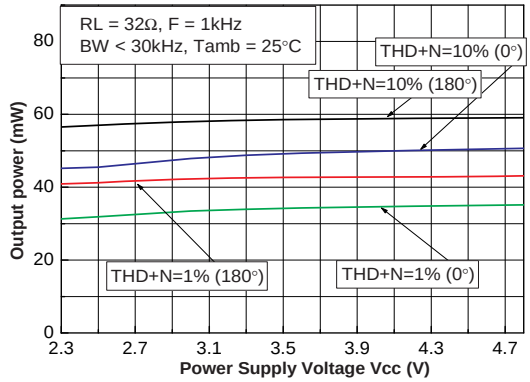


**Figure 10. Maximum output power vs. power supply voltage**

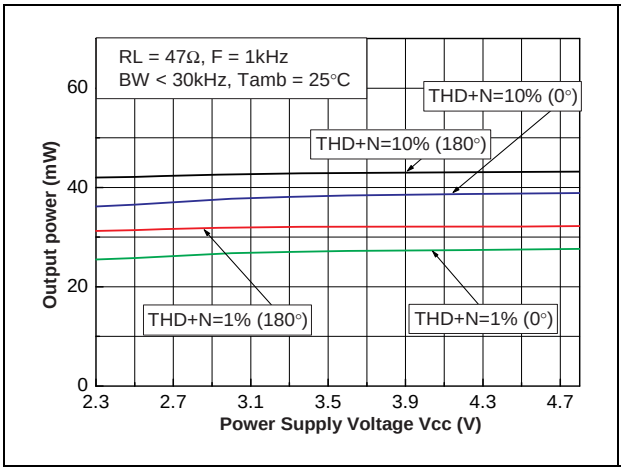



**Figure 11. Maximum output voltage vs. power supply voltage**

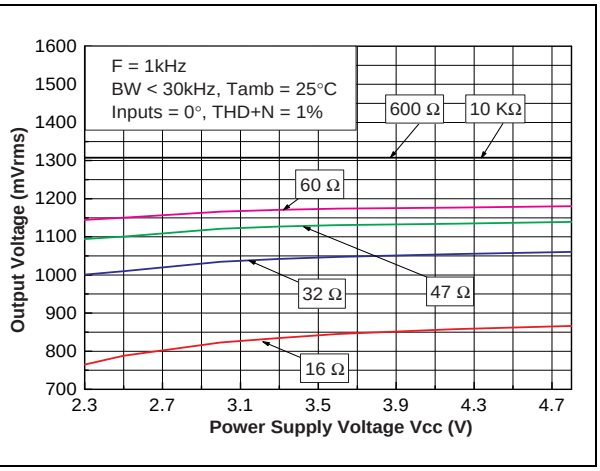



**Figure 12. Maximum output voltage vs. power supply voltage**

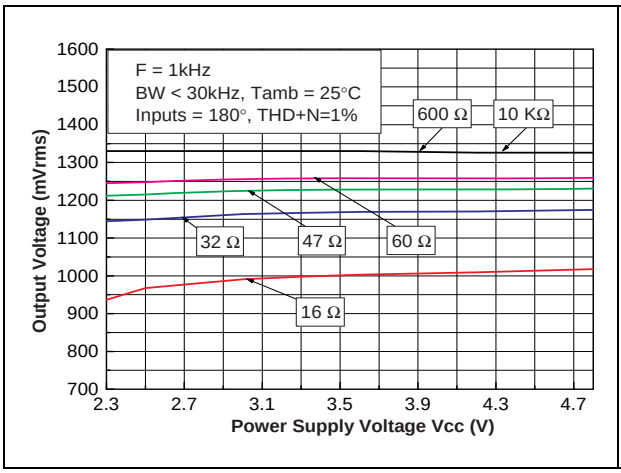



**Figure 13. Current consumption vs. total output power**

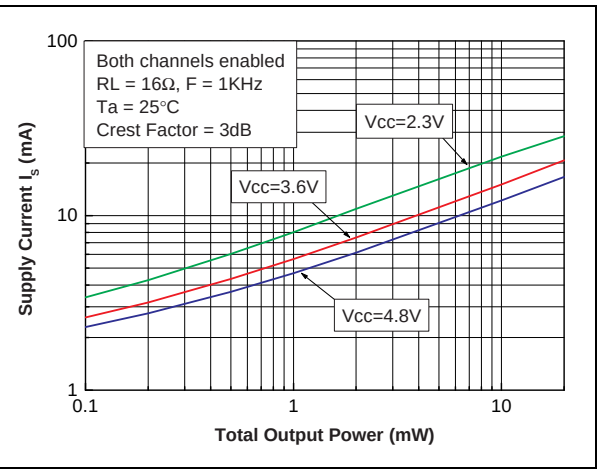



**Figure 14. Current consumption vs. total output power**

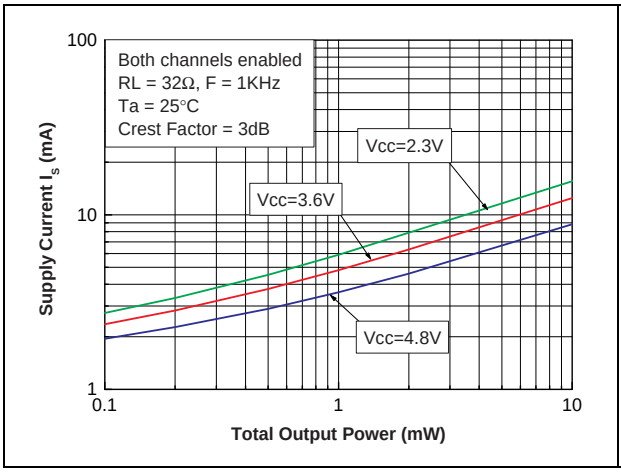



**Figure 15. Current consumption vs. total output power**

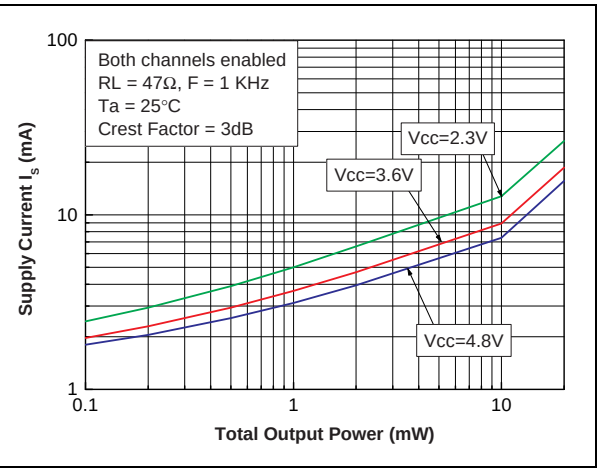


**Figure 16. Current consumption vs. total output power**

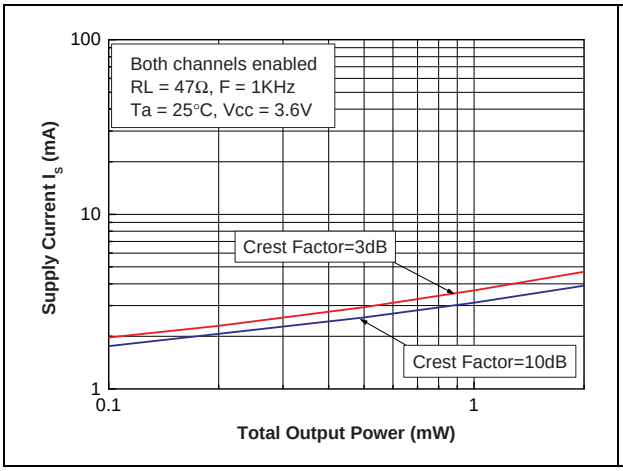



**Figure 17. Power dissipation vs. total output power**

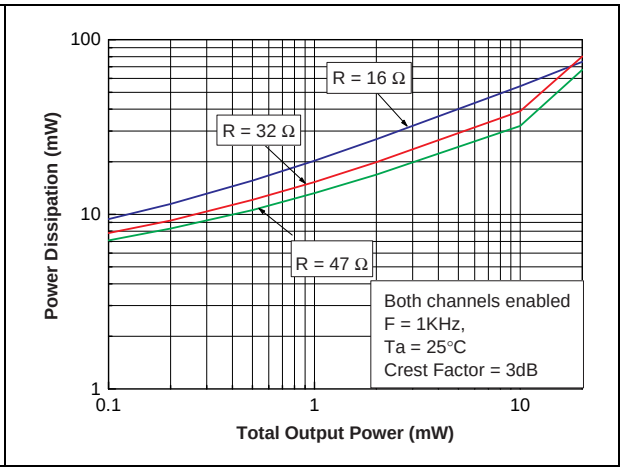



**Figure 18. Output impedance vs. frequency**

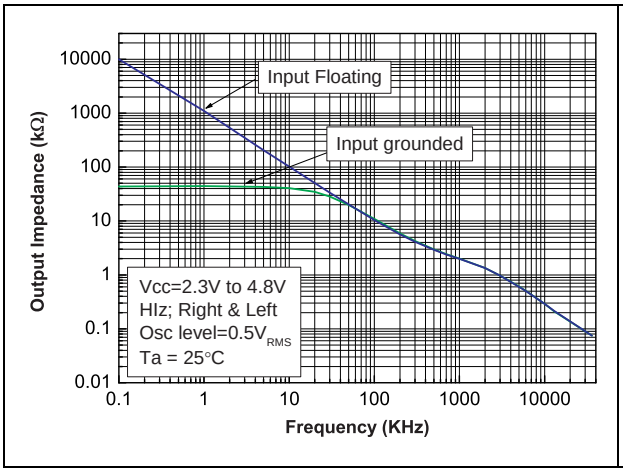



**Figure 19. Differential input impedance vs. gain**

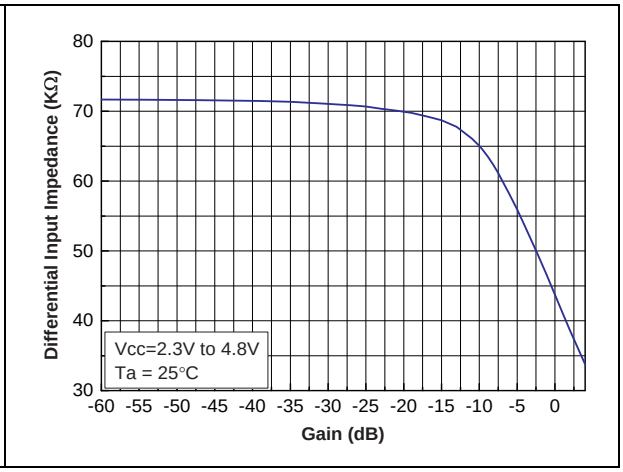



**Figure 20. THD+N vs. output power**

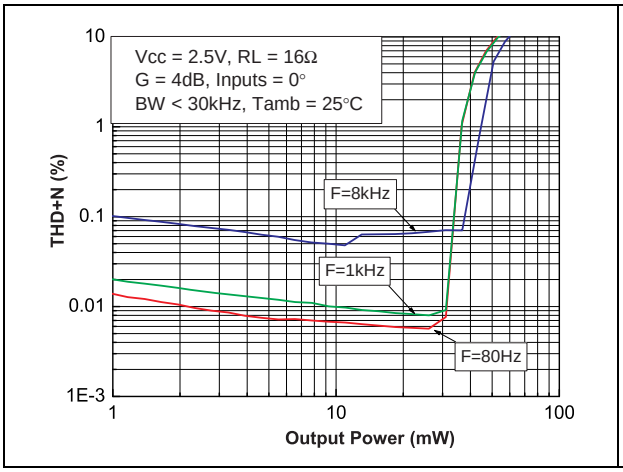



**Figure 21. THD+N vs. output power**

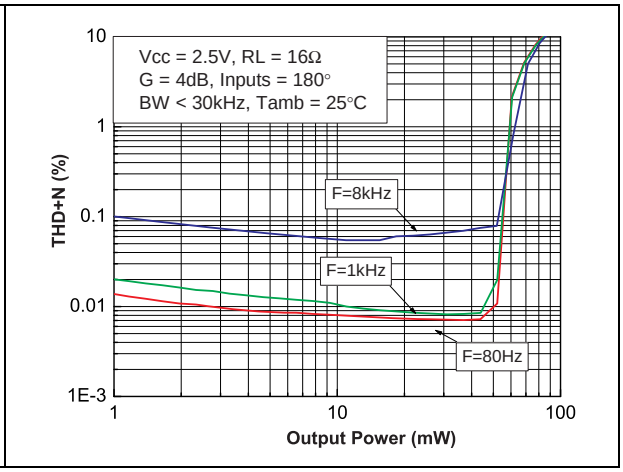


**Figure 22. THD+N vs. output power**

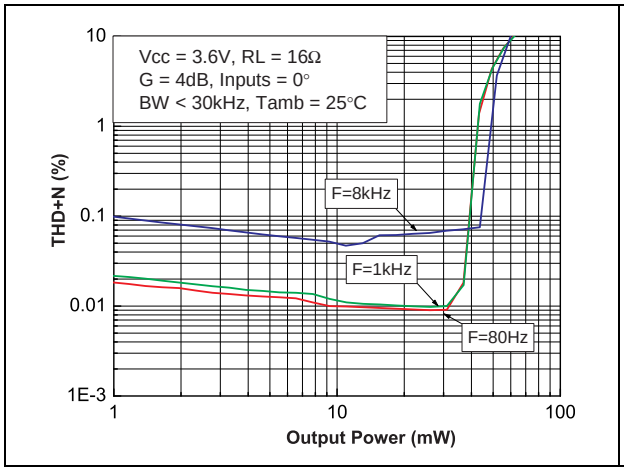



**Figure 23. THD+N vs. output power**

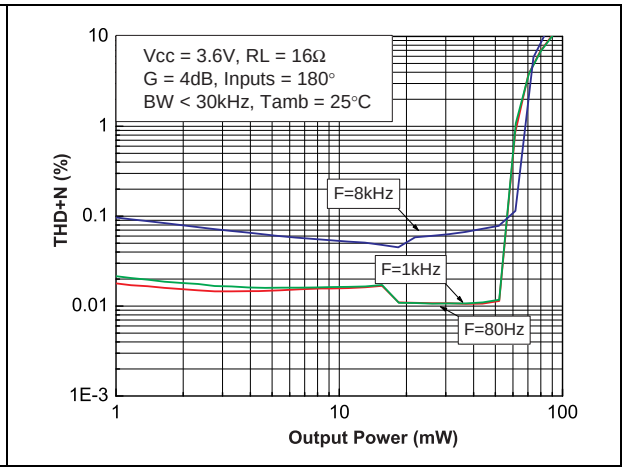



**Figure 24. THD+N vs. output power**

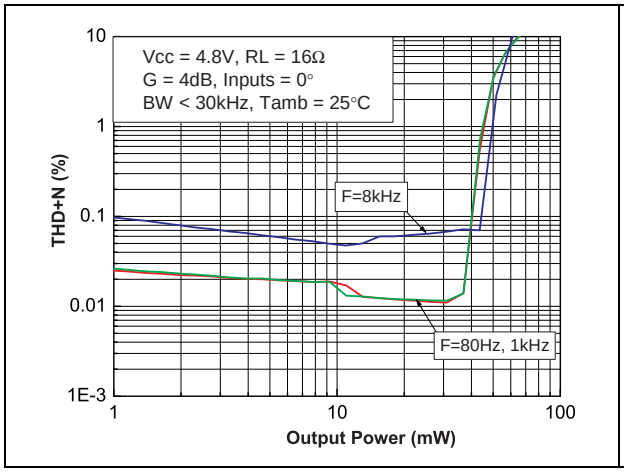



**Figure 25. THD+N vs. output power**

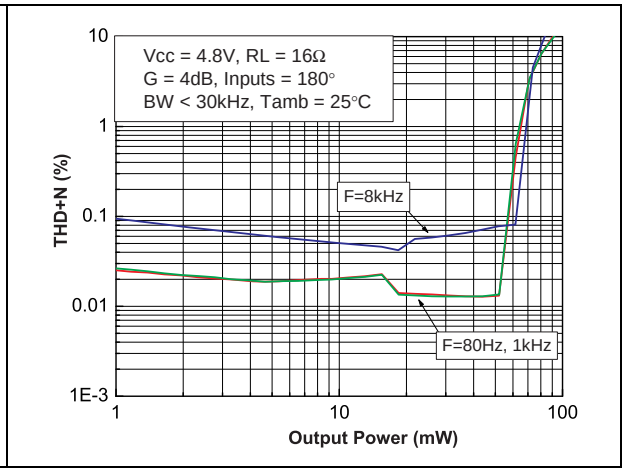



**Figure 26. THD+N vs. output power**

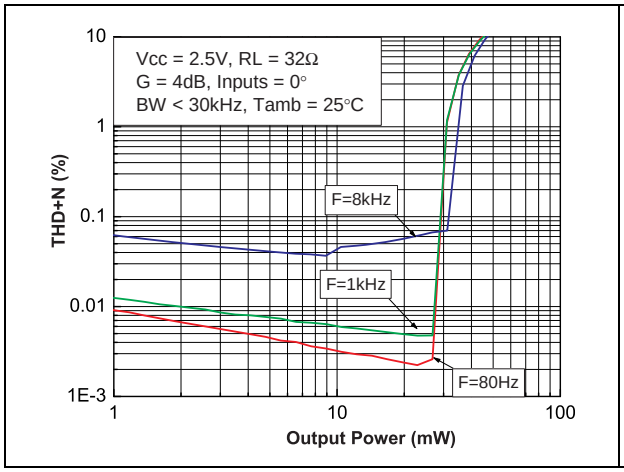



**Figure 27. THD+N vs. output power**

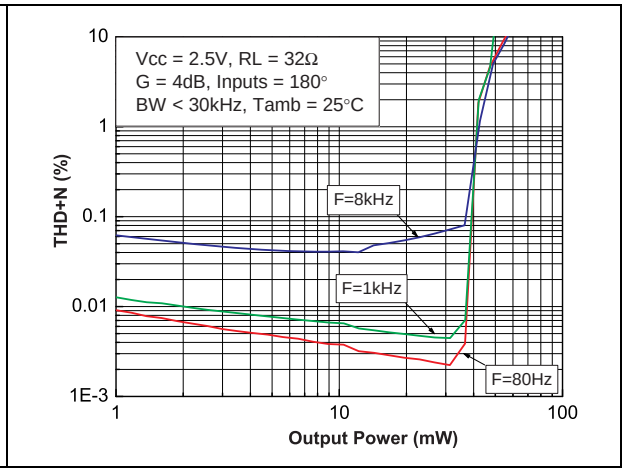


Figure 28. THD+N vs. output power

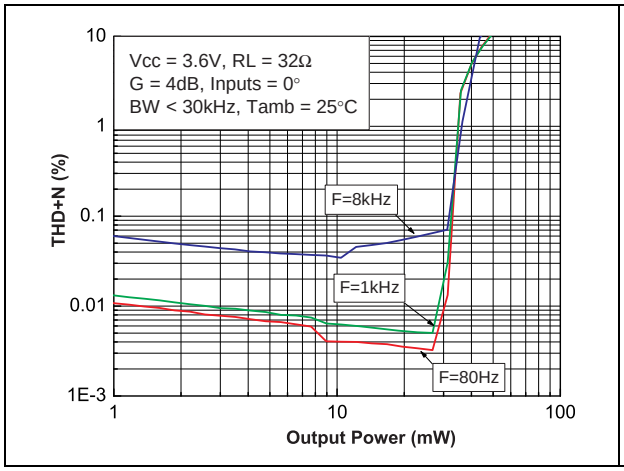



Figure 29. THD+N vs. output power

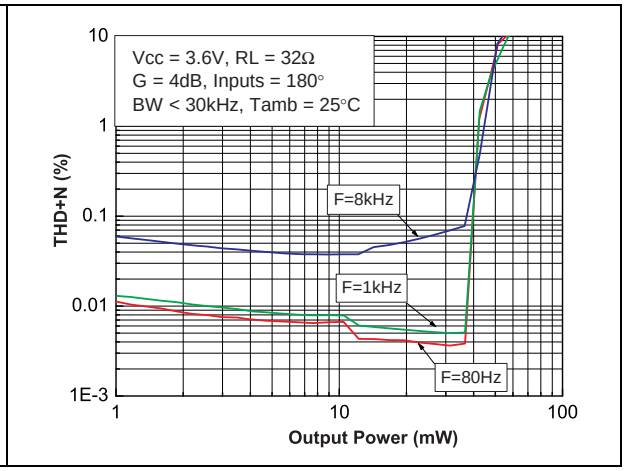



Figure 30. THD+N vs. output power

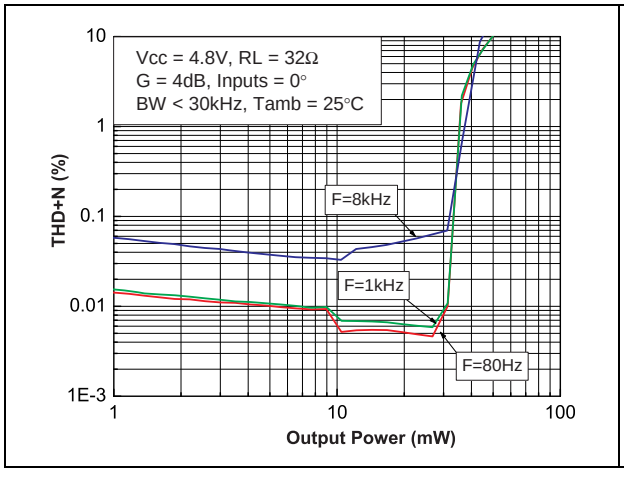



Figure 31. THD+N vs. output power

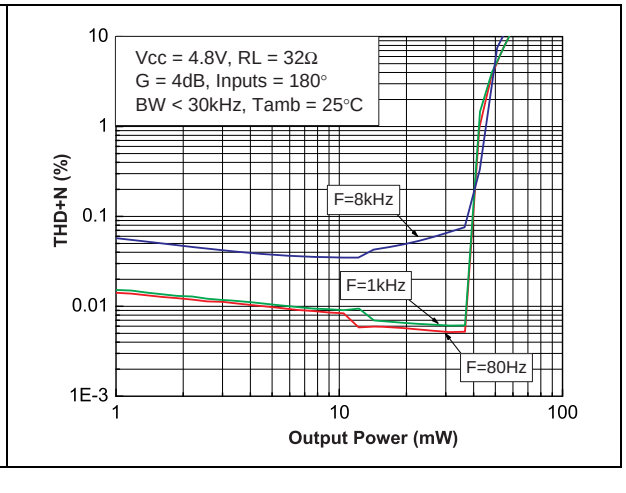



Figure 32. THD+N vs. output power

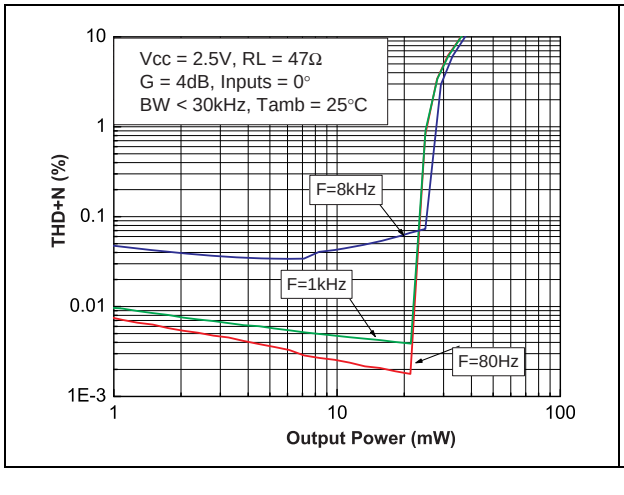



Figure 33. THD+N vs. output power

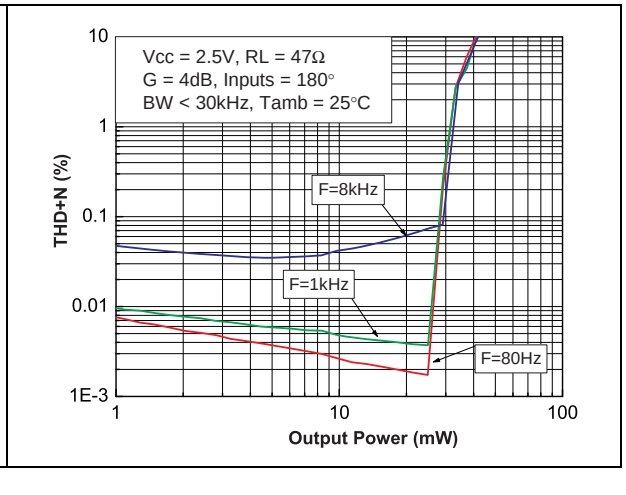


**Figure 34. THD+N vs. output power**

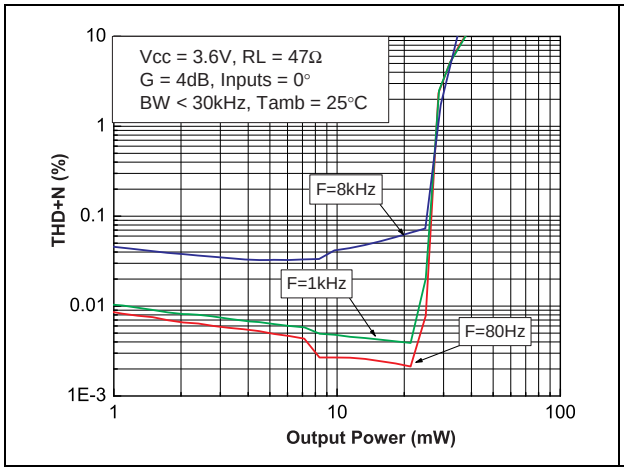



**Figure 35. THD+N vs. output power**

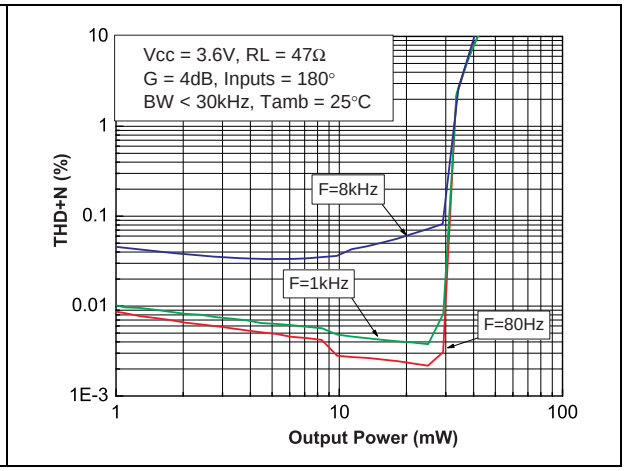



**Figure 36. THD+N vs. output power**

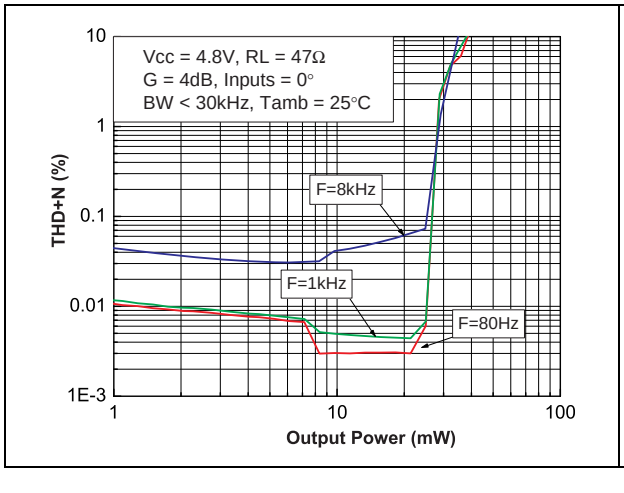



**Figure 37. THD+N vs. output power**

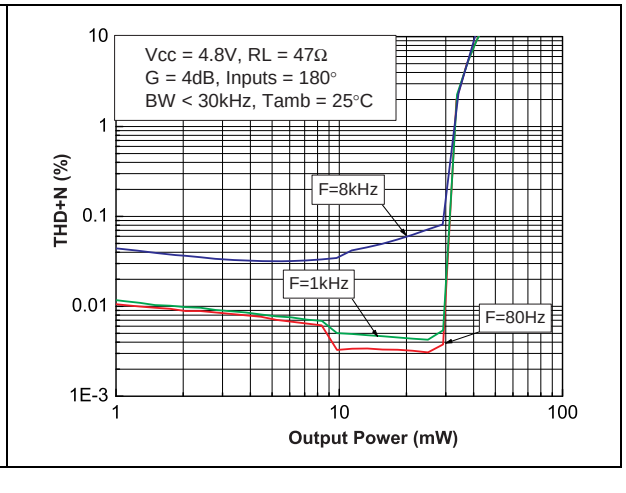



**Figure 38. THD+N vs. frequency**

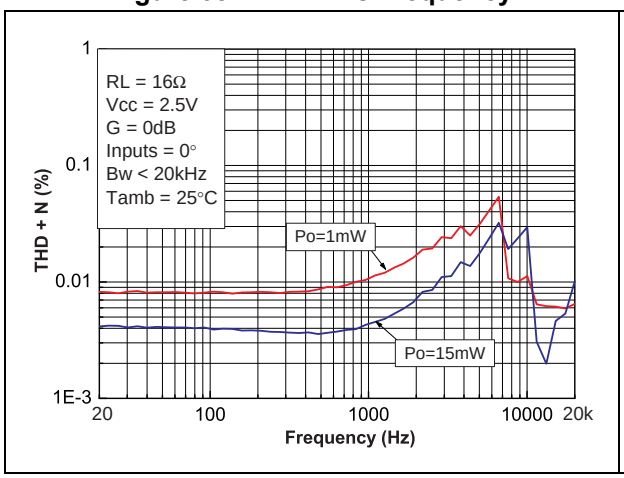



**Figure 39. THD+N vs. frequency**

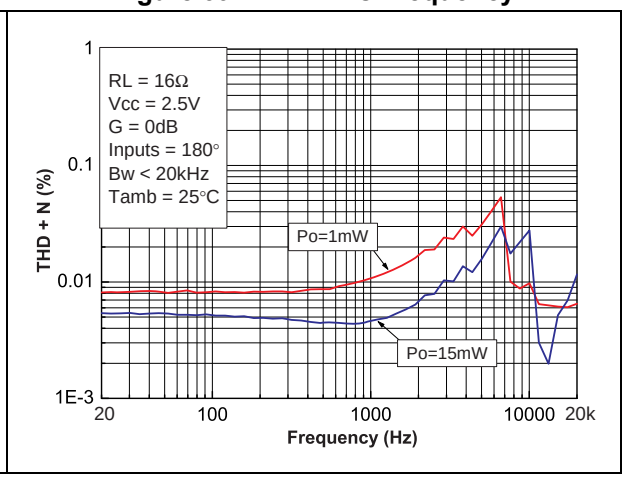


Figure 40. THD+N vs. frequency

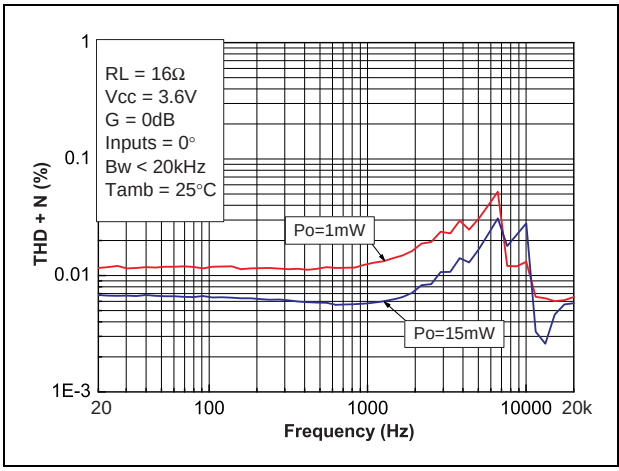



Figure 41. THD+N vs. frequency

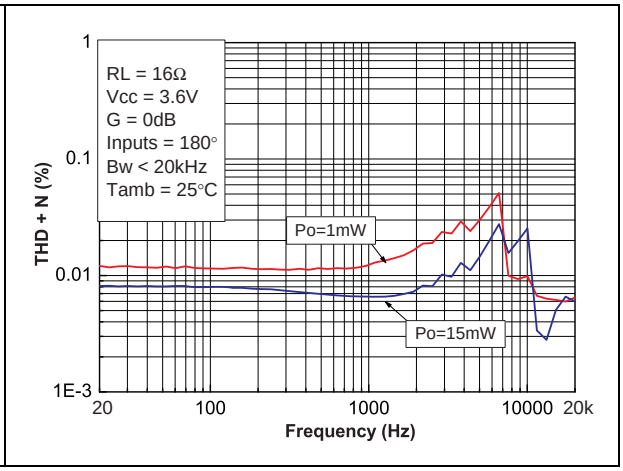



Figure 42. THD+N vs. frequency

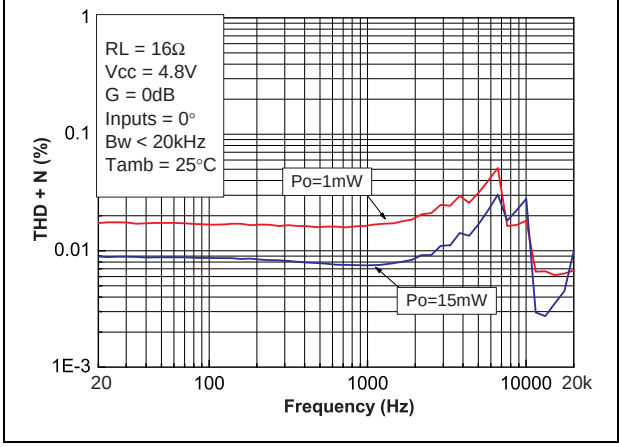



Figure 43. THD+N vs. frequency

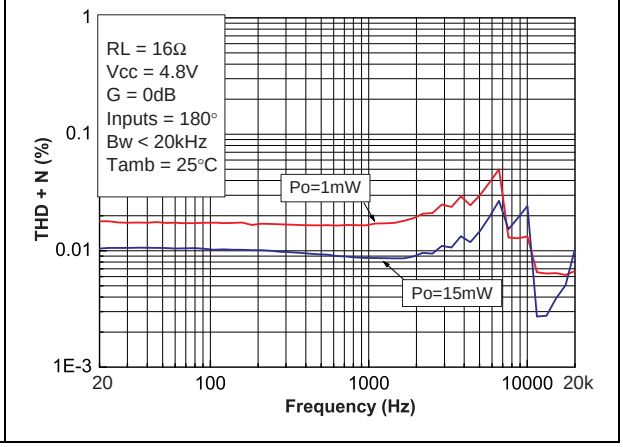



Figure 44. THD+N vs. frequency

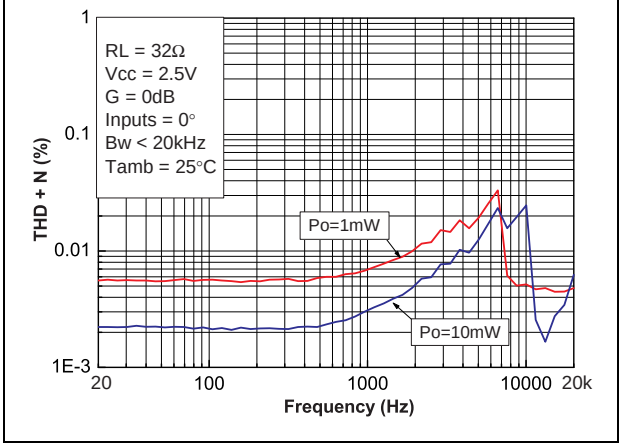



Figure 45. THD+N vs. frequency

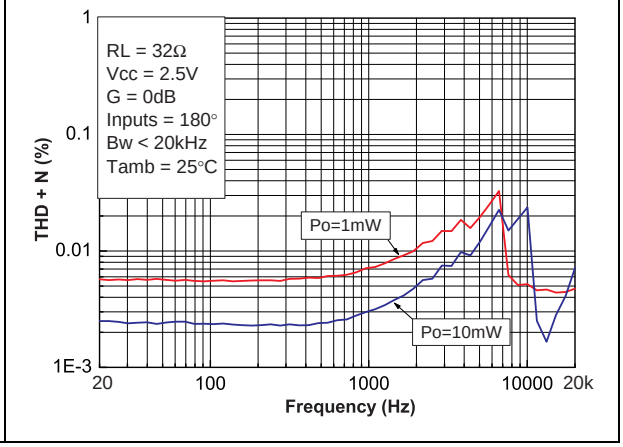


**Figure 46. THD+N vs. frequency**

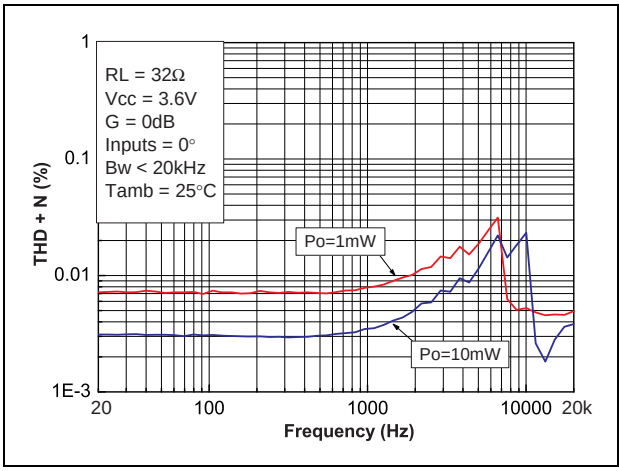



**Figure 47. THD+N vs. frequency**

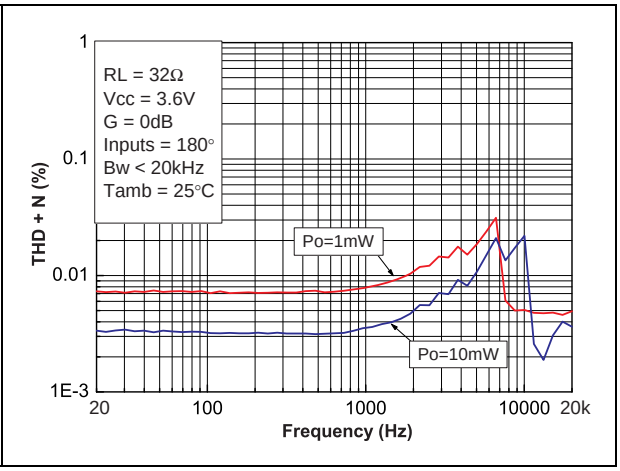



**Figure 48. THD+N vs. frequency**

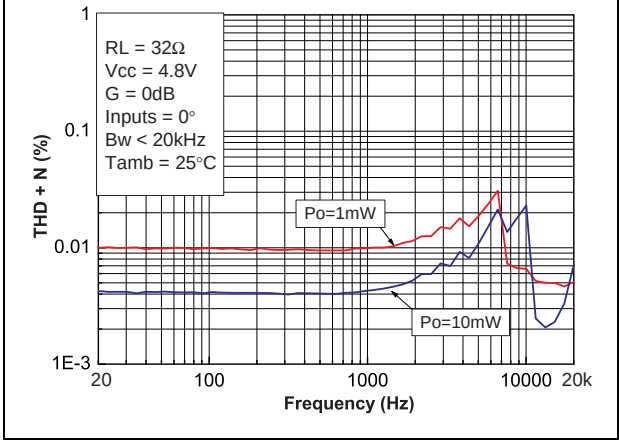



**Figure 49. THD+N vs. frequency**

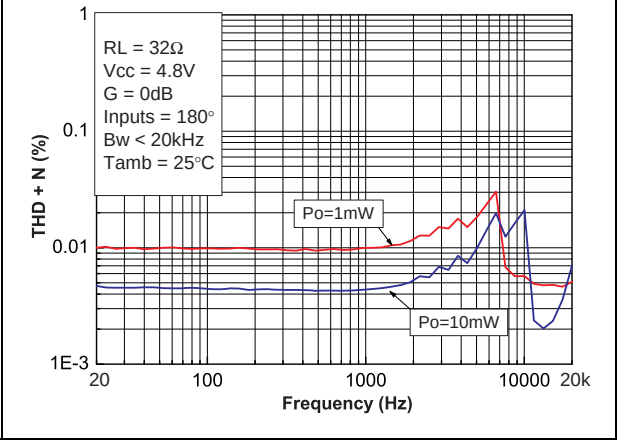



**Figure 50. THD+N vs. frequency**

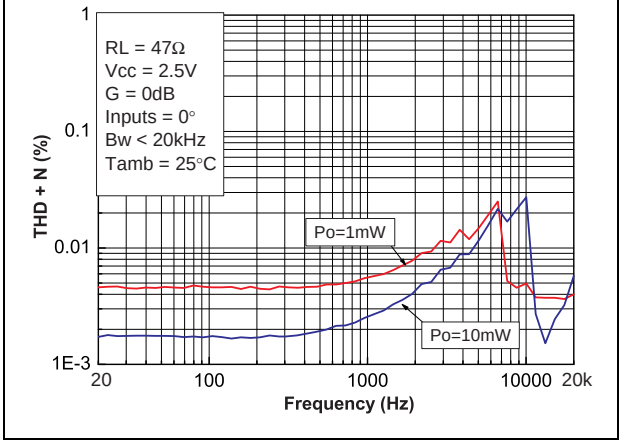



**Figure 51. THD+N vs. frequency**

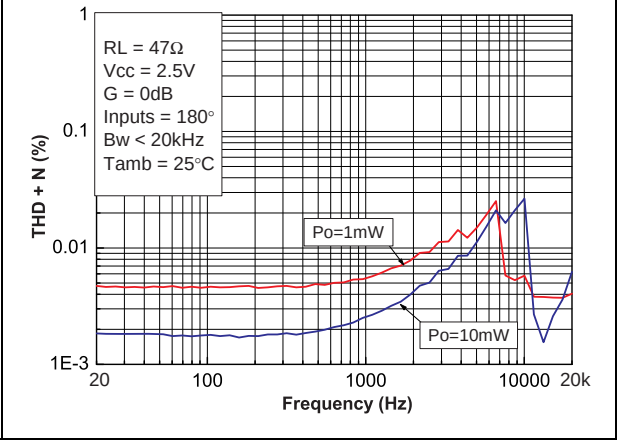


**Figure 52. THD+N vs. frequency**

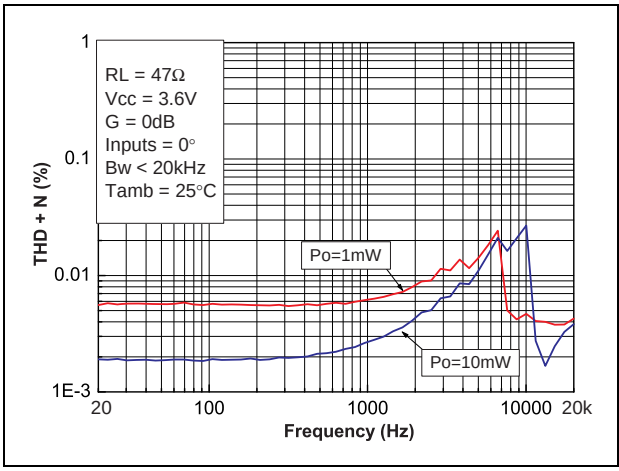



**Figure 53. THD+N vs. frequency**

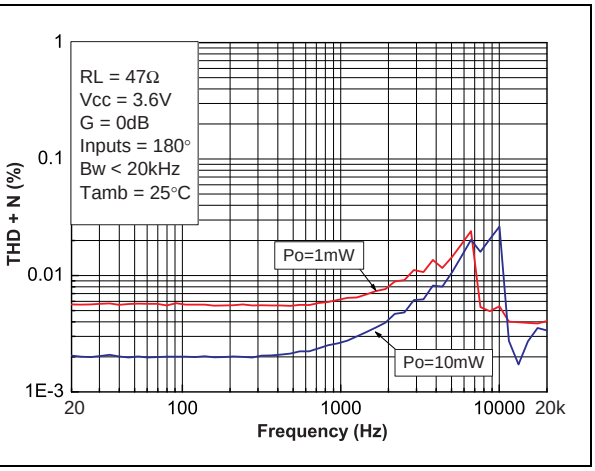



**Figure 54. THD+N vs. frequency**

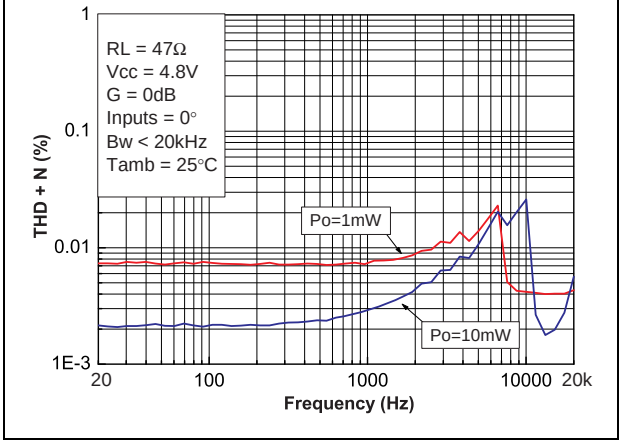



**Figure 55. THD+N vs. frequency**

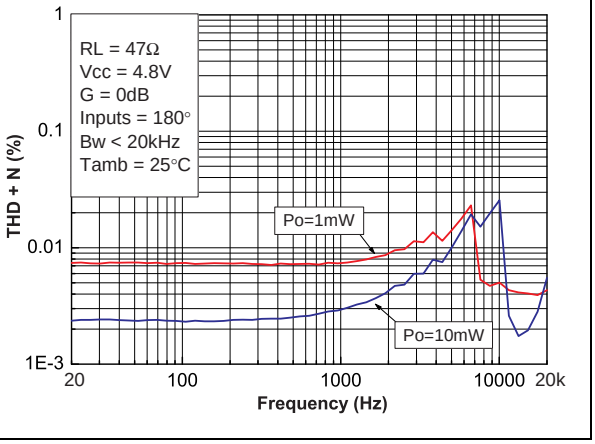



**Figure 56. THD+N vs. frequency**

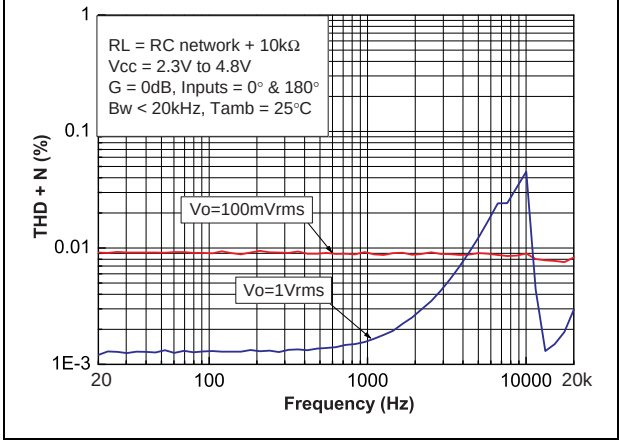



**Figure 57. THD+N vs. frequency**

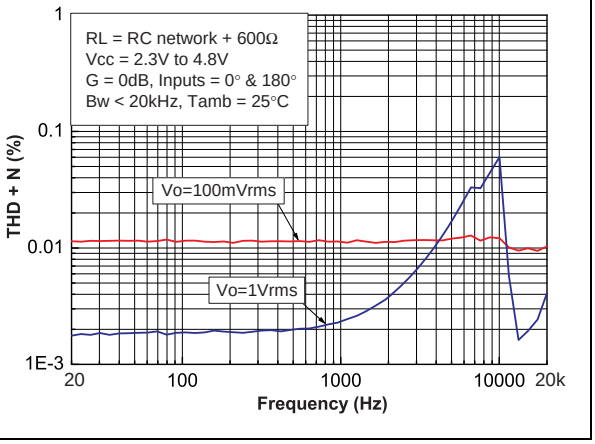


**Figure 58. THD+N vs. output voltage**

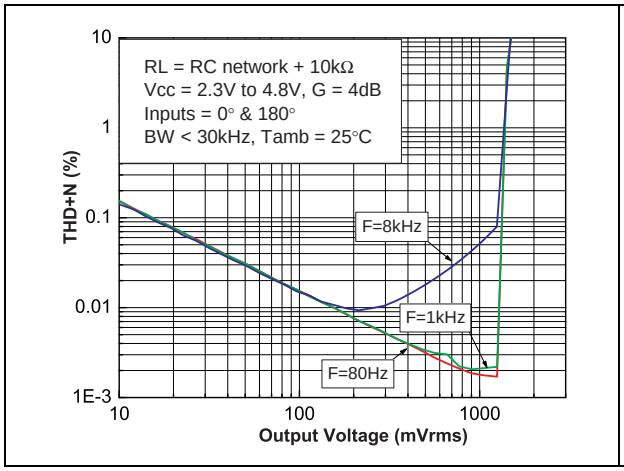



**Figure 59. THD+N vs. output voltage**

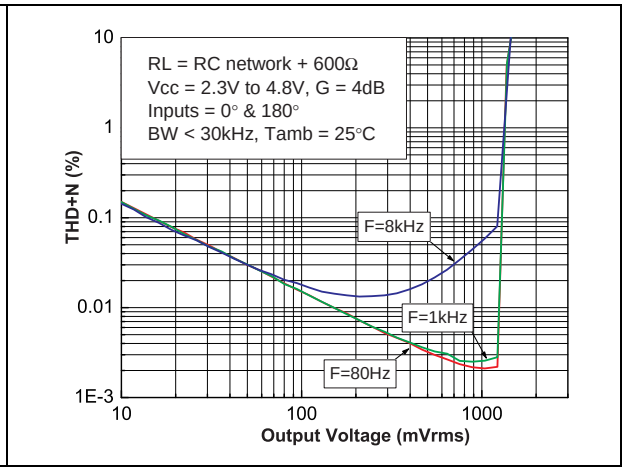



**Figure 60. THD+N vs. input voltage, HiZ left and right**

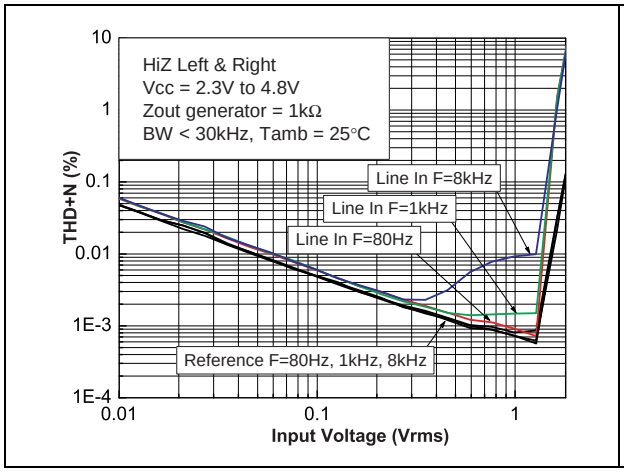



**Figure 61. CMRR vs. frequency**

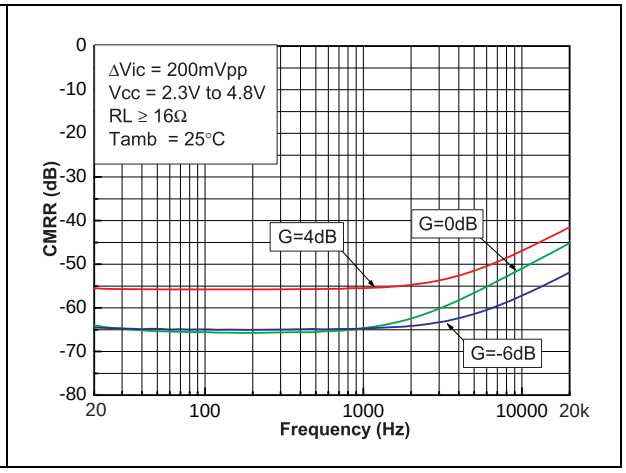



**Figure 62. PSRR vs. frequency**

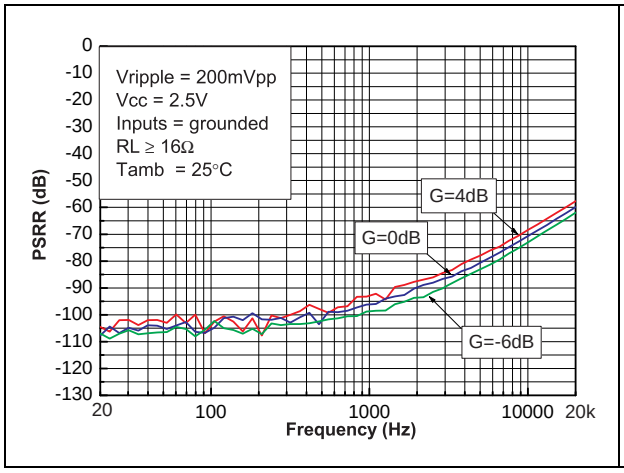



**Figure 63. PSRR vs. frequency**

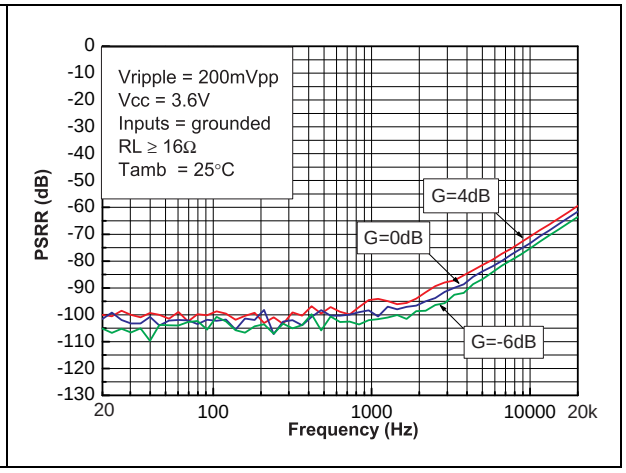


Figure 64. PSRR vs. frequency

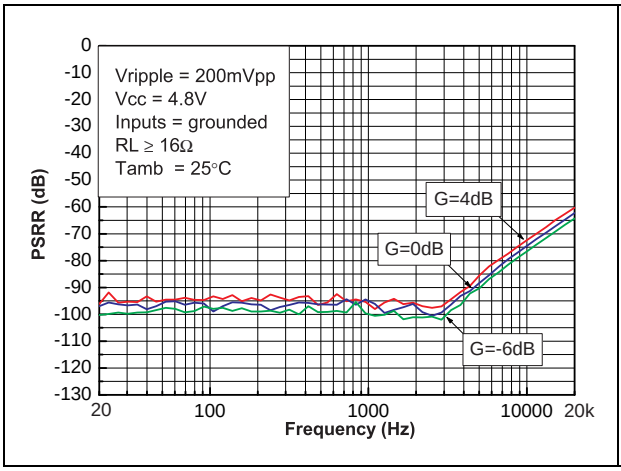



Figure 65. Output signal spectrum

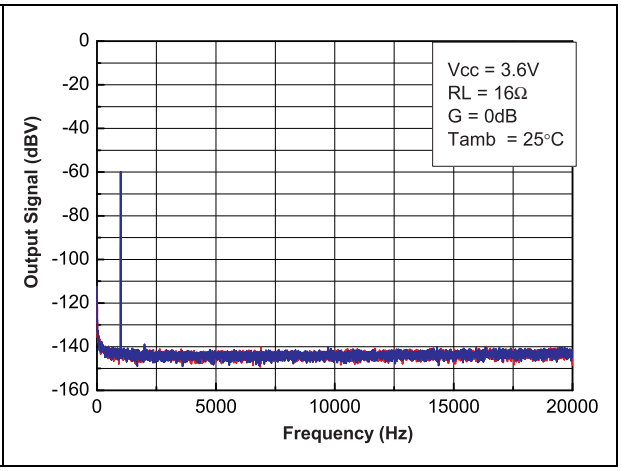



Figure 66. Crosstalk vs. frequency

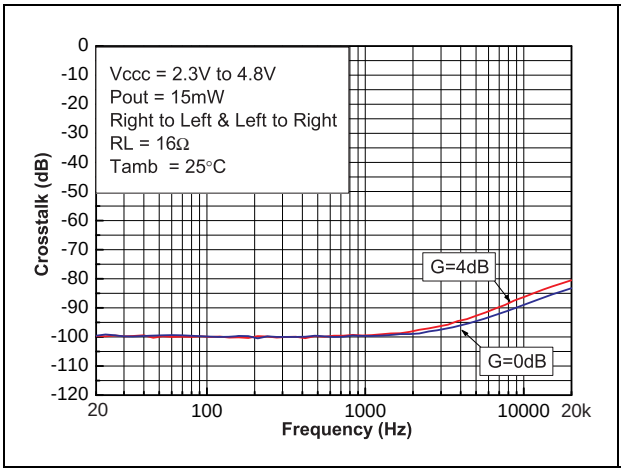



Figure 67. Crosstalk vs. frequency

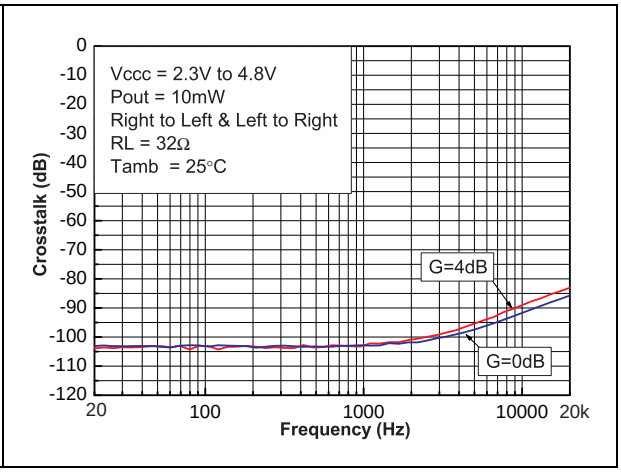



Figure 68. Crosstalk vs. frequency

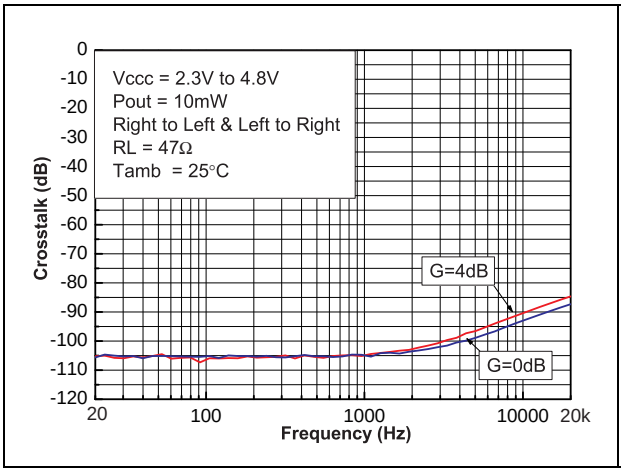



Figure 69. Crosstalk vs. frequency

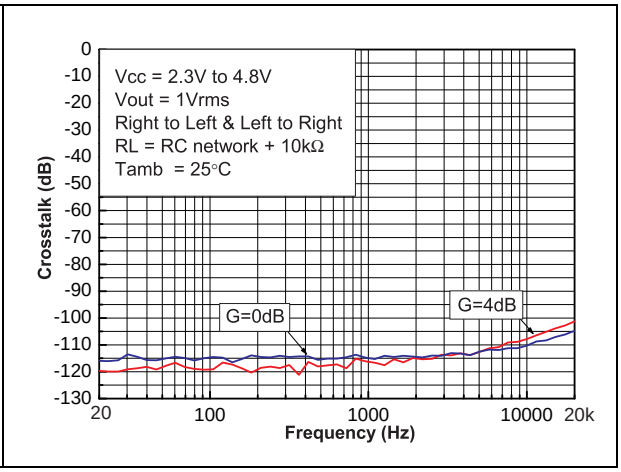


Figure 70. Wake-up time

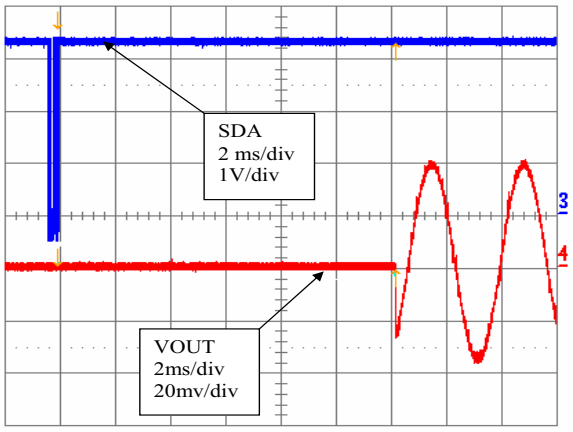
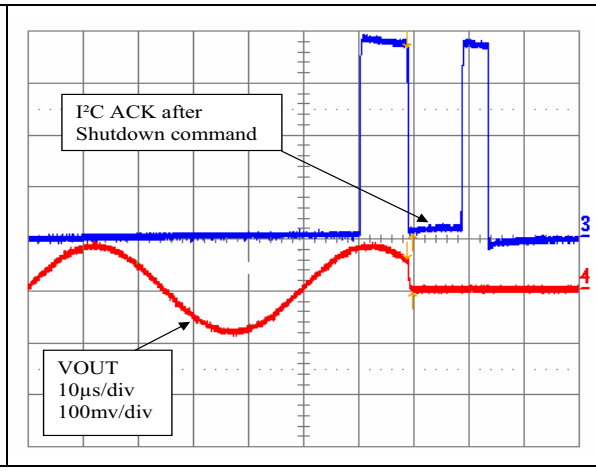



Figure 71. Shutdown time



# 4 Application information

## 4.1 I²C bus interface

In compliance with the I²C protocol, the A22H165M uses a serial bus to control the chip's functions with the clock (SCL) and data (SDA) wires. These two lines are bi-directional (open collector) and require an external pull-up resistor (typically 10 kΩ). The maximum clock frequency in fast mode specified by the I²C standard is 400 kHz, which the A22H165M supports. In this application, the A22H165M is always the slave device and the controlling microcontroller MCU is the master device.

The slave address of the A22H165M is 1100 000x (C0h).

*Table 8* summarizes the pin descriptions for the I²C bus interface.

**Table 8. I²C bus interface pin descriptions**

| Pin | Functional description |
|---|---|
| SDA | Serial data pin |
| SCL | Clock input pin |

### 4.1.1 I²C bus operation

The host MCU can write to the A22H165M control register to control the A22H165M, and read from the control register to obtain a configuration from the A22H165M. The A22H165M is addressed by the byte consisting of the 7-bit slave address and the R/$\overline{W}$ bit.

**Table 9. First byte after the START message for addressing the device**

| A6 | A5 | A4 | A3 | A2 | A1 | A0 | R/$\overline{W}$ |
|---|---|---|---|---|---|---|---|
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | X |

There are four control registers (*Table 10*) named CR1 to CR4. In read mode, all the control registers can be accessed. In write mode, only CR1, CR2 and CR3 can be addressed.

**Table 10. Summary of control registers**

| Description | Register address | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| CR1 | 1 | HP_EN_L | HP_EN_R | 0 | 0 | SC_L | SC_R | T_SH | SWS |
| CR2 volume control | 2 | Mute_L | Mute_R | Volume control | | | | | 0 |
| CR3 | 3 | 0 | 0 | 0 | 0 | 0 | 0 | HiZ_L | HiZ_R |
| CR4 identification | 4 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |

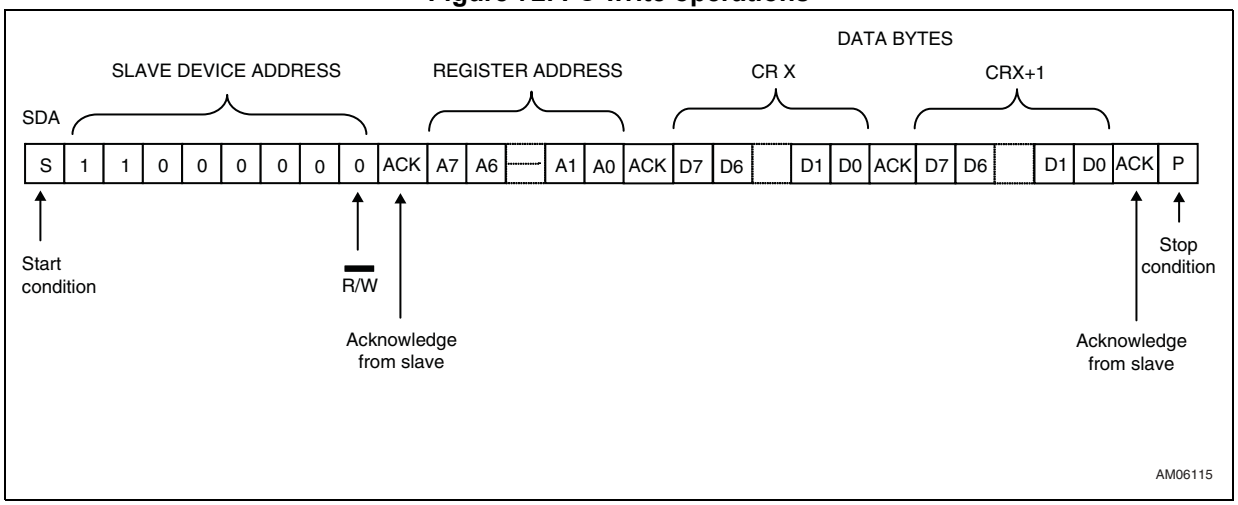
### Writing to the control registers

To write data to the A22H165M, after the "start" message the MCU must:

- send the I²C 7-bit slave address and a low level for the R/$\overline{W}$ bit.
- send the register address to write to.
- send the data bytes (control register settings).

All bytes are sent MSB first. The transfer of written data ends with a "stop" message. When transmitting several data bytes, the data can be written without having to repeat the "start" message or send the byte with the slave address. If several bytes are transmitted, they will be written repeatedly to CR1, CR2 and CR3.

**Figure 72. I²C write operations**



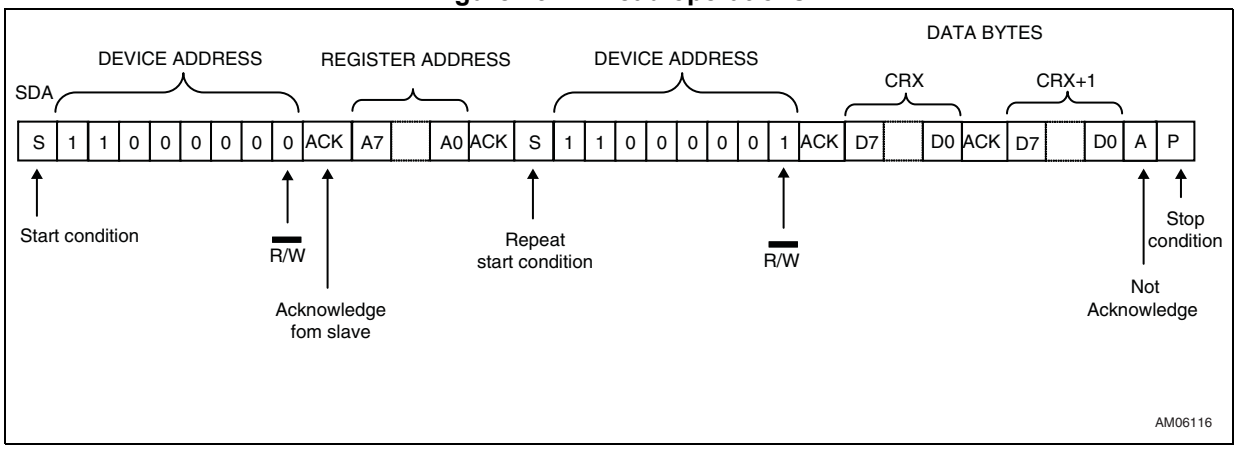

### Reading from the control registers

To read data from the A22H165M, after the "start" message the MCU must:

- send the I²C 7-bit slave address and a low level for the R/$\overline{W}$ bit.
- send the register address to write to.
- send the I²C 7-bit slave address and a high level for the R/$\overline{W}$ bit.
- receive the data (control register value).

All bytes are read MSB first. The transfer of read data ends with a "stop" message. When transmitting several data bytes, the data can be read without having to repeat the "start" message or send the byte with the slave address. If several bytes are transmitted, they will be read repeatedly from CR1, CR2, CR3 and CR4.

**Figure 73. I²C read operations**




## 4.1.2 Control register CR2 - address 2

**Table 11. Volume control register CR2 - address 2**

| Volume control range: -60 dB to +4 dB | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **D5** | **D4** | **D3** | **D2** | **D1** | **Gain (in dB)** | | **D5** | **D4** | **D3** | **D2** | **D1** | **Gain (in dB)** |
| 0 | 0 | 0 | 0 | 0 | -60 dB | | 1 | 0 | 0 | 0 | 0 | -11 dB |
| 0 | 0 | 0 | 0 | 1 | -54 dB | | 1 | 0 | 0 | 0 | 1 | -10 dB |
| 0 | 0 | 0 | 1 | 0 | -50.5 dB | | 1 | 0 | 0 | 1 | 0 | -9 dB |
| 0 | 0 | 0 | 1 | 1 | -47 dB | | 1 | 0 | 0 | 1 | 1 | -8 dB |
| 0 | 0 | 1 | 0 | 0 | -43 dB | | 1 | 0 | 1 | 0 | 0 | -7 dB |
| 0 | 0 | 1 | 0 | 1 | -39 dB | | 1 | 0 | 1 | 0 | 1 | -6 dB |
| 0 | 0 | 1 | 1 | 0 | -35 dB | | 1 | 0 | 1 | 1 | 0 | -5 dB |
| 0 | 0 | 1 | 1 | 1 | -31 dB | | 1 | 0 | 1 | 1 | 1 | -4 dB |
| 0 | 1 | 0 | 0 | 0 | -27 dB | | 1 | 1 | 0 | 0 | 0 | -3 dB |
| 0 | 1 | 0 | 0 | 1 | -25 dB | | 1 | 1 | 0 | 0 | 1 | -2 dB |
| 0 | 1 | 0 | 1 | 0 | -23 dB | | 1 | 1 | 0 | 1 | 0 | -1 dB |
| 0 | 1 | 0 | 1 | 1 | -21 dB | | 1 | 1 | 0 | 1 | 1 | 0 dB |
| 0 | 1 | 1 | 0 | 0 | -19 dB | | 1 | 1 | 1 | 0 | 0 | +1 dB |
| 0 | 1 | 1 | 0 | 1 | -17 dB | | 1 | 1 | 1 | 0 | 1 | +2 dB |
| 0 | 1 | 1 | 1 | 0 | -15 dB | | 1 | 1 | 1 | 1 | 0 | +3 dB |
| 0 | 1 | 1 | 1 | 1 | -13 dB | | 1 | 1 | 1 | 1 | 1 | +4 dB |

### Mute function: bits MUTE_L and MUTE_R

In the volume register, MUTE_L and MUTE_R are dedicated to enabling the mute function, independently of the channel. When MUTE_L and MUTE_R are set to $V_{IH}$, the mute function is enabled on the corresponding channel and the gain is set to -80 dB. When MUTE_L and MUTE_R are set to $V_{IL}$, the I²C gain level is applied to the channel.

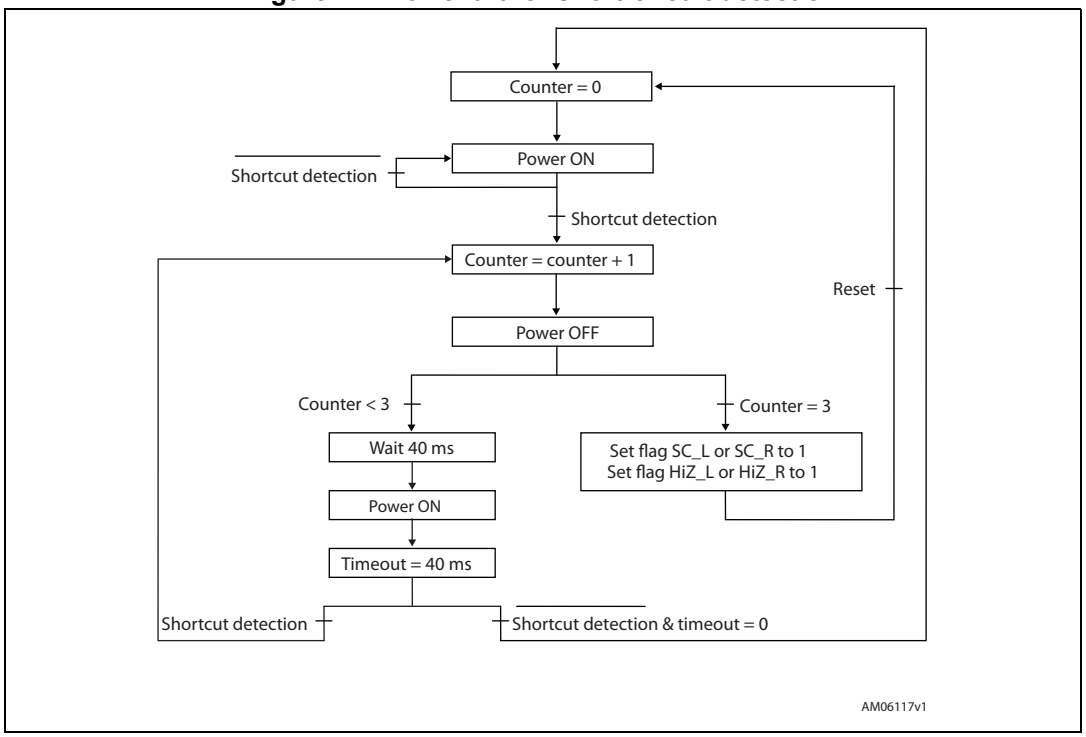
### 4.1.3 Control register CR1 - address 1

#### Amplifier output short-circuit detection: bits SC_L and SC_R

The amplifier's outputs are protected from short-circuit that might accidentally occur during manipulation of the device. In a typical application, if a short-circuit arises on the jack plug, there will be no detection because of the serial resistor present on the amplifier output, thus the output current threshold will not be reached.

To be active, the detection has to occur directly on the amplifier's output with a signal modulation on the inputs of the A22H165M. This detection is depicted in *Figure 74*.

**Figure 74. Flowchart for short-circuit detection**




If a short-circuit is detected three consecutive times on one channel, a flag is raised in the I²C read register CR1.

- SC_L: equals 0 during normal operation, equals 1 when a short-circuit is detected on the left channel.
- SC_R: equals 0 during normal operation, equals 1 when a short-circuit is detected on the right channel.

The corresponding channel's output stage is then set to high impedance mode. An I²C read command allows the reading of the SC_L and SC_R flags but does not reset them. An I²C write command has to be sent to CR1 to reset the flags to 0 and restore normal operation.

### Thermal shutdown protection: bit T_SH

A thermal shutdown protection is implemented to protect the device from overheating. If the temperature rises above the thermal junction of 150°C, the device is put into standby mode and a flag is raised in the read register CR1.

- T_SH: equals 0 during normal operation, equals 1 when a thermal shutdown is detected.

When the temperature decreases to safe levels, the circuit switches back to normal operation and the corresponding flag is cleared.

### Software shutdown: bit SWS

When SWS equals 1, the device is set to I²C software shutdown. When SWS equals 0, the negative supply and buck converters are activated.

### Channel activation: bits HP_EN_L and HP_EN_R

When HP_EN_L or HP_EN_R equals 1, the corresponding amplifier channel is enabled.

## 4.2 Wake-up and standby time definition

The wake-up time of the A22H165M is guaranteed at 12 ms typical (refer to *Chapter 3: Electrical characteristics on page 7*). However, since the A22H165M is activated with an I²C bus, the wake-up start procedure is as follows.

1. The master sends a start bit.
2. The master sends the device address.
3. The slave (A22H165M) answers by an acknowledge bit.
4. The master sends the register address.
5. The slave (A22H165M) answers by an acknowledge bit.
6. The master sends the output mode configuration (CR1).
7. If the A22H165M was previously in standby mode, the wake-up starts on the falling edge of the eighth clock signal (SCL) corresponding to the CR1 byte.
8. After 12 ms (de-pop sequence time), the A22H165M outputs are operational.

The standby time is guaranteed as 100 µs typical (refer to *Chapter 3: Electrical characteristics on page 7*). However, since the A22H165M is de-activated with an I²C bus, the standby time operates as follows.

1. The master sends a start bit.
2. The master sends the device address.
3. The slave (A22H165M) answers by an acknowledge bit.
4. The master sends the register address.
5. The slave (A22H165M) answers by an acknowledge bit.
6. The master sends the output mode configuration (CR1), which corresponds, in this case, to standby mode.
7. The standby time starts on the falling edge of the eighth clock signal (SCL) corresponding to the CR1 byte.
8. After 100 µs, the A22H165M is in standby mode.

## 4.3 Common mode sense

The A22H165M implements a common-mode sense pin to correct any voltage differences that might occur between the return of the headphone jack and the GND of the device and create parasitic noise in the headphone and/or line out.

The solution to strongly reduce and practically eliminate this noise consists in connecting the headphone jack ground to the CMS pin. This pin senses the difference of potential (voltage noise) between the A22H165M ground and the headphone ground. By way of the frequency response of the common-mode sense pin, this noise is removed from the A22H165M outputs.

# 5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

**Figure 75. A22H165M footprint recommendation**

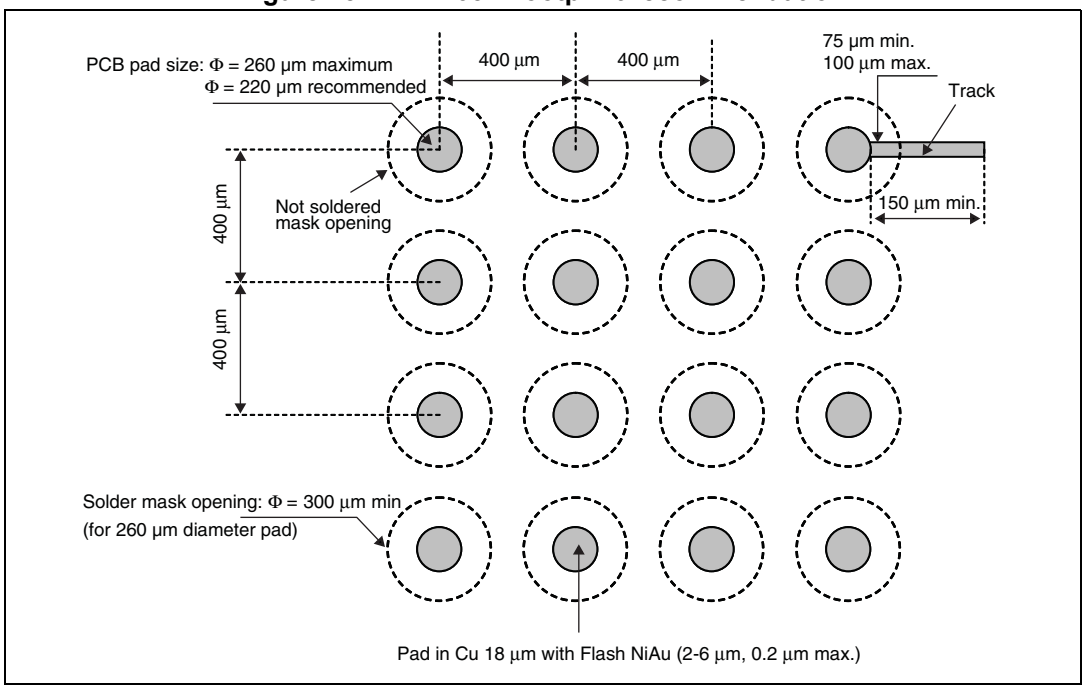



**Figure 76. Pinout**

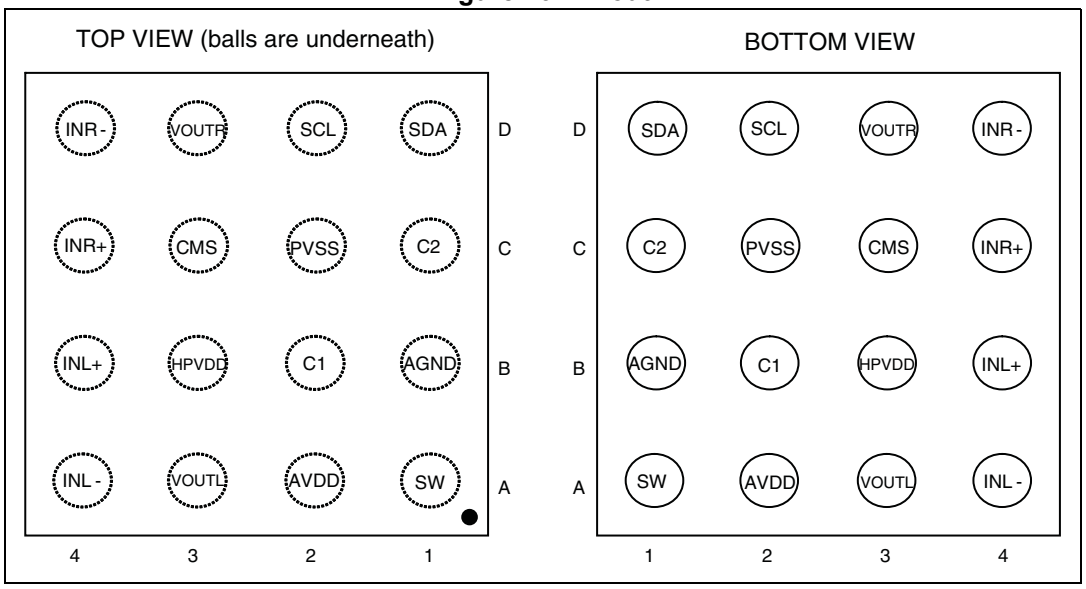


**Figure 77. Marking (top view)**

- Logo: ST
- Symbol for lead-free: E
- Part number: 21
- X digit: Assembly code
- Date code: YWW
- The dot marks pin A1

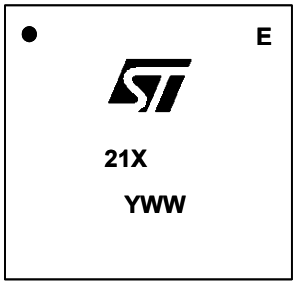
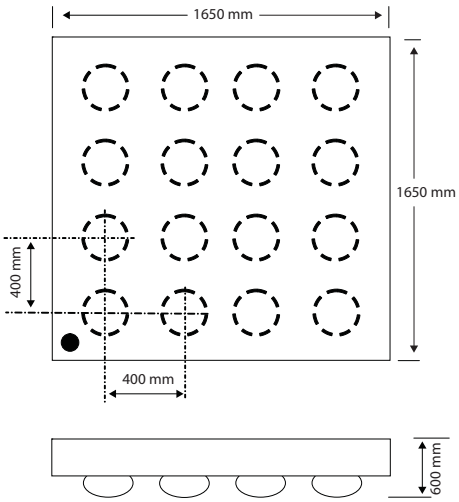
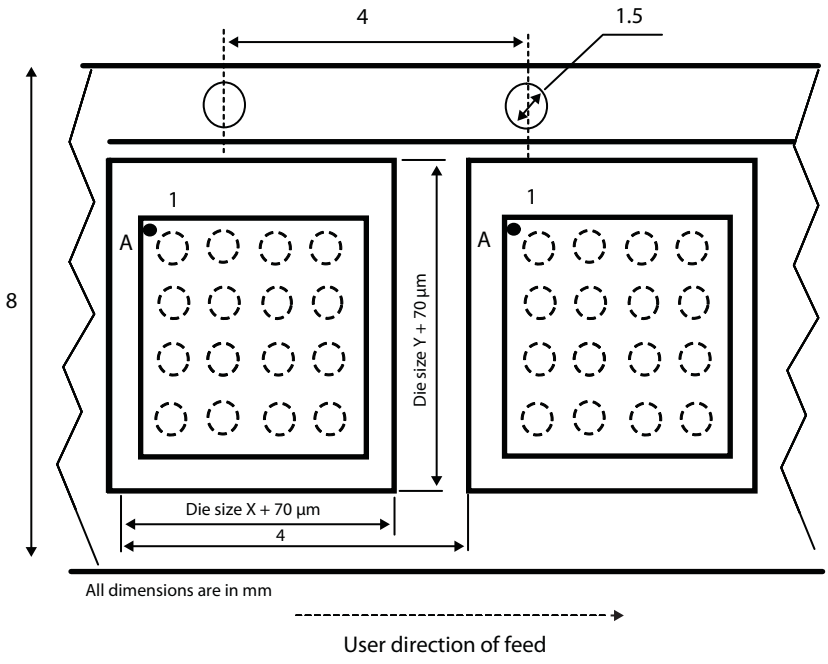



**Figure 78. Flip-chip - 16 bumps**




- Die size: 1.65 mm x 1.65 mm ± 30 µm
- Die height (including bumps): 600 µm ±55 µm
- Bump diameter: 250 µm ±40 µm
- Bump height: 205 µm ±35 µm
- Die height: 395 µm ±20 µm
- Pitch: 400 µm ±40 µm
- Coplanarity: 50 µm max

**Figure 79. Device orientation in tape pocket**



# 6 Ordering information

Table 12. Order codes

| Order code | Temperature range | Package | Packing | Marking |
|---|---|---|---|---|
| A22H165MJ | -40°C to +85°C | Flip-chip | Tape & reel | 21 |

# 7 Revision history

Table 13. Document revision history

| Date | Revision | Changes |
|---|---|---|
| 06-Mar-2014 | 1 | Initial release. |
| 03-Aug-2020 | 2 | Updated order code in *Table 12*. |

**IMPORTANT NOTICE – PLEASE READ CAREFULLY**

STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. For additional information about ST trademarks, please refer to *www.st.com/trademarks*. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

# X-ON Electronics

Largest Supplier of Electrical and Electronic Components

***Click to view similar products for*** Audio Amplifiers ***category:***

***Click to view products by*** STMicroelectronics ***manufacturer:***

Other Similar products are found below :

LV47002P-E NCP2811AFCT1G NCP2890AFCT2G SSM2377ACBZ-R7 IS31AP4915A-QFLS2-TR NCP2820FCT2G TDA1591T TDA7563AH SSM2529ACBZ-R7 SSM2518CBZ-R7 MAX9890AETA+T TS2012EIJT NCP2809BMUTXG NJW1157BFC2 SSM2375CBZ-REEL7 IS31AP4996-GRLS2-TR STPA002OD-4WX NCP2823BFCT1G MAX9717DETA+T MAX9717CETA+T MAX9724AEBC+TG45 LA4450L-E IS31AP2036A-CLS2-TR MAX9723DEBE+T TDA7563ASMTR AS3561-DWLT SSM2517CBZ-R7 MP1720DH-12-LF-P SABRE9601K THAT1646W16-U MAX98396EWB+ PAM8965ZLA40-13 BD37532FV-E2 BD5638NUX-TR BD37512FS-E2 BD37543FS-E2 BD3814FV-E2 TPA3140D2PWPR TS2007EIJT IS31AP2005-DLS2-TR SSM2518CPZ-R7 AS3410-EQFP-500 FDA4100LV MAX98306ETD+T TS4994EIJT NCP2820FCT1G NCP2823AFCT2G NCS2211MNTXG CPA2233CQ16-A1 OPA1604AIPWR