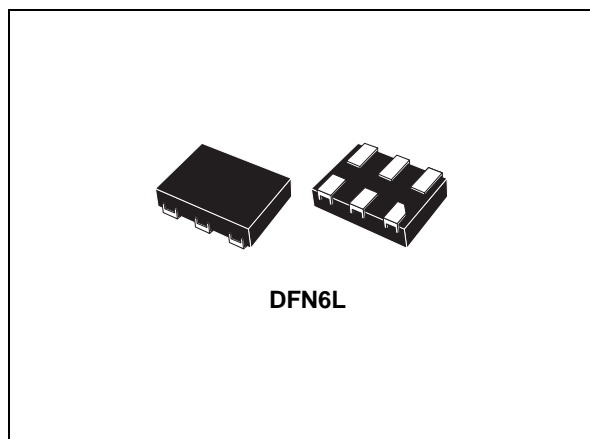


Low voltage 1 Ω single-pole double-throw analog switch with break-before-make feature

Datasheet - production data



Description

The AS11P2TLR is a high speed CMOS low voltage single analog SPDT (single-pole double-throw) switch or 2:1 multiplexer/demultiplexer switch manufactured using silicon gate C²MOS technology. Designed to operate from a 1.65 to 4.5 V supply, this device is ideal for portable applications.

The device offers very low ON-resistance (1 Ω) at $V_{CC} = 4.5$ V. Switch S1 is ON (connected to common ports Dn) when the SEL input is held high, and OFF (state of high impedance exists between the two ports) when SEL is held low.

Switch S2 is ON (connected to common port D) when the SEL input is held low, and OFF (state of high impedance exists between the two ports) when SEL is held high.

Additional key features are fast switching speed, break-before-make delay time and ultralow power consumption. All inputs and outputs are equipped with protection circuits to protect against static discharge, giving them immunity from ESD and transient excess voltage.

Features

- High speed:
 - $t_{PD} = 130$ ps (typ.) at $V_{CC} = 3.0$ V
 - $t_{PD} = 140$ ps (typ.) at $V_{CC} = 2.3$ V
- Ultra low power dissipation:
 - $I_{CC} = 0.2$ μ A (max.) at $T_A = 85$ °C
- Low ON resistance:
 - $R_{ON} = 1.0$ Ω (typ.) at $V_{CC} = 4.5$ V
 - $R_{ON} = 1.2$ Ω (typ.) at $V_{CC} = 3.0$ V
 - $R_{ON} = 2.0$ Ω (typ.) at $V_{CC} = 1.8$ V
- Wide operating voltage range:
 - V_{CC} (opr.) = 1.65 to 4.5 V single supply
- 5 V tolerant and 1.8 V compatible threshold ON digital control input at $V_{CC} = 1.65$ to 4.5 V
- Latch-up performance exceeds 200 mA per JESD 78, Class II
- ESD performance tested per JESD 22
 - 2000 V human-body model (A114-B, Class II)
 - 200 V machine model (A115-A)
- 1000 V charged-device model (C101)

Table 1. Device summary

Order code	Package	Packaging
AS11P2TLRQ	DFN6L (1.2 x 1 mm)	Tape and reel

Contents

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- 2 Electrical ratings 4**
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- 4 Test circuits 8**
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1 Pin connections and functions

Figure 1. Pin connections (top through view)

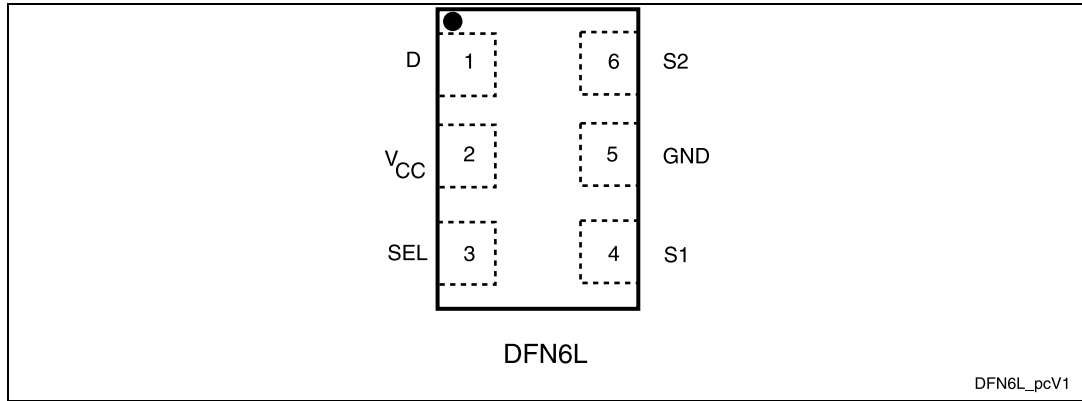


Table 2. Pin descriptions

Pin number	Symbol	Name and function
4	S1	Independent channel
6	S2	Independent channel
1	D	Common channels
3	SEL	Control
2	V _{CC}	Positive supply voltage
5	GND	Ground (0 V)

Figure 2. Input equivalent circuit

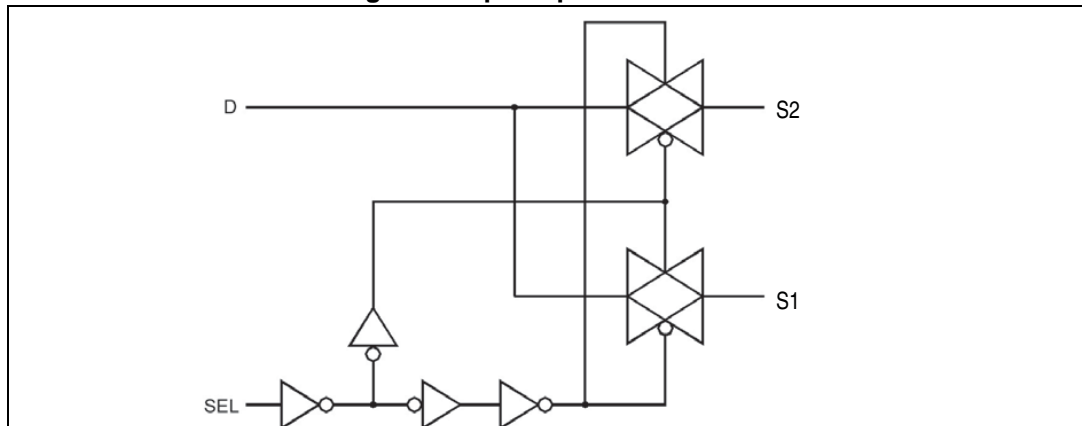


Table 3. Truth table

Sel	Switch S1	Switch S2
H	ON	OFF ⁽¹⁾
L	OFF ⁽¹⁾	ON

1. High impedance.

2 Electrical ratings

Stressing the device above the rating listed in [Table 4: Absolute maximum ratings](#) may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in [Table 5: Recommended operating conditions](#) of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics™ SURE program and other relevant quality documents.

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V _{CC}	Supply voltage	-0.5 to 5.5	V
V _I	DC input voltage	-0.5 to V _{CC} +0.5	V
V _{IC}	DC control input voltage	-0.5 to 5.5	V
V _O	DC output voltage	-0.5 to V _{CC} +0.5	V
I _{IKC}	DC input diode current on control pin (V _{SEL} < 0 V)	-50	mA
I _{IK}	DC input diode current (V _{IN} < 0 V)	±50	mA
I _{OK}	DC output diode current	±20	mA
I _O	DC output current	±200	mA
I _{OP}	DC output current peak (pulse at 1 ms, 10% duty cycle)	±400	mA
I _{CC} or I _{GND}	DC V _{CC} or ground current	±100	mA
P _D	Power dissipation at T _A = 70 °C ⁽¹⁾	1120	mW
T _{STG}	Storage temperature	-65 to 150	°C
T _L	Lead temperature (10 s)	300	°C

1. Derate above 70 °C by 18.5 mW/°C.

Table 5. Recommended operating conditions

Symbol	Parameter	Value	Unit
V _{CC}	Supply voltage	1.65 to 4.5	V
V _I	Input voltage	0 to V _{CC}	V
V _{IC}	Control input voltage	0 to 4.5	V
V _O	Output voltage	0 to V _{CC}	V
T _{op}	Operating temperature	-40 to 85	°C
dt/dv	Input rise and fall time control input	V _{CC} = 1.65 to 2.7 V	0 to 20
		V _{CC} = 3.0 to 4.5 V	0 to 10

3 Electrical characteristics

3.1 DC electrical characteristics

Table 6. DC specifications

Symbol	Parameter	V _{CC} (V)	Test condition	Value					Unit
				T _A = 25 °C			-40 to 85 °C		
				Min.	Typ.	Max.	Min.	Max.	
V _{IH}	High level input voltage	1.65 – 1.95		0.65 V _{CC}			0.65 V _{CC}		V
		2.3 – 2.5		1.2			1.2		
		2.7 – 3.0		1.3			1.3		
		3.3 – 3.6		1.4			1.4		
		4.5		1.6			1.6		
V _{IL}	Low level input voltage	1.65 – 1.95				0.40		0.40	V
		2.3 – 2.5				0.60		0.60	
		2.7 – 3.0				0.60		0.60	
		3.3 – 3.6				0.60		0.60	
		4.5				0.80		0.80	
R _{ON}	Switch ON-resistance	1.8	V _S = 0 V to V _{CC} I _S = 100 mA		2.0	3.0		3.5	Ω
		2.7			1.3	1.6		1.8	
		3.0			1.2	1.5		1.7	
		4.5			1.0	1.2		1.4	
ΔR _{ON}	ON-resistance match between channels ⁽¹⁾	1.8	V _S at R _{ON} max I _S = 100 mA		0.06				Ω
		2.7			0.05				
		3.0			0.05				
		4.5			0.05				
R _{FLAT}	ON-resistance flatness ⁽²⁾	1.8	V _S = 0 V to V _{CC} I _S = 100 mA		1.0	1.5		1.5	Ω
		2.7			0.45	0.60		0.70	
		3.0			0.43	0.50		0.60	
		4.5			0.39	0.50		0.60	
I _{OFF}	OFF state leakage current (Sn), (D)	4.3	V _S = 0.3 or 4 V			±20		±100	nA
I _{IN}	Input leakage current	0 – 4.5	V _{SEL} = 0 to 4.5 V			±0.1		±1.0	μA
I _{CC}	Quiescent supply current	1.65 – 4.5	V _{SEL} = V _{CC} or GND			±0.1		±1.0	μA

Table 6. DC specifications (continued)

Symbol	Parameter	V _{CC} (V)	Test condition	Value					Unit
				T _A = 25 °C			-40 to 85 °C		
				Min.	Typ.	Max.	Min.	Max.	
I _{CCLV}	Quiescent supply current low voltage driving	4.3	V _{SEL} = 1.65 V		±17	±35		±70	μA
		4.3	V _{SEL} = 1.80 V		±15	±30		±60	
		4.3	V _{SEL} = 2.60 V		±5	±10		±20	

1. $\Delta R_{ON} = R_{ON(Max)} - R_{ON(Min)}$
2. Flatness is defined as the difference between the maximum and minimum value of ON-resistance as measured over the specified analog signal ranges.

3.2 AC electrical characteristics

Table 7. AC electrical characteristics (C_L = 35 pF, R_L = 50 Ω, t_r = t_f ≤ 5 ns)

Symbol	Parameter	V _{CC} (V)	Test conditions	Value					Unit
				T _A = 25 °C			- 40 to 85 °C		
				Min.	Typ.	Max.	Min.	Max.	
t _{PLH} , t _{PHL}	Propagation delay	1.65 – 1.95			0.15				ns
		2.3 – 2.7			0.14				
		3.0 – 3.3			0.13				
		3.6 – 5.0			0.13				
t _{ON}	Turn-ON time	1.65 – 1.95	V _S = 0.8 V		36				ns
		2.3 – 2.7	V _S = 1.5 V		31	40		45	
		3.0 – 3.3			24	31		40	
		3.6 – 5.0			21	28		32	
t _{OFF}	Turn-OFF time	1.65 – 1.95	V _S = 0.8 V		29				ns
		2.3 – 2.7	V _S = 1.5 V		17	27		37	
		3.0 – 3.3			12	23		33	
		3.6 – 5.0			11	21		31	
t _D	Break-before-make time delay	1.65 – 1.95	C _L = 35 pF R _L = 50 Ω V _S = 1.5 V		15				ns
		2.3 – 2.7			10				
		3.0 – 3.3			8				
		3.6 – 5.0			6				
Q	Charge injection	1.65	C _L = 100 pF V _{GEN} = 0 V R _{GEN} = 0 Ω		16				pC
		2.3			22				
		3			26				
		5.0			33				



3.3 Analog switch characteristics

Table 8. Analog switch characteristics ($C_L = 5 \text{ pF}$, $R_L = 50 \text{ } \Omega$, $T_A = 25 \text{ } ^\circ\text{C}$)

Symbol	Parameter	V_{CC} (V)	Test conditions	Value					Unit
				$T_A = 25 \text{ } ^\circ\text{C}$			$-40 \text{ to } 85 \text{ } ^\circ\text{C}$		
				Min.	Typ.	Max.	Min.	Max.	
OIRR	OFF isolation ⁽¹⁾	1.65 – 5.0	$V_S = 1 V_{RMS}$ $f = 100 \text{ kHz}$		– 75				dB
Xtalk	Crosstalk	1.6 – 5.0	$V_S = 1 V_{RMS}$ $f = 100 \text{ kHz}$		– 80				dB
THD	Total harmonic distortion	2.3 – 5.0	$R_L = 600 \text{ } \Omega$ $V_S = 2 V_{PP}$ $f = 20 \text{ Hz to } 20 \text{ kHz}$		0.03				%
BW	-3 dB bandwidth	1.65 – 5.0	$R_L = 50 \text{ } \Omega$		150				MHz
C_{IN}	Control pin input capacitance				6				pF
C_{ON}	Sn port capacitance when switch is enabled	3.3	$f = 1 \text{ MHz}$		52				
C_{OFF}	Sn port capacitance when switch is disabled	3.3	$f = 1 \text{ MHz}$		25				
C_D	D port capacitance when switch is enabled	3.3	$f = 1 \text{ MHz}$		50				

1. OFF isolation = $20 \log_{10} (V_D/V_S)$, V_D = output. V_S = input to OFF switch.

4 Test circuits

Figure 3. ON resistance

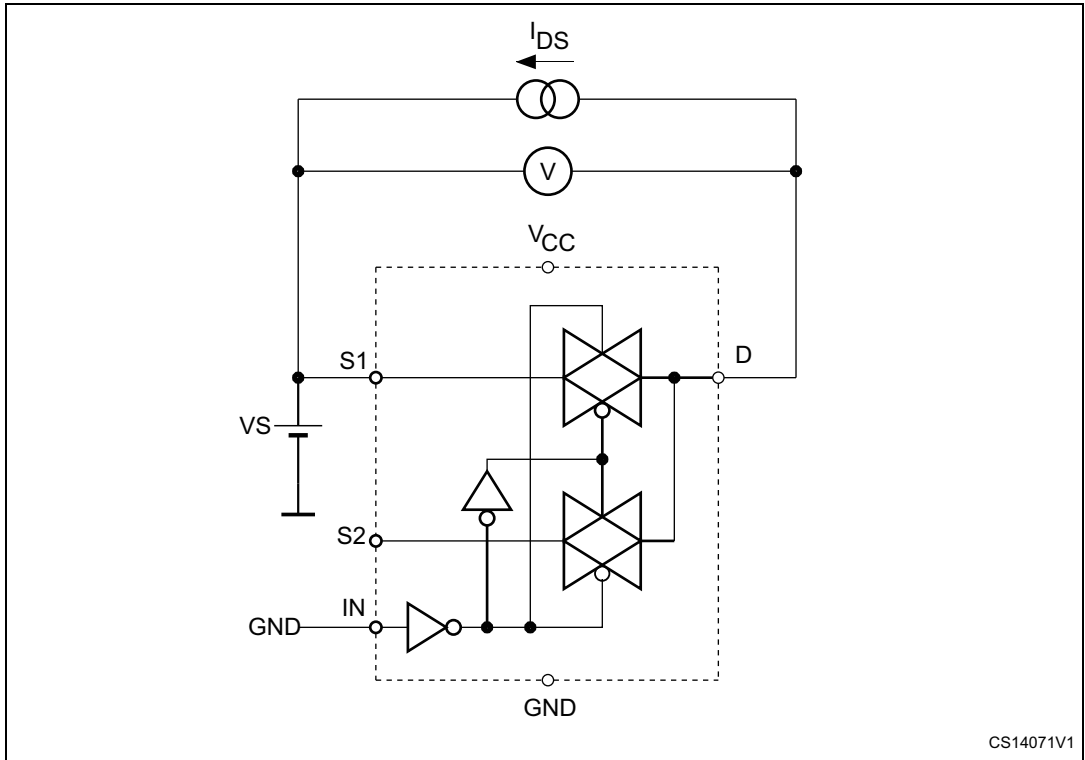


Figure 4. Bandwidth

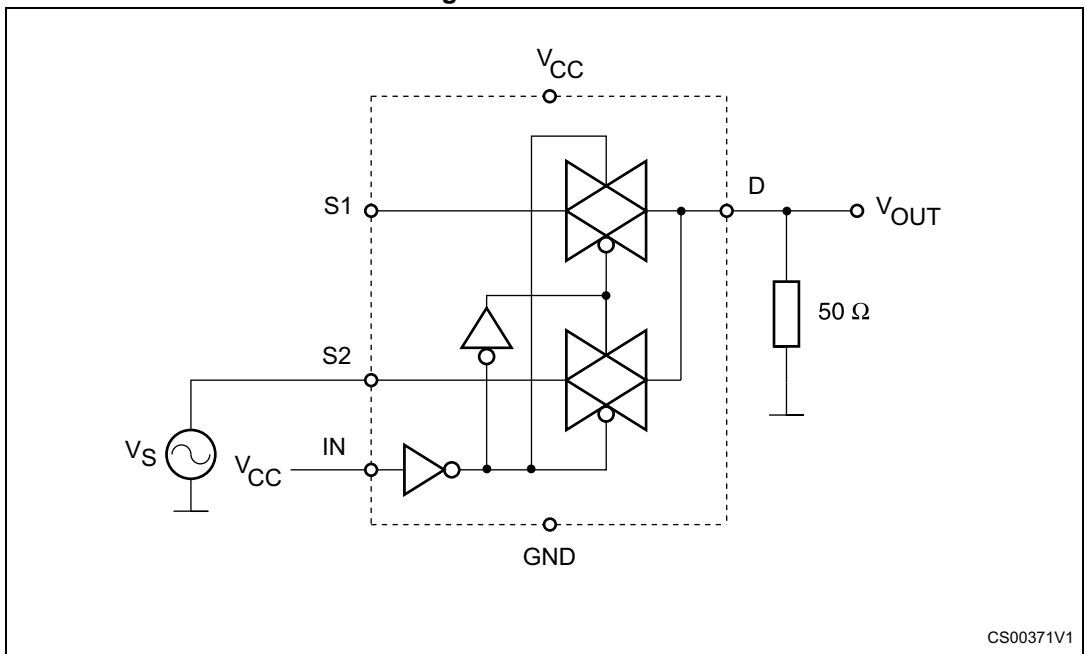


Figure 5. OFF leakage

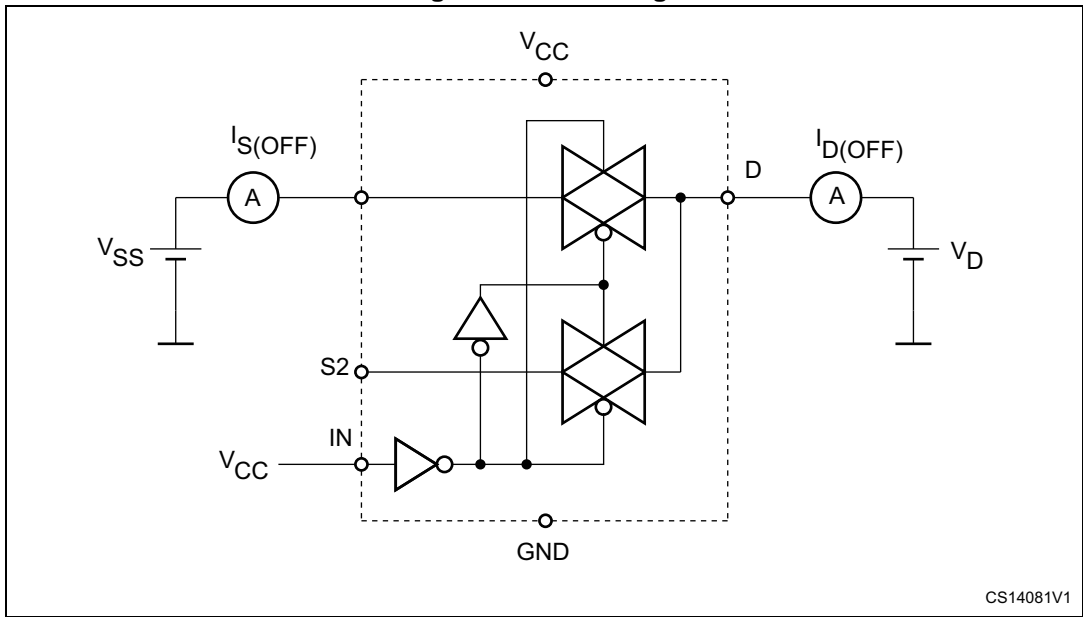


Figure 6. Channel-to-channel crosstalk

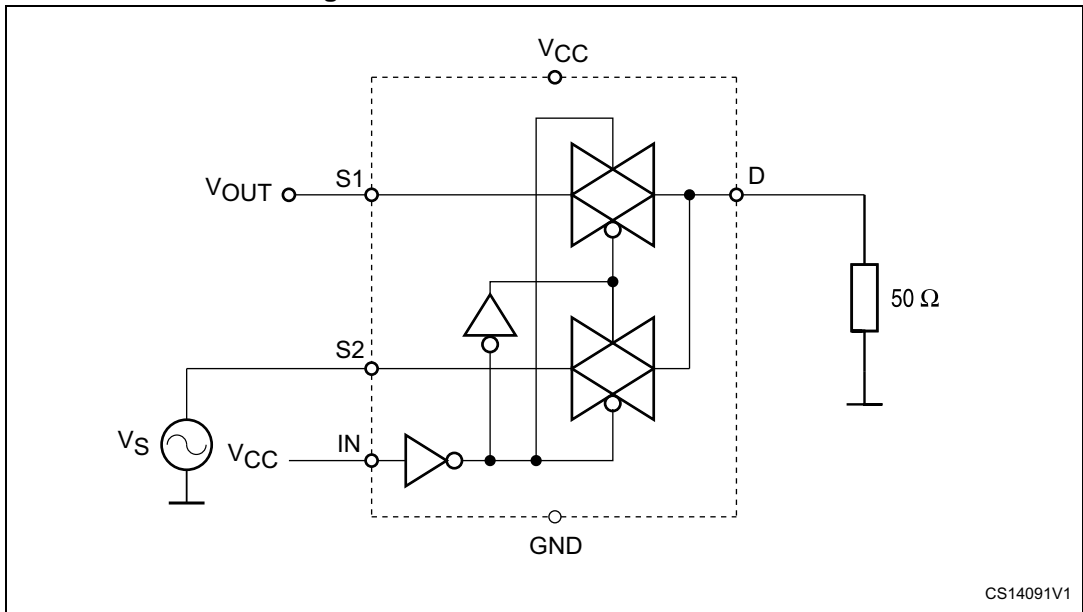
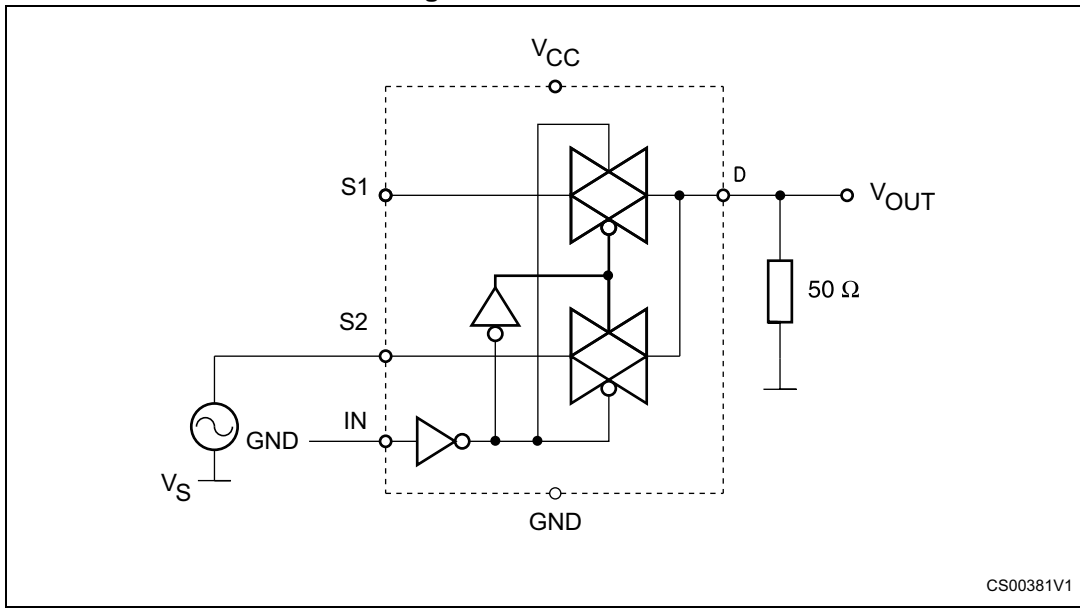
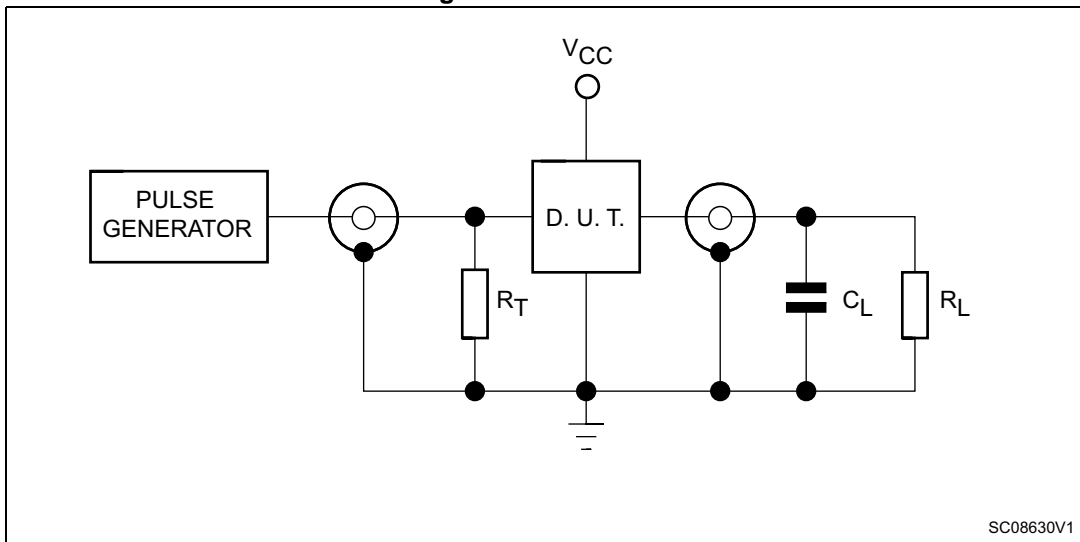


Figure 7. OFF isolation



CS00381V1

Figure 8. Test circuit



SC08630V1

1. $C_L = 5/35$ pF or equivalent: (includes jig capacitance).
2. $R_L = 50 \Omega$ or $\epsilon\theta\upsilon\iota\omega\lambda\epsilon\nu\tau$.
3. $R_T = Z_{OUT}$ of pulse generator (typically 50Ω).

Figure 9. Break-before-make time delay

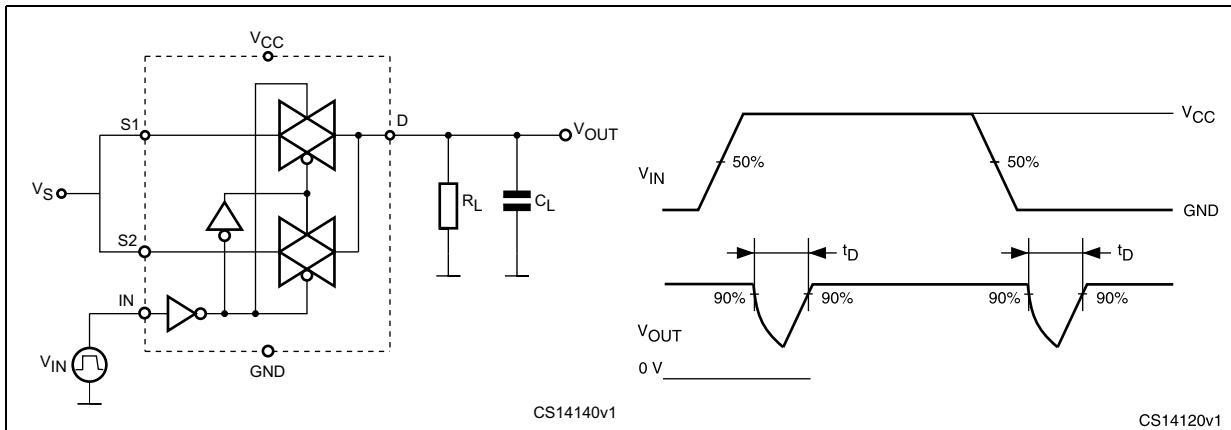


Figure 10. Switching time and charge injection ($V_{GEN} = 0\text{ V}$, $R_{GEN} = 0\ \Omega$, $R_L = 1\text{ M}\Omega$, $C_L = 100\text{ pF}$)

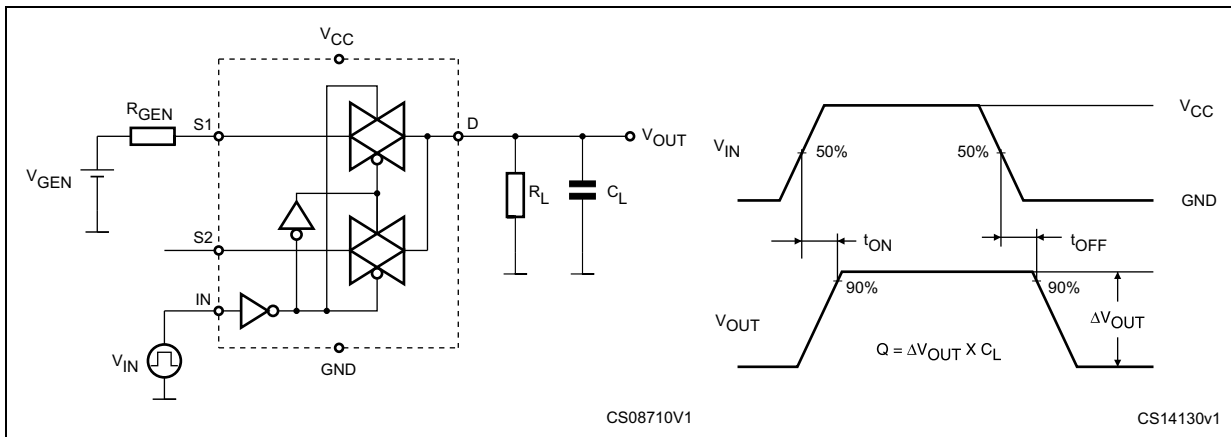
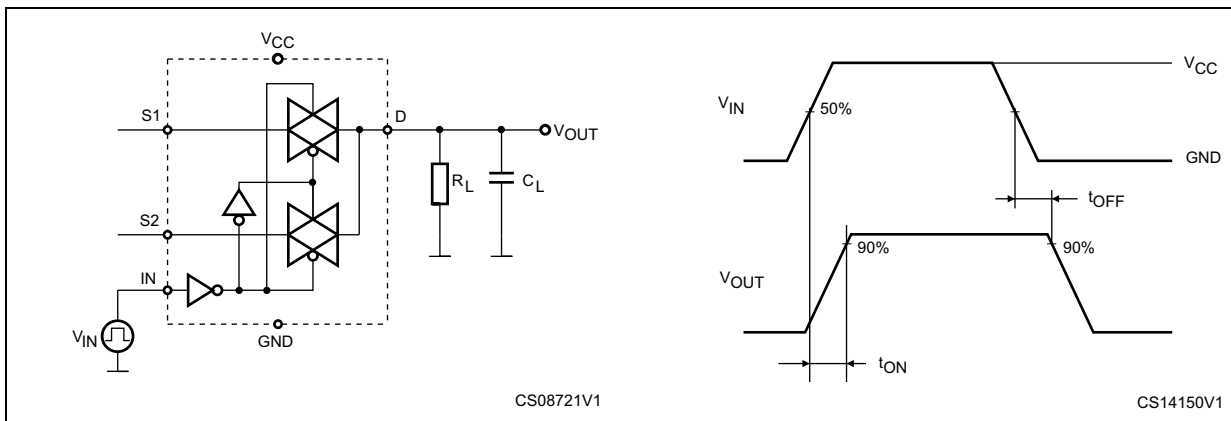


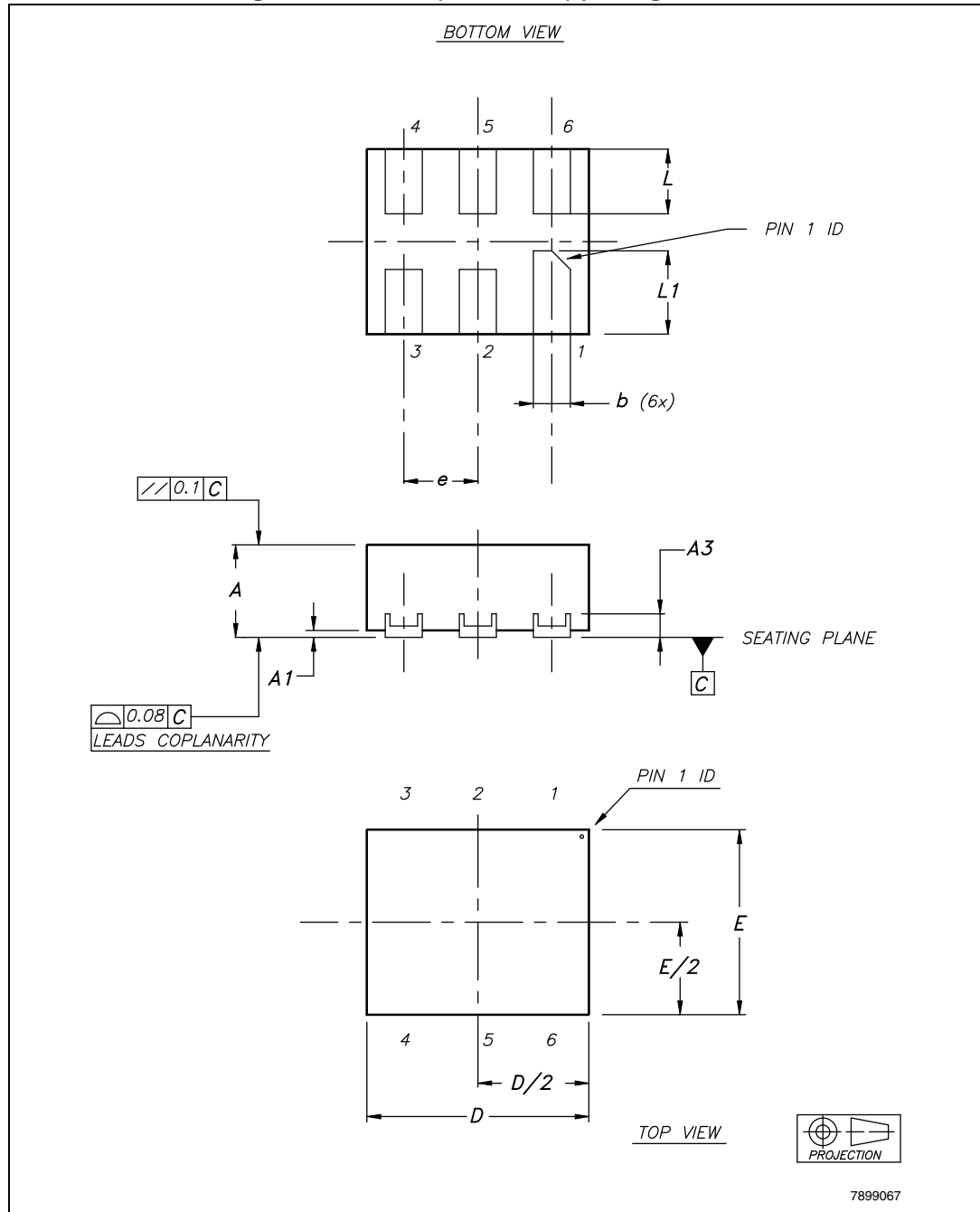
Figure 11. Turn-on, turn-off delay time



5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Figure 12. DFN6L (1.2 x 1 mm) package outline



1. Drawing is not to scale.

Table 9. DFN6L (1.2 x 1 mm) mechanical data

Symbol	Dimensions (millimeters)		
	Typ.	Min.	Max.
A	0.50	0.45	0.55
A1	0.02	0	0.05
A3	0.127		
b	0.20	0.15	0.25
D	1.20	1.15	1.25
E	1	0.95	1.05
e	0.40		
L	0.35	0.30	0.40
L1	0.45	0.40	0.50

Figure 13. DFN6L (1.2 x 1 mm) footprint recommendation

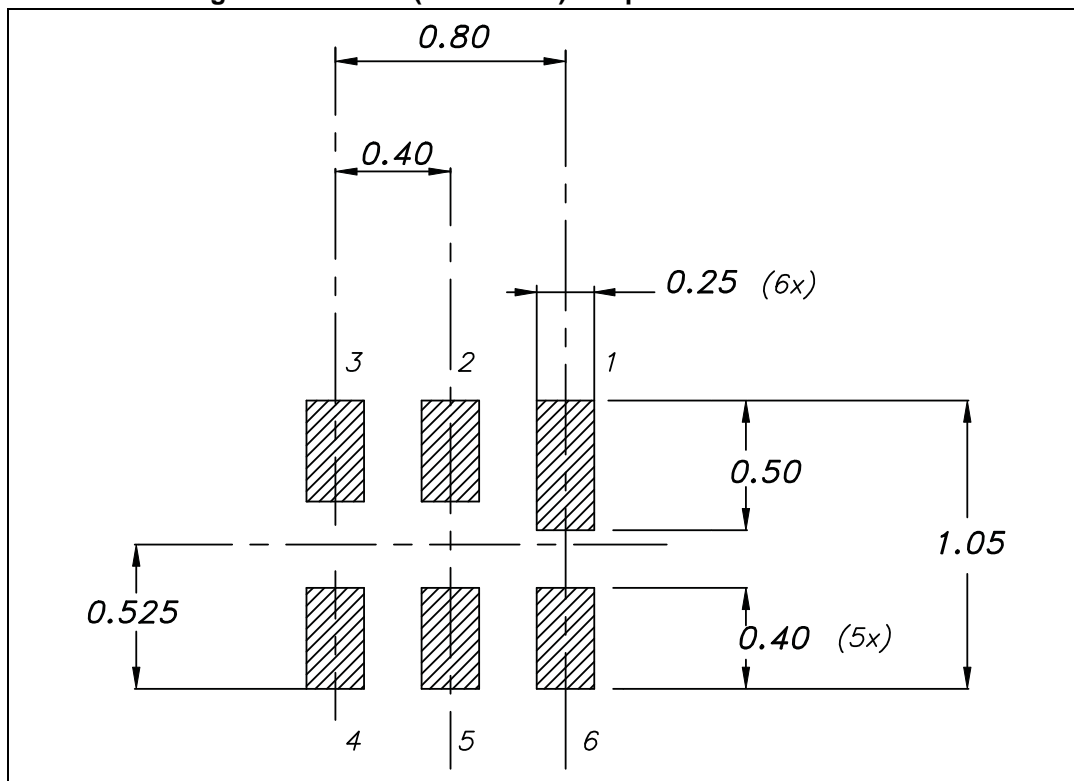
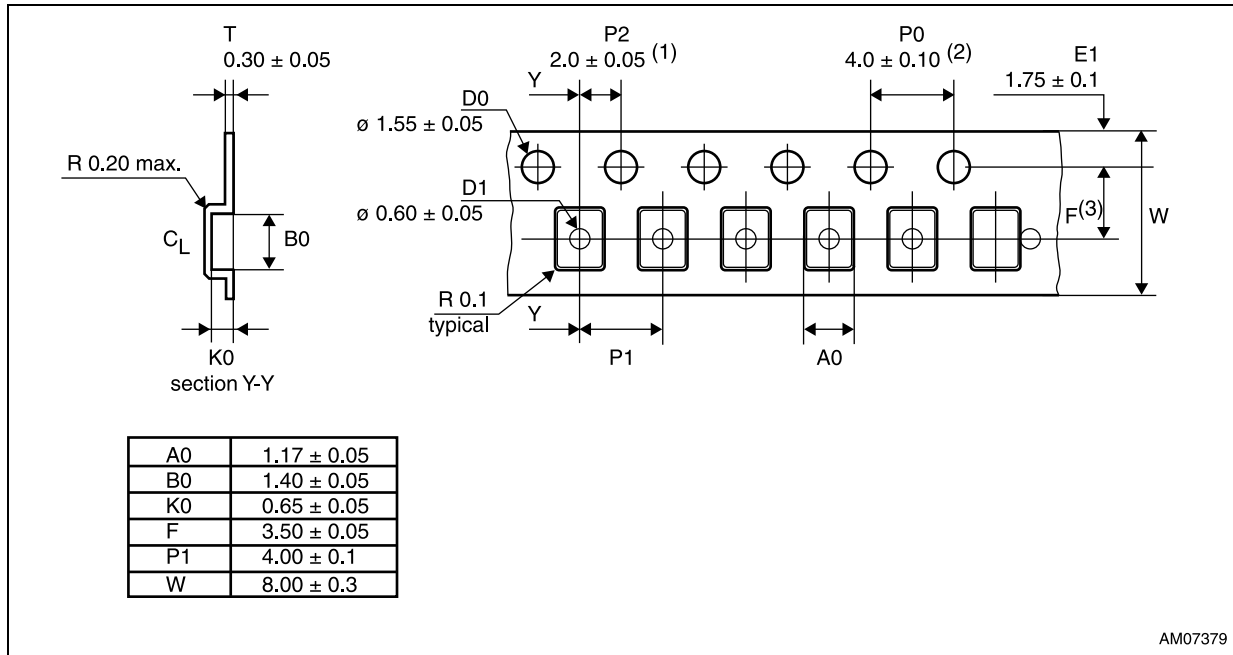
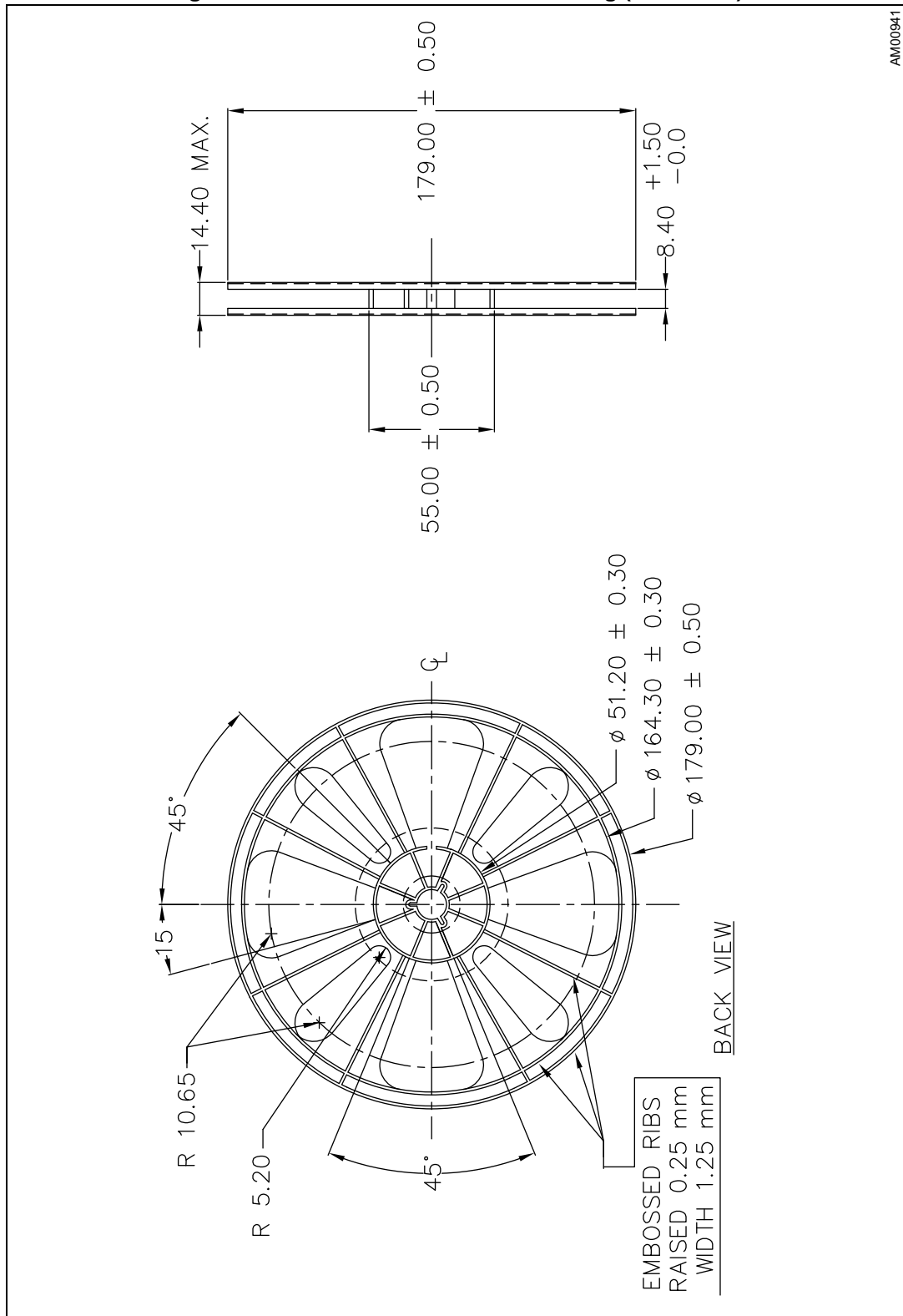


Figure 14. DFN6L carrier tape information



1. Measured from centreline of sprocket hole to centreline of pocket.
2. Cumulative tolerance of 10 sprocket holes is ± 0.20.
3. Measured from centreline of sprocket hole to centreline of pocket.
4. Other material available.
5. Drawing is not to scale.
6. All dimensions are in millimeters unless otherwise stated.

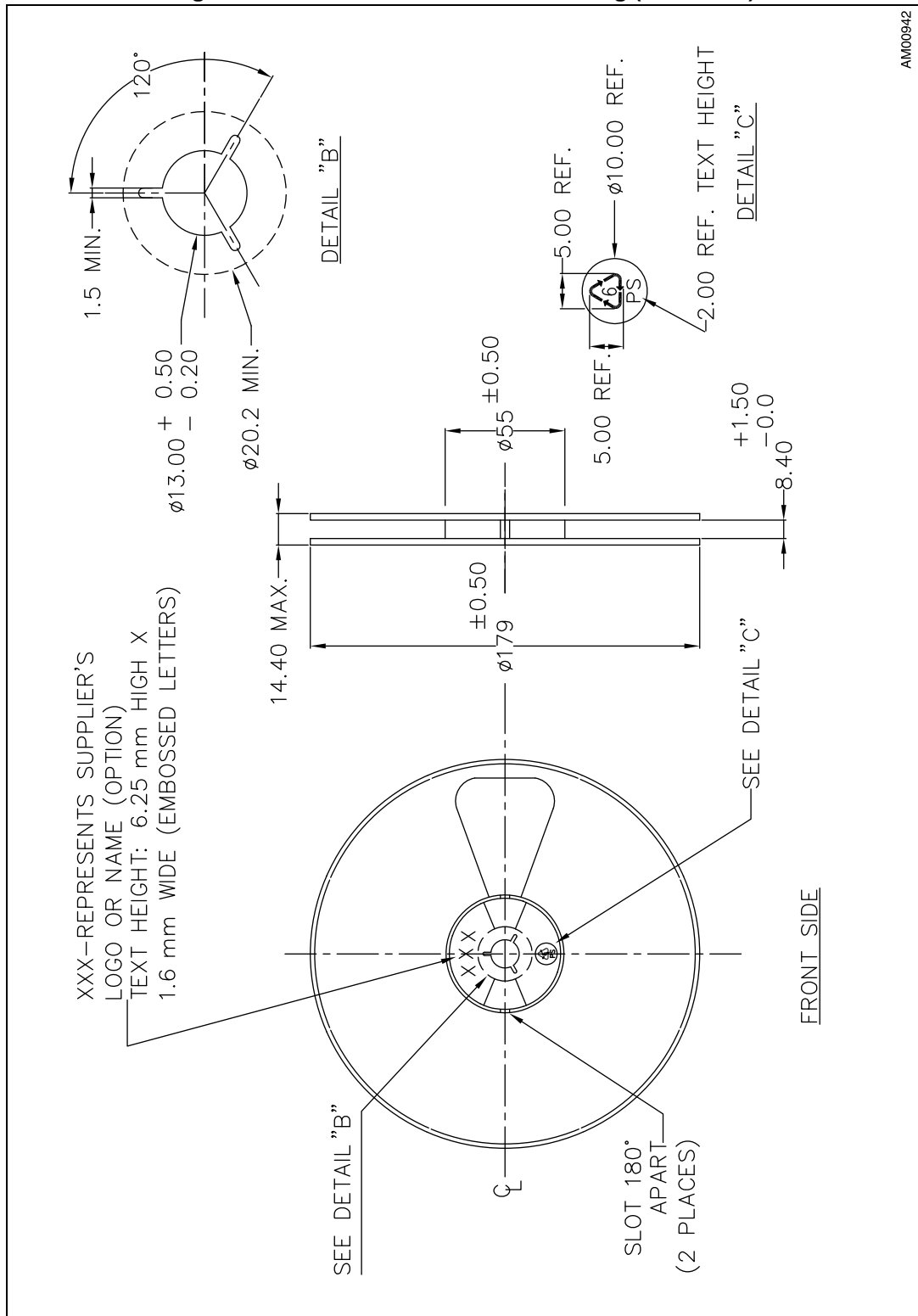
Figure 15. DFN6L reel information drawing (back view)



AM00941

1. Drawing is not to scale.
2. Dimensions are in millimeters.

Figure 16. DFN6L reel information drawing (front view)



AM00942

1. Drawing not to scale.
Dimensions are in millimeters.

6 Revision history

Table 10. Document revision history

Date	Revision	Changes
07-Mar-2014	1	Initial release.
08-Nov-2017	2	Updated order code AS11P2TLR with AS11P2TLRQ Table 1: Device summary.

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