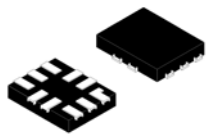
AS21P2TLR

Low voltage 0.5 Ω max dual single-pole double-throw analog switch with break-before-make

Datasheet - production data



(1.8 x 1.4 mm)

Features

- Ultra low power dissipation: I_{CC} = 0.2 µA (max.) at T_A = 85 °C
- Low ON resistance V_{IN} = 0 V:
  - R_{ON} = 0.50 Ω (max. T_A = 25 °C) at V_{CC} = 4.3 V
  - R_{ON} = 0.50 Ω (max. T_A = 25 °C) at V_{CC} = 3.6 V
- Wide operating voltage range: V_{CC} (OPR) = 1.65 to 4.3 V single supply
- 4.3 V tolerant and 1.8 V compatible threshold on digital control input at V_{CC} = 2.3 to 4.3 V
- Latch-up performance exceeds 300 mA (JESD 17)
- ESD performance: HMB > 2 kV (MIL STD 883 method 3015)

Description

The AS21P2TLR is a high-speed CMOS single-pole double-throw (SPDT) analog switch or dual 2:1 multiplexer/demultiplexer bus switch fabricated using silicon gate C²MOS technology. Designed to operate from 1.65 to 4.3 V, this device is ideal for portable applications.

It offers very low ON resistance (R_{ON} < 0.5 Ω) at V_{CC} = 3.6 V. The nIN inputs are provided to control the independent channel switches nS1 and nS2. The switches nS1 are ON (connected to common ports Dn) when the nIN input is held high and OFF (state of high impedance exists between the two ports) when nIN is held low. The switches nS2 are ON (connected to common ports Dn) when the nIN input is held low and OFF (state of high impedance exists between the two ports) when IN is held high. Additional key features are fast switching speed, break-before-make delay time and ultralow power consumption. All inputs and outputs are equipped with protection circuits against static discharge, giving them ESD and excess transient voltage immunity.

Table 1. Device summary

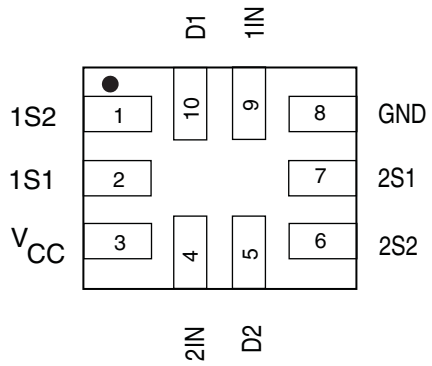
Order code	Package	Packing
AS21P2TLRQ	QFN10L (1.8 x 1.4 mm)	Tape and reel

Contents

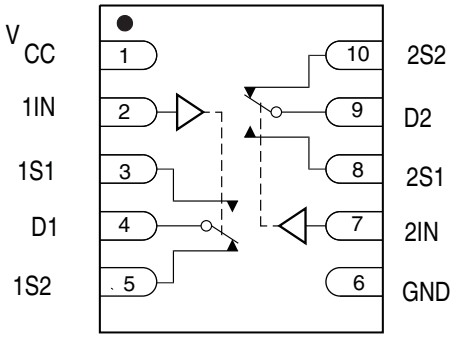
1 Pin settings

1.1 Pin connection

Figure 1. Pin connection (top through view)



QFN10L (1.8 x 1.4 mm)



DFN10L (2.3 x 2 mm)

1.2 Pin description

Table 2. Pin description

Pin number	Symbol	Name and function
1	1S2	Independent channel
2	1S1	Independent channel
3	V_{CC}	Positive voltage supply
4	2IN	Control
5	D2	Common channel
6	2S2	Independent channel
7	2S1	Independent channel
8	GND	Ground (0 V)
9	1IN	Control
10	D1	Common channel

Note: Exposed pad must be soldered to a floating plane. Do NOT connect to power or ground.

2 Input equivalent circuit and truth table

Figure 2. Input equivalent circuit

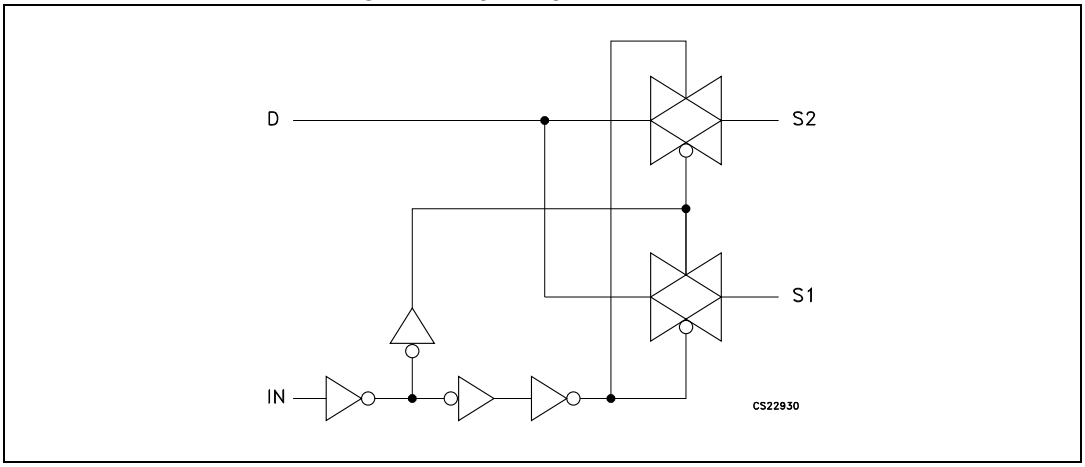


Table 3. Truth table

IN	Switch S1	Switch S2
H	ON	OFF(1)
L	OFF(1)	ON

1. High impedance.

3 Maximum rating

Stressing the device above the rating listed in the “Absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	-0.5 to 5.5	V
V_I	DC input voltage	-0.5 to V_{CC} + 0.5	V
V_{IC}	DC control input voltage	-0.5 to 5.5	V
V_O	DC output voltage	-0.5 to V_{CC} + 0.5	V
I_{IKC}	DC input diode current on control pin (V_{IN} < 0 V)	-50	mA
I_{IK}	DC Input diode current (V_{IN} < 0 V)	±50	mA
I_{OK}	DC output diode current	±20	mA
I_O	DC output current	±300	mA
I_{OP}	DC output current peak (pulse at 1 ms, 10% duty cycle)	±500	mA
I_{CC} or I_{GND}	DC V_{CC} or ground current	±100	mA
P_D	Power dissipation at T_A = 70 °C	1120	mW
T_{STG}	Storage temperature	-65 to 150	°C
T_L	Lead temperature (10 sec)	300	°C

Table 5. Recommended operating conditions

Symbol	Parameter		Value	Unit
V_{CC}	Supply voltage		1.65 to 4.3	V
V_I	Input voltage		0 to V_{CC}	V
V_{IC}	Control input voltage		0 to 4.3	V
V_O	Output voltage		0 to V_{CC}	V
T_{op}	Operating temperature		-40 to 85	°C
dt/dv	Input rise and fall time control input	V_{CC} = 1.65 to 2.7 V	0 to 20	ns/V
		V_{CC}= 3.0 to 4.3 V	0 to 10	

4 Electrical characteristics

Table 6. DC specifications

Symbol	Parameter	V_{CC} (V)	Test condition	Value					Unit
				T_A = 25 °C			-40 to 85 °C		
				Min	Typ	Max	Min	Max	
V_{IH}	High level input voltage	1.65 – 1.95		0.65 V_{CC}			0.65 V_{CC}		V
		2.3 – 2.5		1.2			1.2		
		2.7 – 3.0		1.3			1.3		
		3.0 – 3.6		1.4			1.4		
		4.3		1.5			1.5		
V_{IL}	Low level input voltage	1.65 – 1.95				0.25		0.25	V
		2.3 – 2.5				0.25		0.25	
		2.7 – 3.0				0.25		0.25	
		3.0 – 3.6				0.30		0.30	
		4.3				0.40		0.40	
R_{ON}	Switch ON resistance	4.3	V_S = 0 V to V_{CC} I_S = 100 mA		0.45	0.50		0.60	Ω
		3.6			0.45	0.50		0.60	
		3.0			0.50	0.55		0.60	
		2.3			0.60	0.70		0.80	
		1.8			0.80	0.9		1.0	
ΔR_{ON}	ON resistance match between channels[1],[2]	2.7	V_S = 1.5 V I_S = 100 mA		0.1				Ω
R_{FLAT}	ON resistance flatness [3]	4.3	V_S = 1.5 V I_S = 100 mA		0.15	0.20		0.20	Ω
		3.6			0.15	0.20		0.20	
		3.0			0.15	0.20		0.20	
		2.7			0.15	0.20		0.20	
		2.3			0.20	0.25		0.25	
		1.65			0.35	0.45		0.45	
I_{OFF}	OFF state leakage current (nSn), (Dn)	4.3	V_S = 0.3 or 4 V			±20		±100	nA
I_{IN}	Input leakage current	0 – 4.3	V_{IN} = 0 to 4.3 V			±0.05		±1	µA
I_{CC}	Quiescent supply current [1]	1.65 – 4.3	V_{IN} = V_{CC} or GND			±0.05		±0.2	µA

Table 6. DC specifications (continued)

Symbol	Parameter	V_{CC} (V)	Test condition	Value					Unit
				T_A = 25 °C			-40 to 85 °C		
				Min	Typ	Max	Min	Max	
I_{CCLV}	Quiescent supply current low voltage driving	4.3	V_{1IN}, V_{2IN} = 1.65 V		±37	±50		±100	µA
			V_{1IN}, V_{2IN} = 1.80 V		±33	±40		±50	
			V_{1IN}, V_{2IN} = 2.60 V		±12	±20		±30	

1. Guaranteed by design.
2. $\Delta R_{ON} = R_{ON(max)} - R_{ON(min)}$.
3. Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal ranges.

Table 7. AC electrical characteristics (C_L = 35 pF, R_L = 50 Ω, $t_r = t_f \leq$ 6 ns)

Symbol	Parameter	V_{CC} (V)	Test condition	Value					Unit
				T_A = 25 °C			-40 to 85 °C		
				Min	Typ	Max	Min	Max	
t_{PLH}, t_{PHL}	Propagation delay	1.65 – 1.95			0.45				ns
		2.3 – 2.7			0.40				
		3.0 – 3.3			0.30				
		3.6 – 4.3			0.30				
t_{ON}	Turn-ON time	1.65 – 1.95	V_S = 0.8 V		120				ns
		2.3 – 2.7	V_S = 1.5 V		65	85		90	
		3.0 – 3.3			42	55		65	
		3.6 – 4.3			40	55		65	
t_{OFF}	Turn-OFF time	1.65 – 1.95	V_S = 0.8 V		45				ns
		2.3 – 2.7	V_S = 1.5 V		18	30		40	
		3.0 – 3.3			16	30		40	
		3.6 – 4.3			15	30		40	
t_D	Break-before make time delay	1.65 – 1.95	C_L = 35 pF, R_L = 50 Ω, V_S = 1.5 V	2	80				ns
		2.3 – 2.7		2	60				
		3.0 – 3.3		2	55				
		3.6 – 4.3		2	50				

Table 7. AC electrical characteristics (C_L = 35 pF, R_L = 50 Ω, $t_r = t_f \leq$ 6 ns) (continued)

Symbol	Parameter	V_{CC} (V)	Test condition	Value					Unit
				T_A = 25 °C			-40 to 85 °C		
				Min	Typ	Max	Min	Max	
Q	Charge injection	1.65 – 1.95	C_L = 100 pF R_L = 1 MΩ V_{GEN} = 0 V R_{GEN} = 0 Ω		43				pC
		2.3 – 2.7			51				
		3.0 – 3.3			51				
		3.6 – 4.3			49				

Table 8. Analog switch characteristics (C_L = 5 pF, R_L = 50 Ω, T_A = 25 °C)

Symbol	Parameter	V_{CC} (V)	Test condition	Value					Unit
				T_A = 25 °C			-40 to 85 °C		
				Min	Typ	Max	Min	Max	
OIRR	Off isolation(1)	1.65 – 4.3	V_S = 1 V_{RMS} f = 100 kHz		-66				dB
Xtalk	Crosstalk	1.65 – 4.3	V_S = 1 V_{RMS} f = 100 kHz		-72				dB
THD	Total harmonic distortion	2.3 – 4.3	R_L = 600 Ω V_{IN} = 2V_{PP} f = 20 Hz to 20 kHz		0.02				%
BW	-3 dB bandwidth	1.65 – 4.3	R_L= 50 Ω		55				MHz
C_{IN}	Control pin input capacitance				5				pF
C_{Sn}	Sn port capacitance	3.3	f = 1 MHz		40				
C_D	D port capacitance when switch is enabled	3.3	f = 1 MHz		114				

1. Off Isolation = 20 Log_{10} (V_D/V_S), V_D = output. V_S = input at off switch.

5 Test circuit

Figure 3. ON resistance

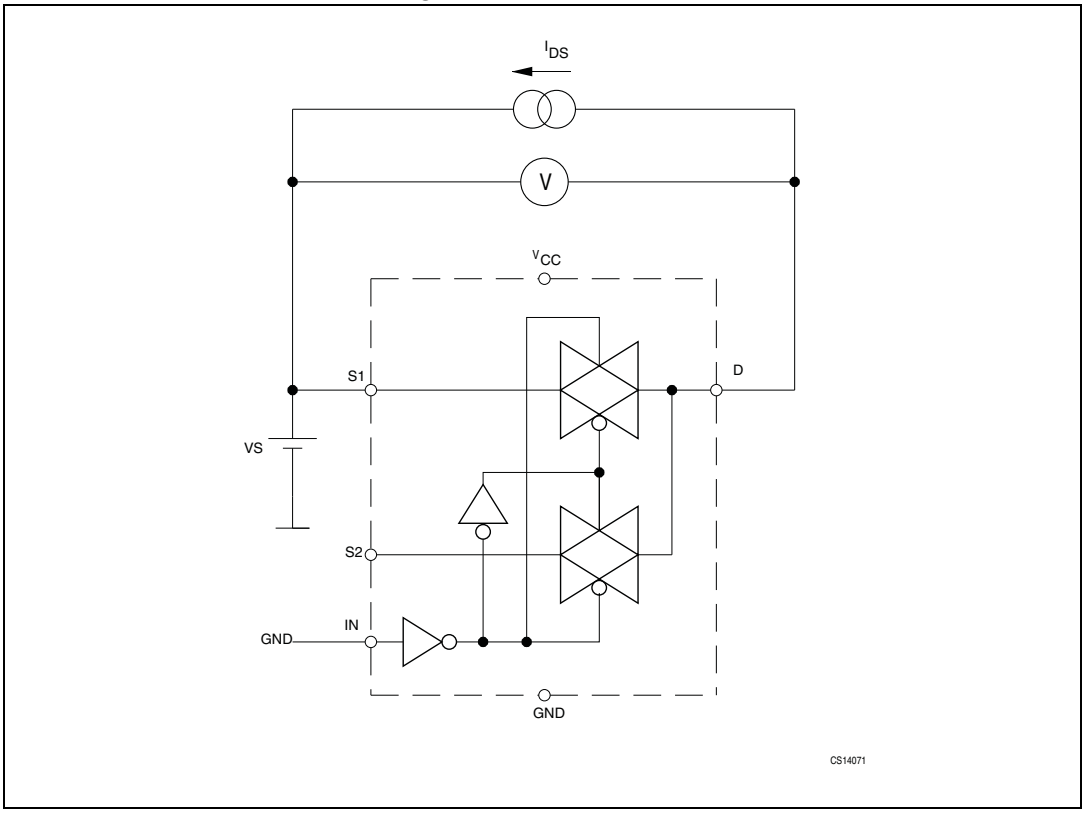


Figure 4. OFF leakage

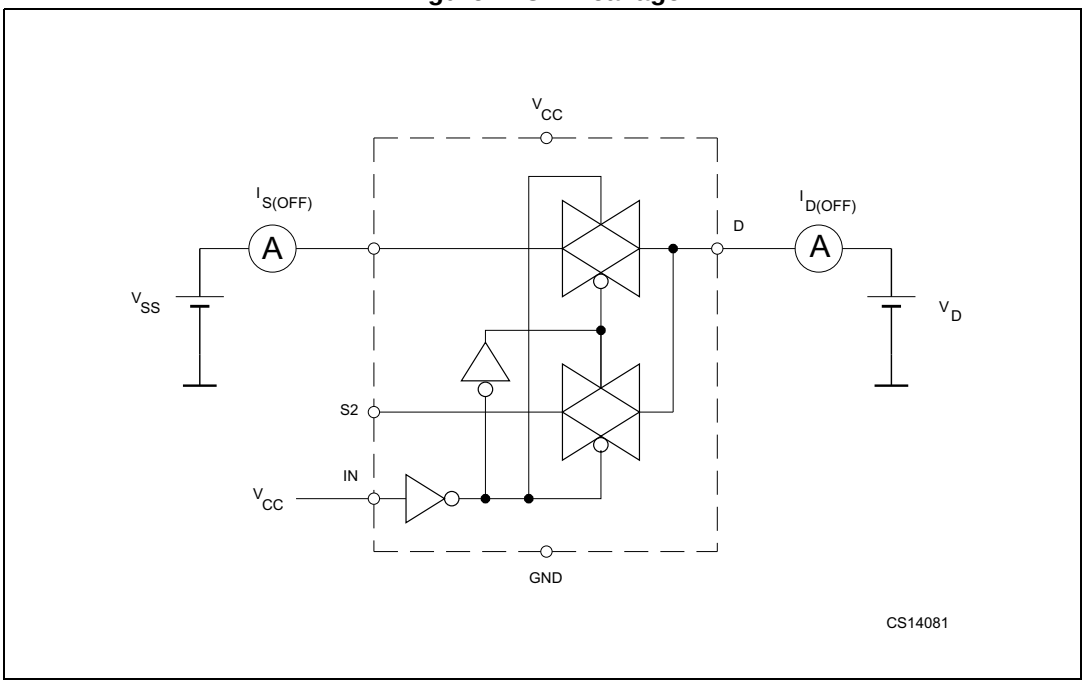


Figure 5. OFF isolation

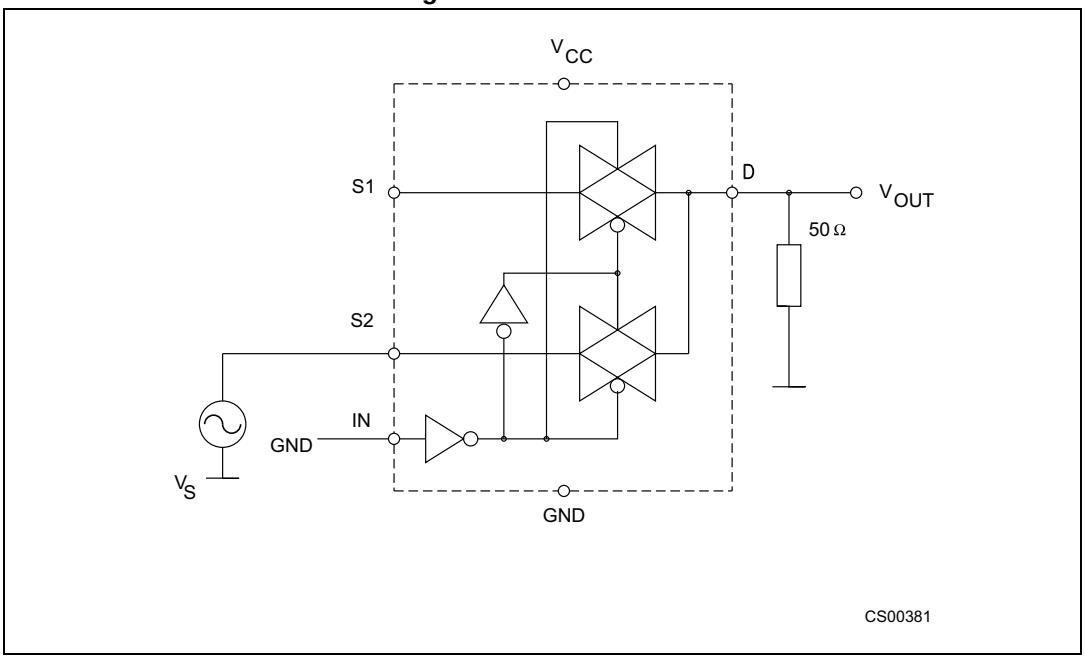


Figure 6. Bandwidth

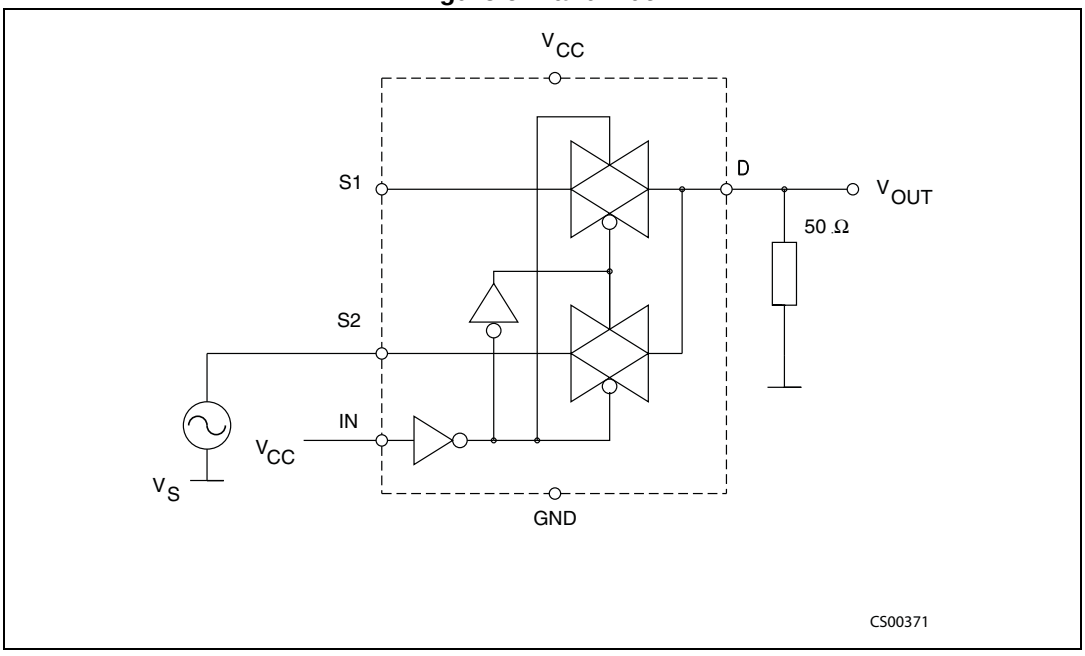


Figure 7. Channel-to-channel crosstalk

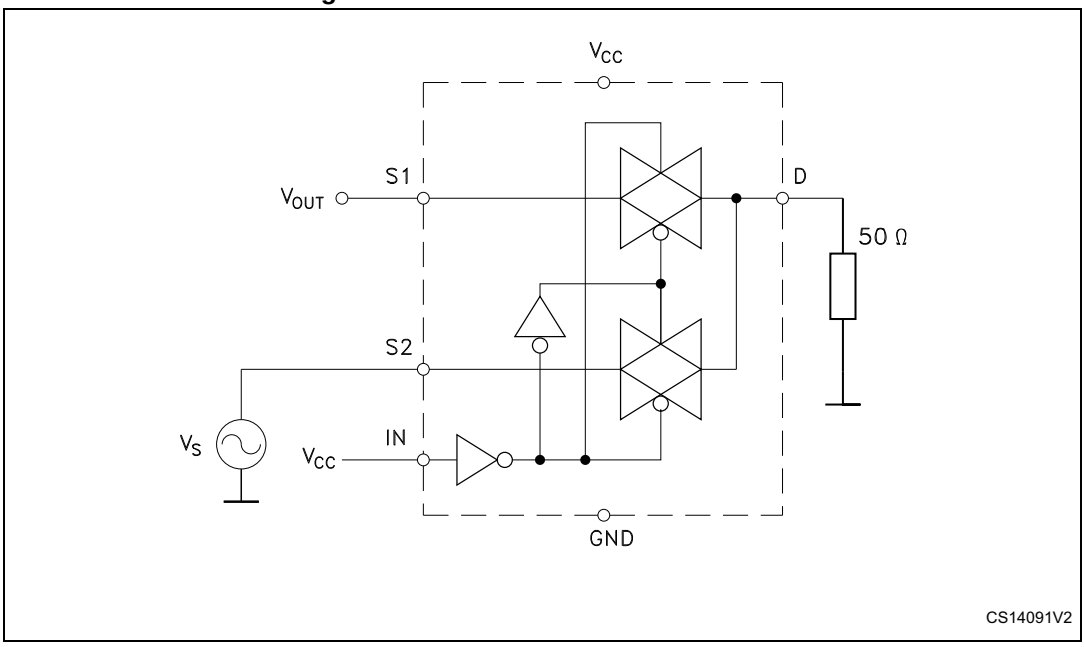
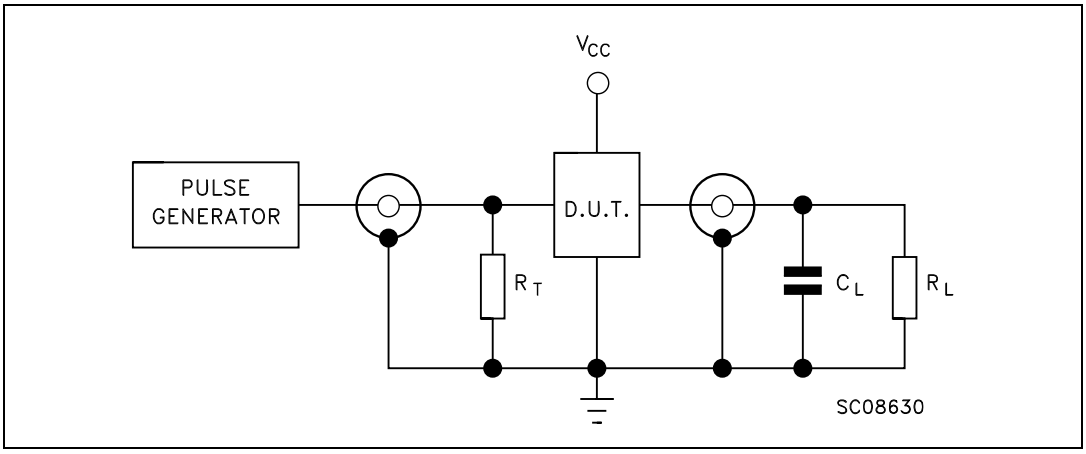


Figure 8. Test circuit



1. C_L = 5/35 pF or equivalent (includes jig and probe capacitance).
   R_L = 50 Ω or equivalent.
   R_T = Z_{OUT} of pulse generator (typically 50 Ω).

Figure 9. Break-before-make time delay

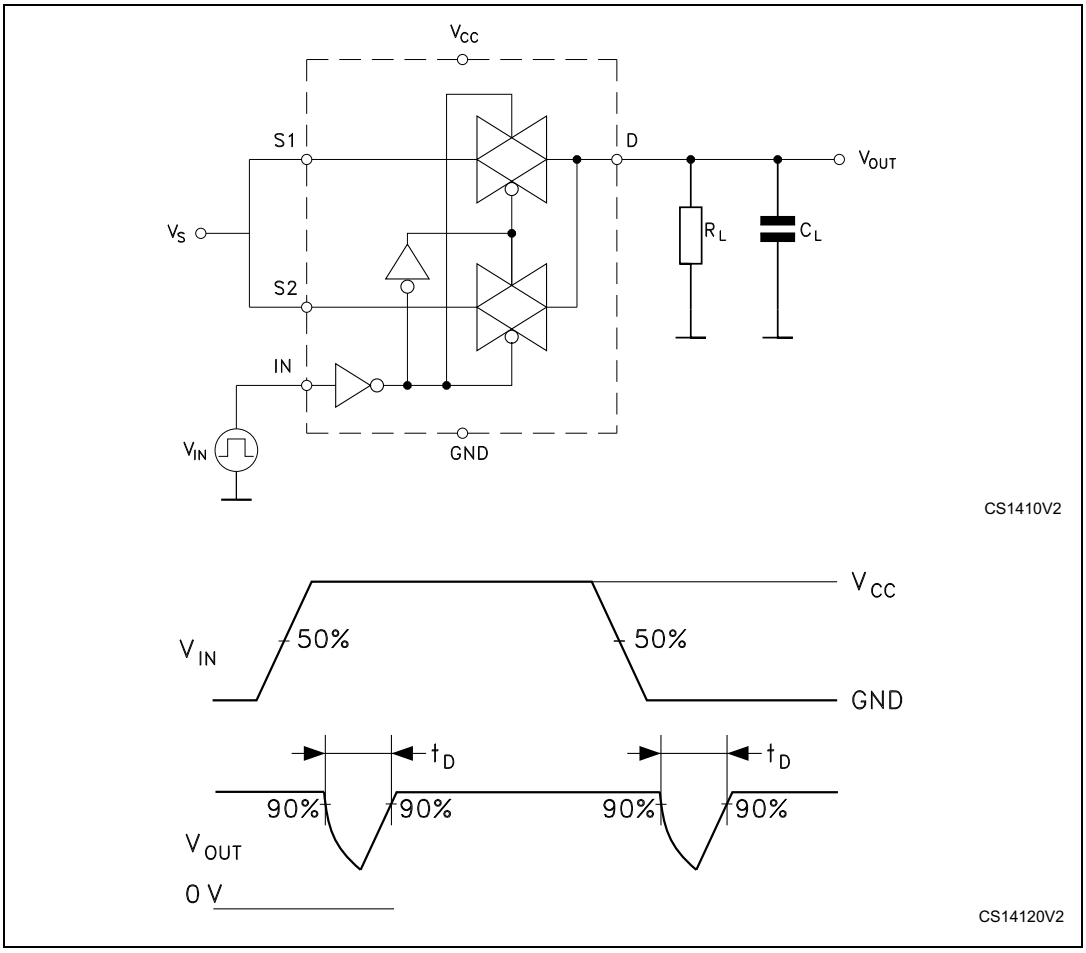


Figure 10. Charge injection (V_{GEN} = 0 V, R_{GEN} = 0 Ω, R_L = 1 MΩ, C_L = 100 pF)

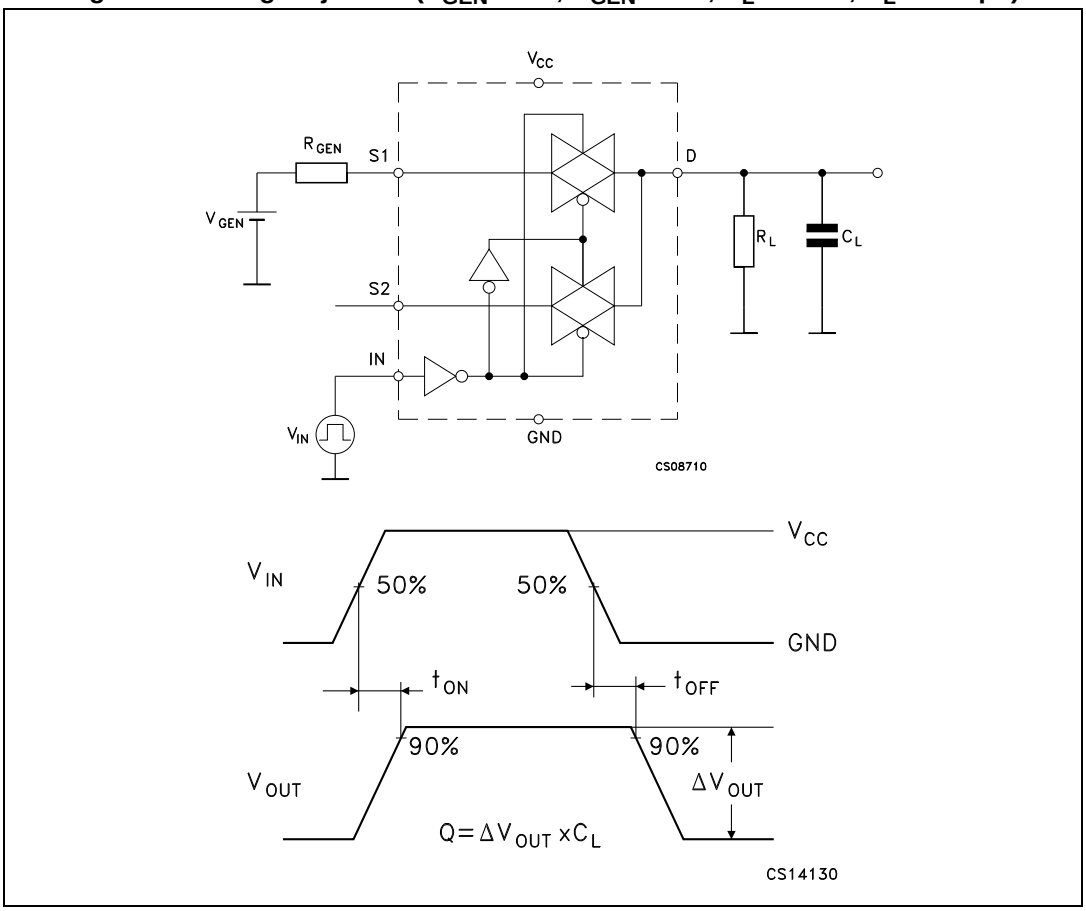
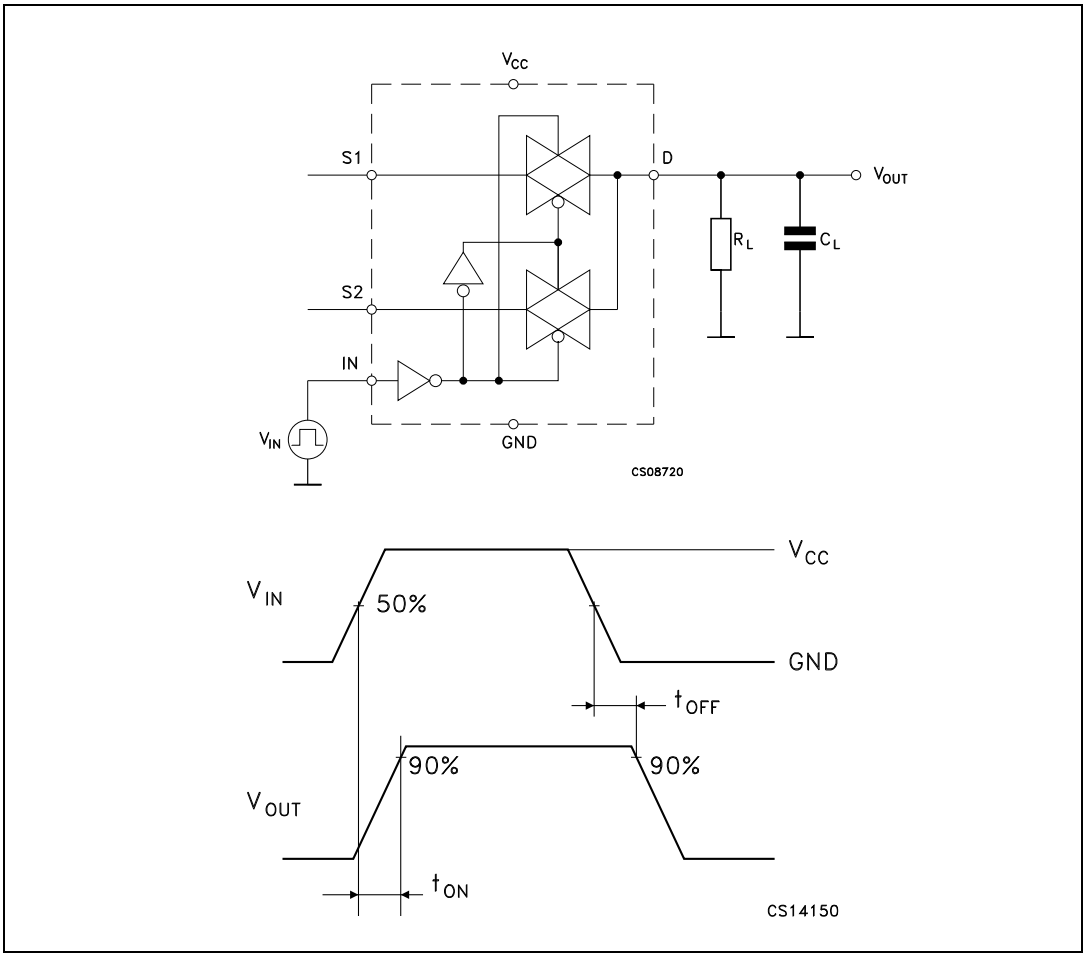


Figure 11. Turn-on, turn-off delay time



6 Package mechanical data

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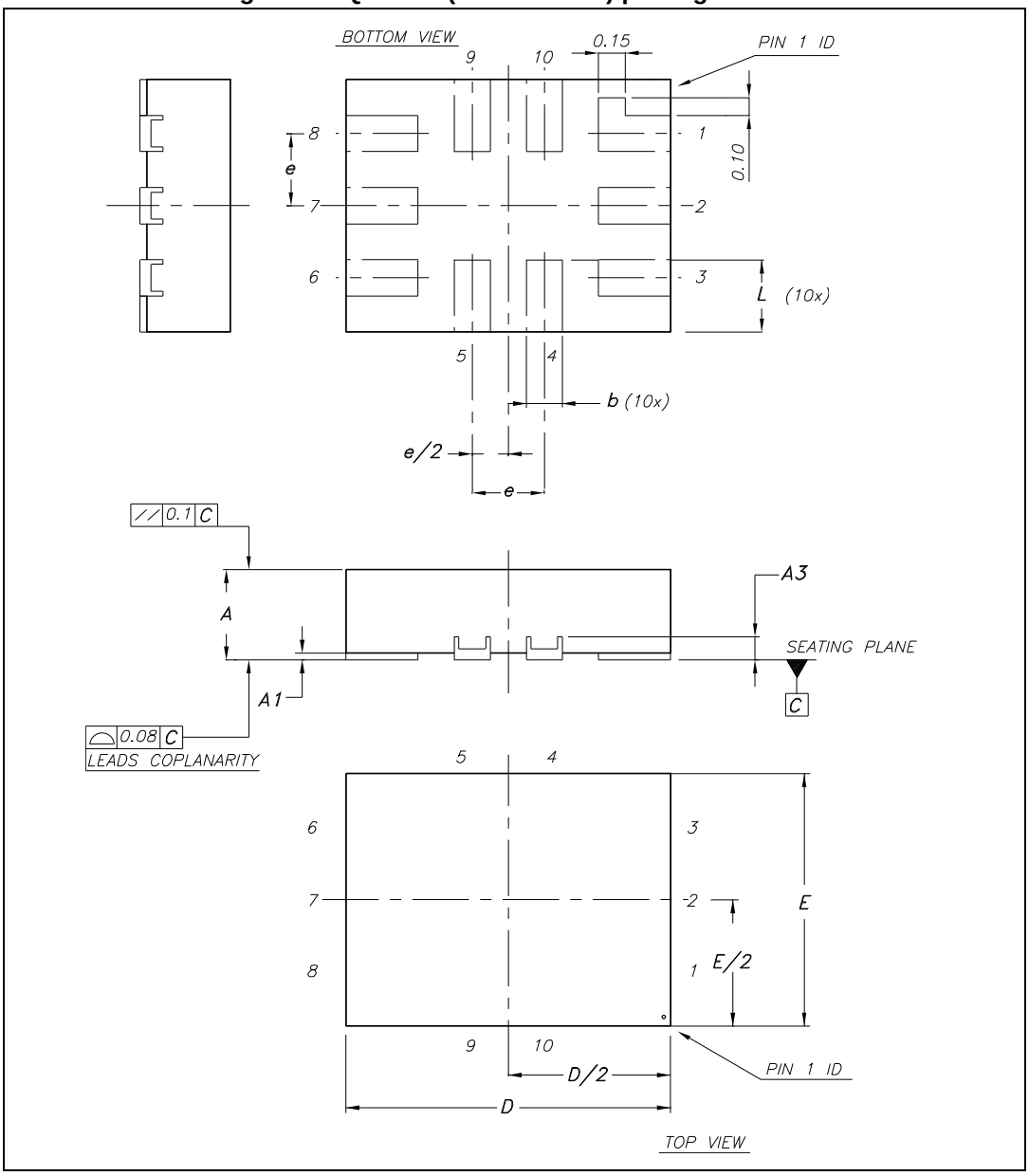
Figure 12. QFN10L (1.8 x 1.4 mm) package outline

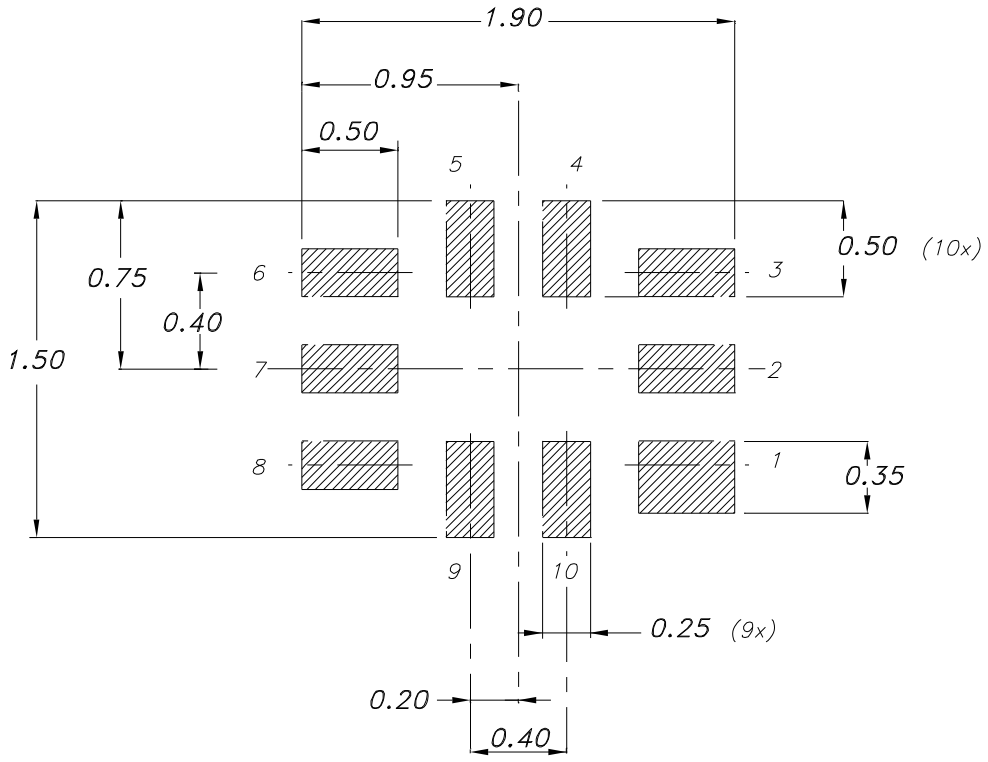


1. Drawing not to scale.

Table 9. QFN10L (1.8 x 1.4 mm) mechanical data

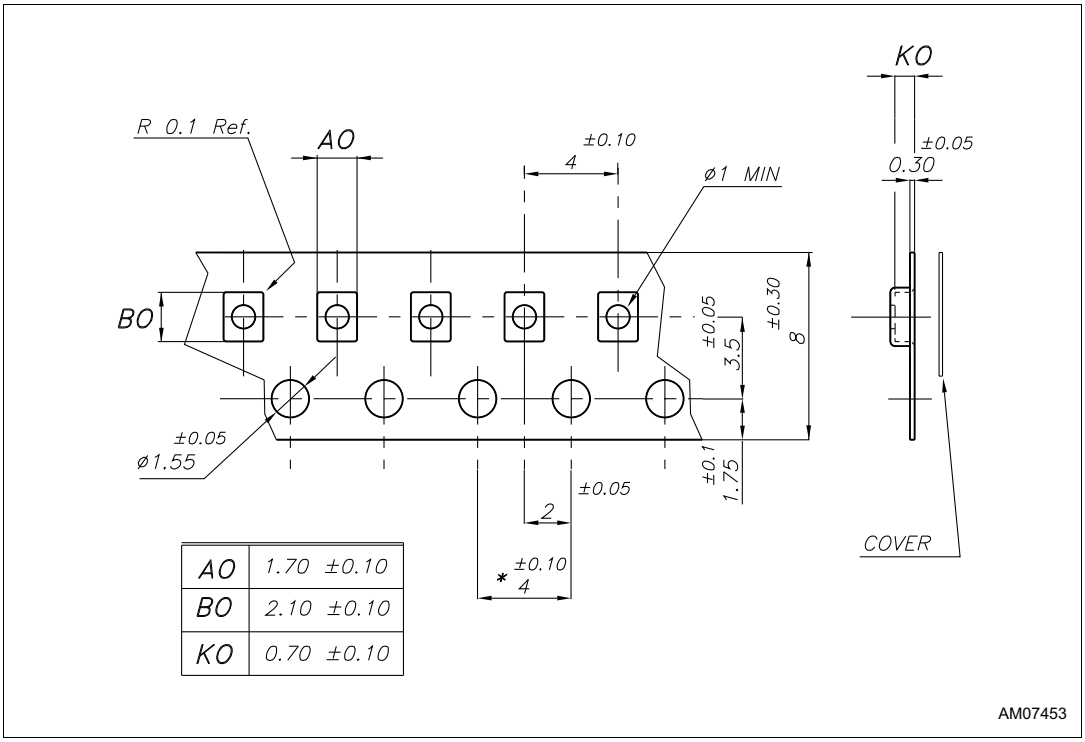
Symbol	millimeters			inches		
	Nom	Min	Max	Nom	Min	Max
A	0.50	0.45	0.55	0.020	0.017	0.021
A1	0.02	0	0.05	0.001	0	0.002
A3	0.127			0.005	0	0
b	0.20	0.15	0.25	0.007	0.006	0.010
D	1.80	1.70	1.90	0.070	0.066	0.074
E	1.40	1.30	1.50	0.055	0.051	0.059
e	0.40			0.015		
L	0.40	0.30	0.50	0.015	0.011	0.020

Figure 13. QFN10L (1.8 x 1.4 mm) footprint recommendations



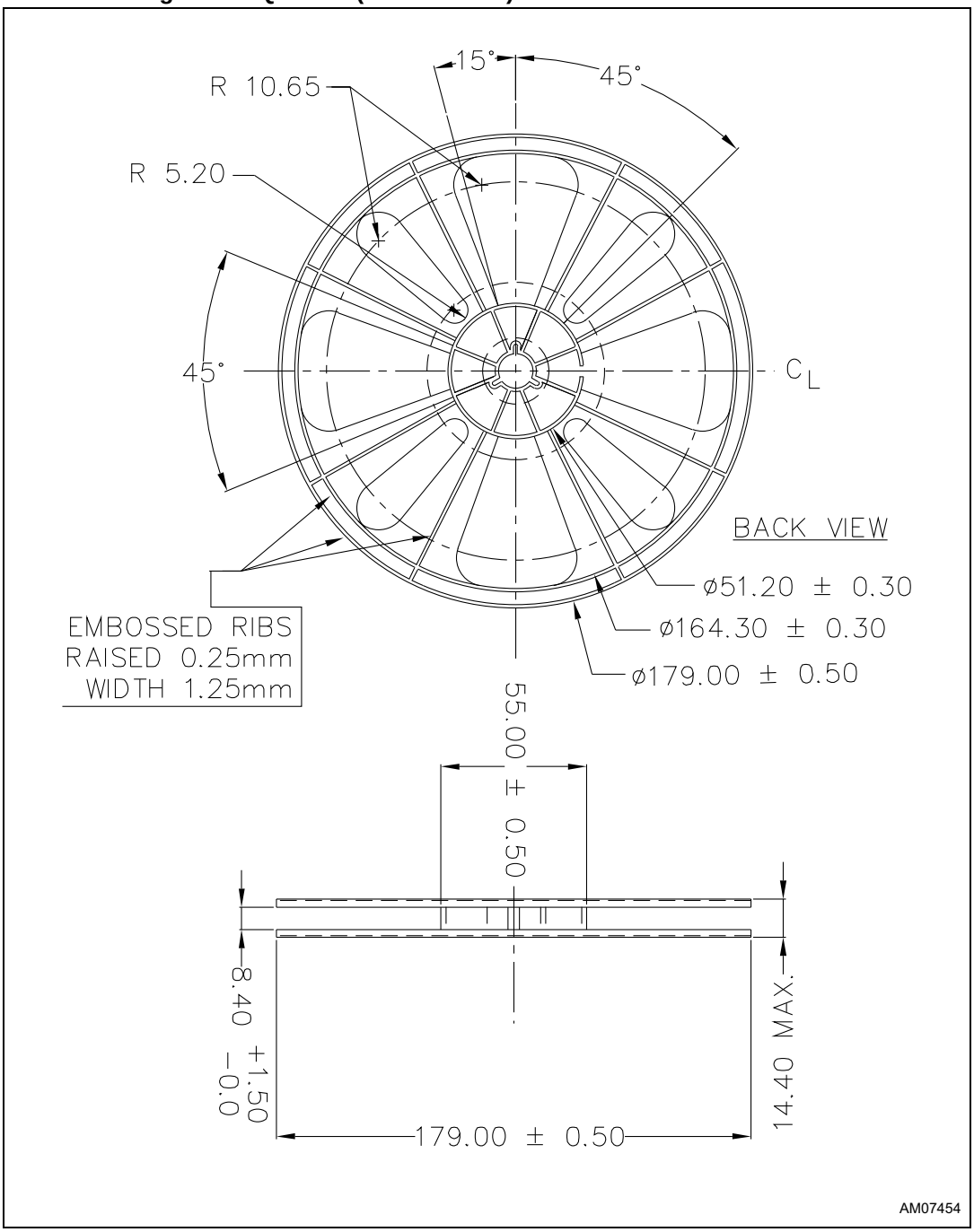
1. Drawing not to scale.

Figure 14. QFN10L (1.8 x 1.4 mm) carrier type



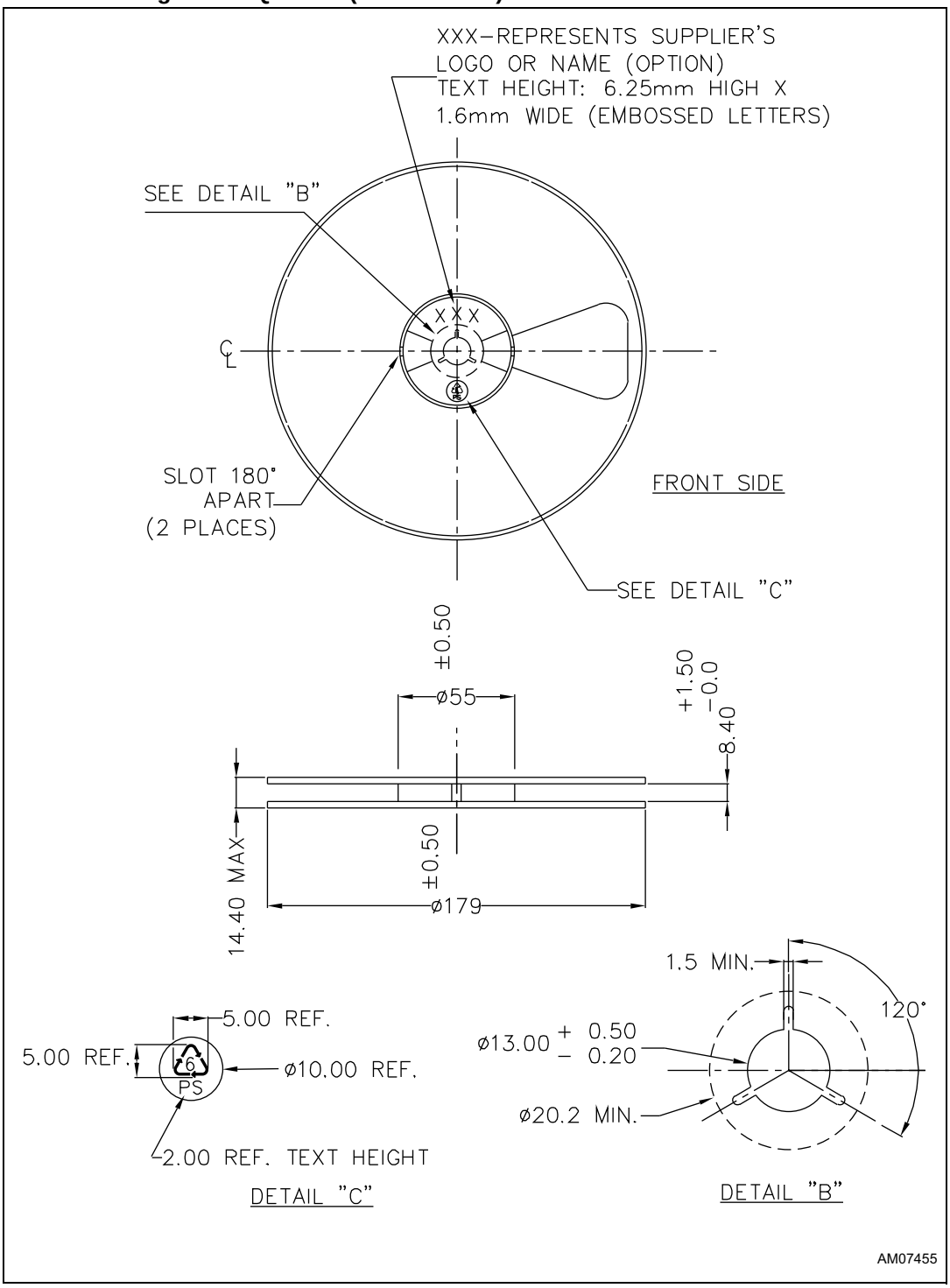
1. Drawing not to scale.

Figure 15. QFN10L (1.8 x 1.4 mm) reel information - back view



1. Drawing not to scale.

Figure 16. QFN10L (1.8 x 1.4 mm) reel information - front side



1. Drawing not to scale.

7 Revision history

Table 10. Document revision history

Date	Revision	Changes
07-Mar-2014	1	Initial release.

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