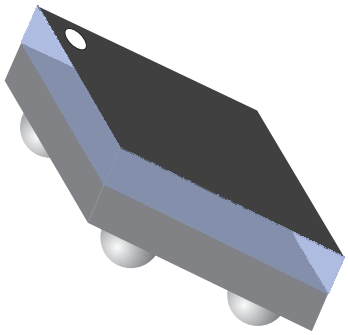
BAL-CC1101-01D3

50 ohm nominal input / conjugate match balun to CC1101 / CC1150 (868-928 MHz), with integrated harmonic filter

Datasheet – production data



Flip-Chip package
4 bumps

Features

- 50 Ω nominal input / conjugate match to CC1101 / CC1150
- Low insertion loss
- Low amplitude imbalance
- Low phase imbalance
- Coated Flip-Chip on glass
- Small footprint: < 2.1 mm²

Benefits

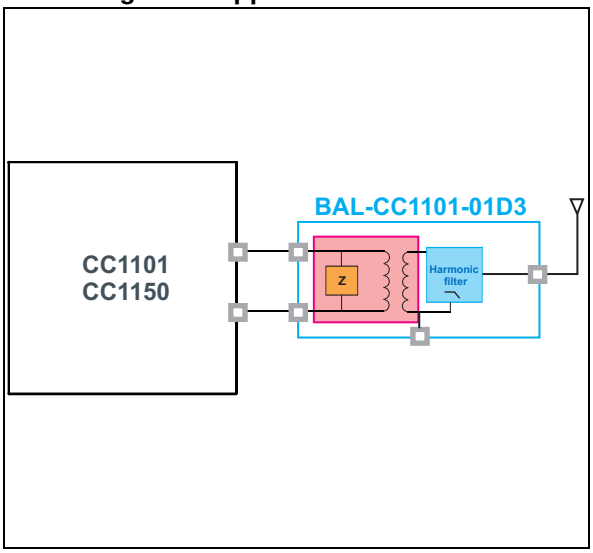
- Extremely low profile (< 550 µm after reflow)
- High RF performance
- RF BOM and area reduction

Description

STMicroelectronics BAL-CC1101-01D3 is an ultra miniature balun which integrates a matching network in a monolithic glass substrate. This has been customized for the CC1101 / CC1150 TI transceiver.

It's a design using STMicroelectronics IPD (integrated passive device) technology on non-conductive glass substrate to optimize RF performance.

Figure 1. Application schematic



1 Characteristics

Table 1. Absolute maximum rating (limiting values)

Symbol	Parameter	Value	Unit
P_{IN}	Input power RF_{IN}	20	dBm
V_{ESD}	ESD ratings human body model (JESD22-A114C), all I/O one at a time while others connected to GND	2000	V
	ESD ratings machine model, all I/O	500	
	ESD ratings charged device model (JESD22-C101D)	500	
T_{OP}	Operating temperature	-40 to +125	ºC

Table 2. Electrical characteristics - RF performance (T_{amb} = 25 °C)

Symbol	Parameter	Value			Unit
		Min.	Typ.	Max.	
Z_{OUT}	Nominal differential output impedance		Conjugate match to CC1101 / CC1150		Ω
Z_{IN}	Nominal input impedance		50		
F	Frequency range (bandwidth)	779		928	MHz
I_L	Insertion loss in bandwidth		1.7	1.9	dB
R_{L_SE}	Single ended return loss in bandwidth		15		dB
R_{L_DIFF}	Differential ended return loss in bandwidth		15		dB
Φ_{imb}	Phase imbalance	-10		10	°
A_{imb}	Amplitude imbalance	-1		1	dB
Att	Harmonic levels (TX filter) Attenuation at 2fo Attenuation at 3fo		 -25 -50		dB

1.1 Measurements

Figure 2. Transmission (S21)

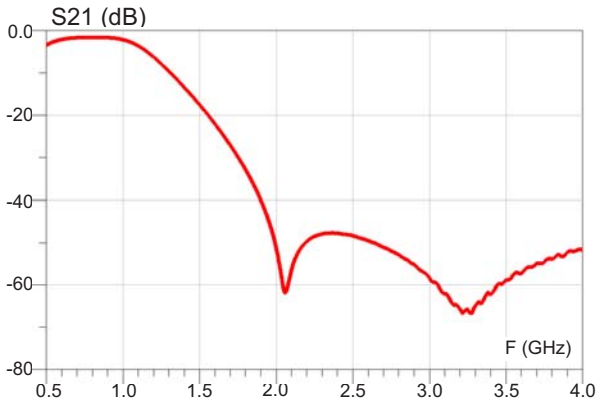


Figure 3. Insertion loss in band

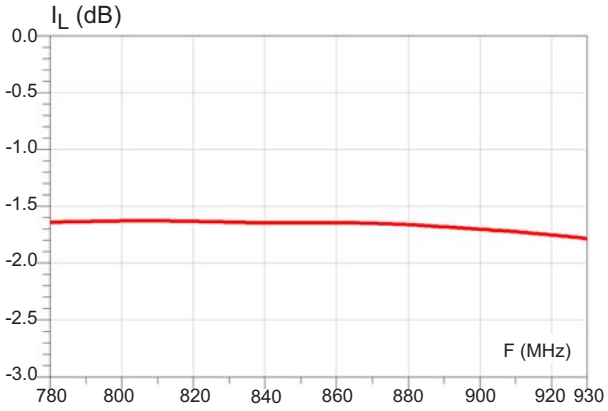


Figure 4. Return loss single-ended

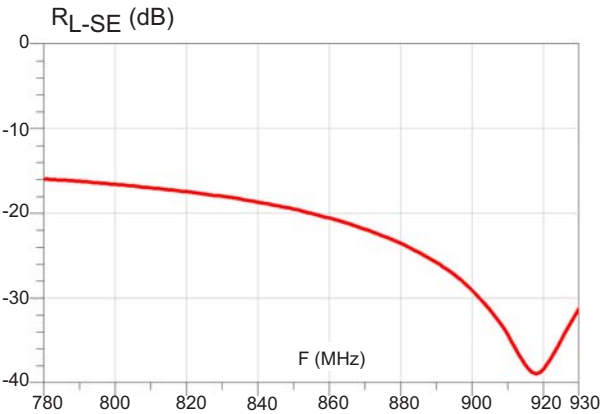


Figure 5. Return loss differential

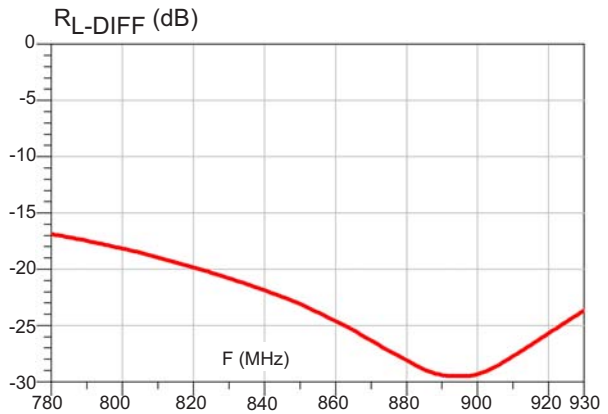


Figure 6. Phase imbalance

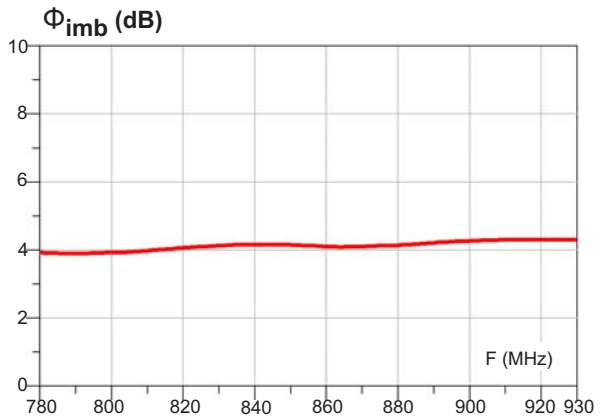


Figure 7. Amplitude imbalance

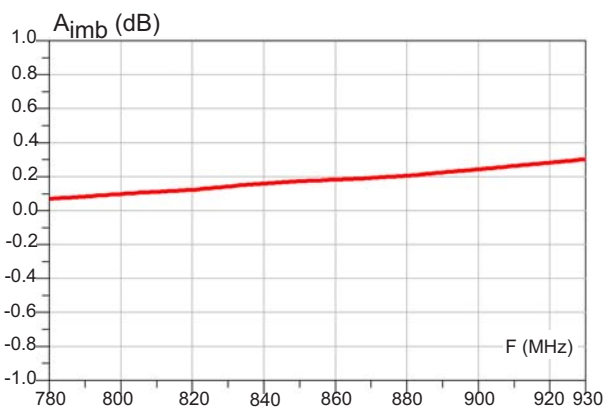


Figure 8. H2 attenuation

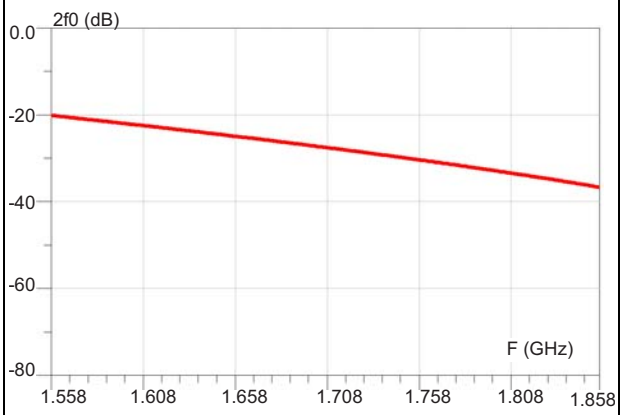
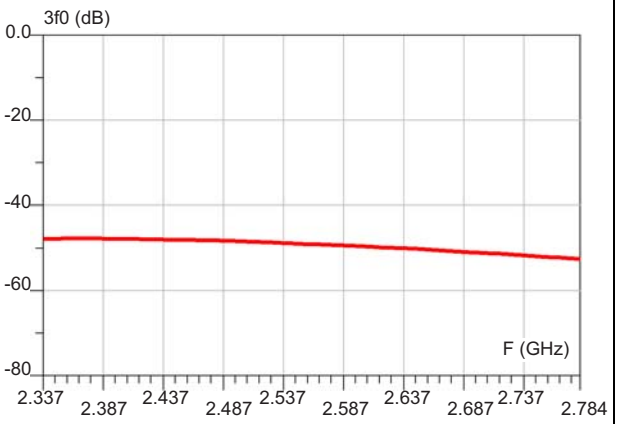


Figure 9. H3 attenuation



2 Package information

- Epoxy meets UL94, V0
- Lead-free package

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

2.1 Flip-Chip package information

Figure 10. Flip-Chip package outline

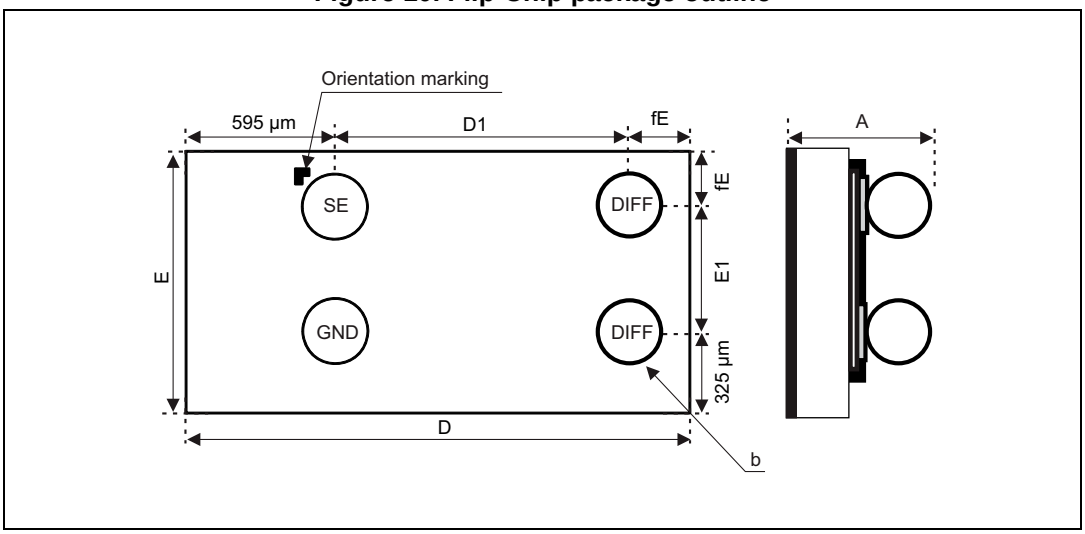


Table 3. Flip-Chip package mechanical data

Parameter	Description	Min.	Typ.	Max.	Unit
A	Bump height + substrate thickness	0.570	0.630	0.690	mm
b	Bump diameter	0.215	0.255	0.295	mm
D	Y dimension of the die	1.970	2.020	2.070	mm
D1	Y pitch		1.200		mm
E	X dimension of the die	1.000	1.050	1.100	mm
E1	X pitch		0.500		mm
fE	Distance from bump to edge of die on X axis			0.225	mm

Figure 11. Footprint - 3 mils stencil -non solder mask defined

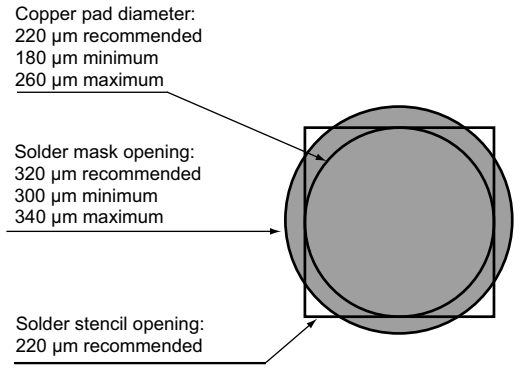


Figure 12. Footprint - 3 mils stencil - solder mask defined

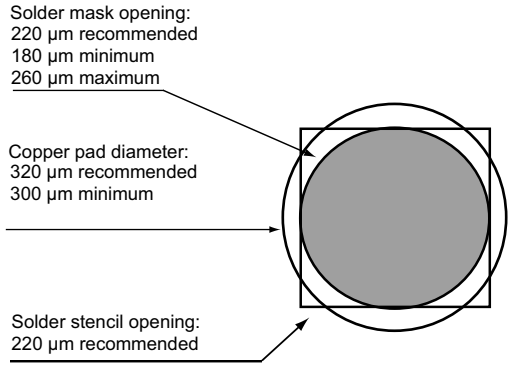


Figure 13. Footprint - 5 mils stencil -non solder mask defined

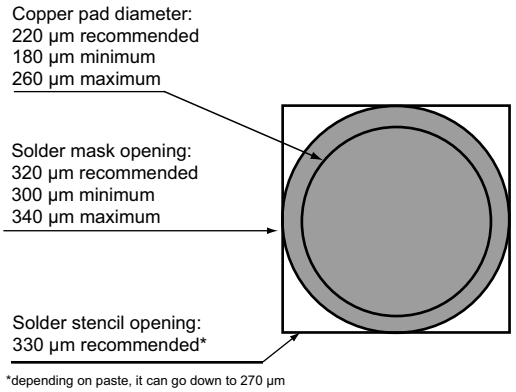


Figure 14. Footprint - 5 mils stencil - solder mask defined

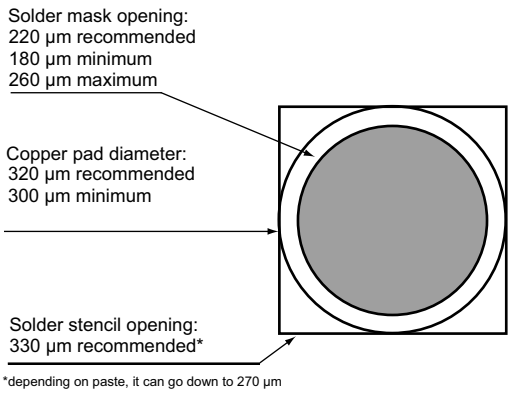


Figure 15. PCB view CC1101 with BAL-CC1101-01D3

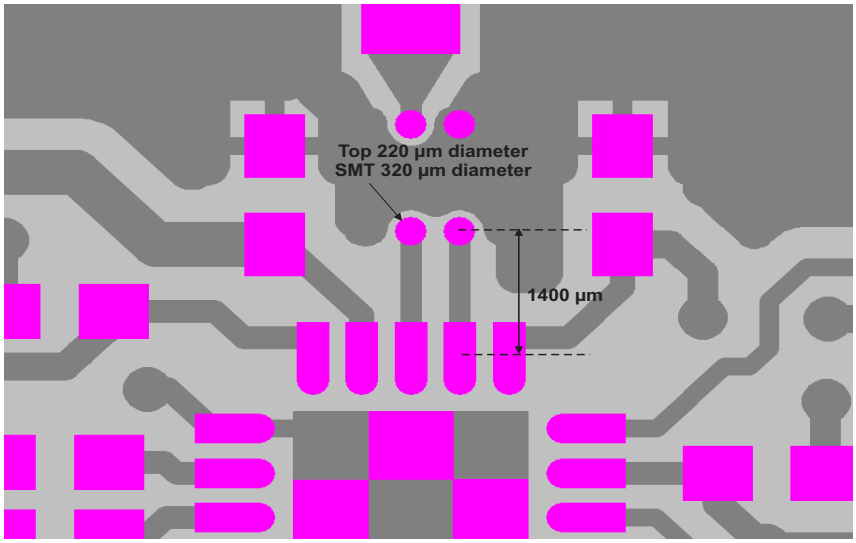


Figure 16. Marking

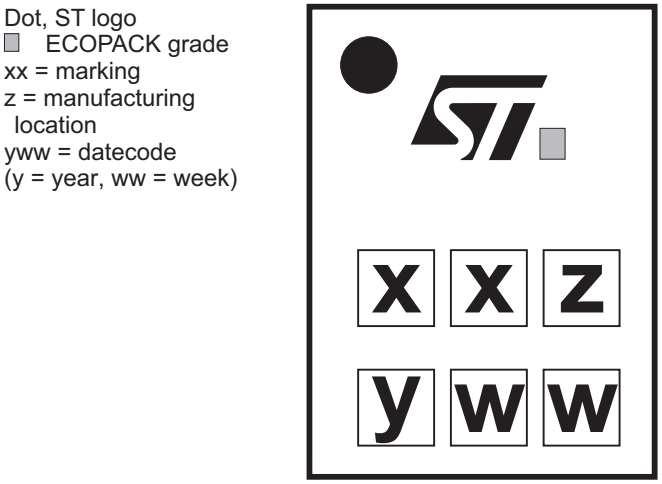
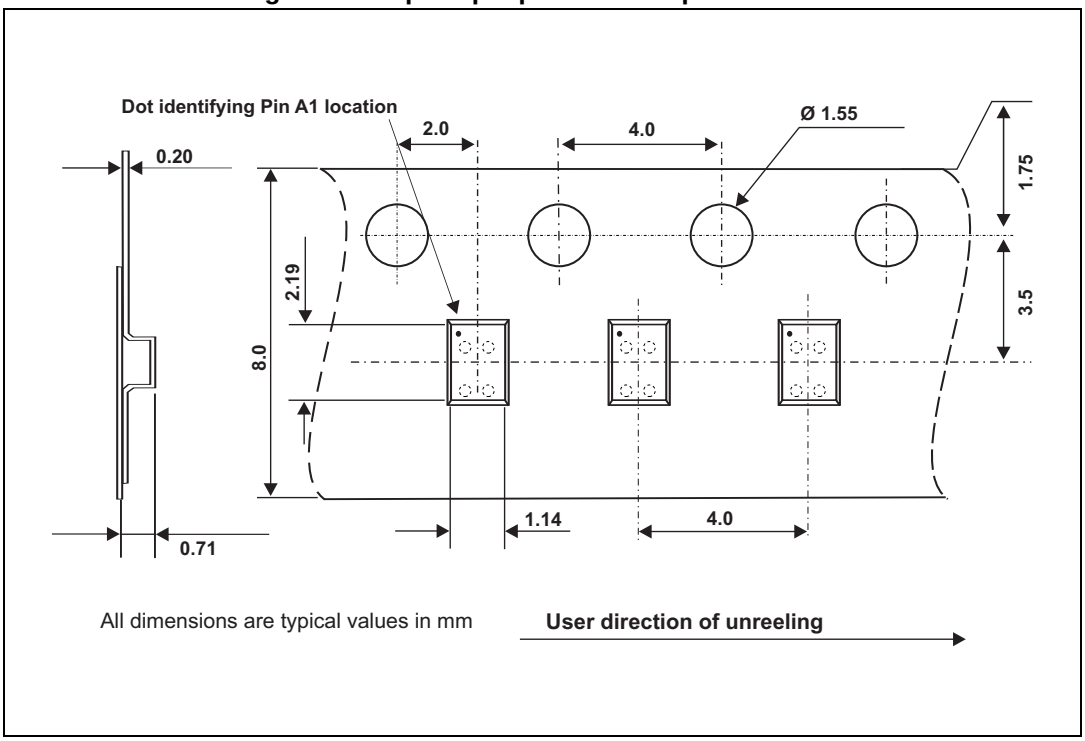


Figure 17. Flip Chip tape and reel specifications



Note: More information is available in the STMicroelectronics Application note: AN2348 Flip-Chip: "Package description and recommendations for use"

3 Ordering information

Table 4. Ordering information

Order code	Marking	Package	Weight	Base qty	Delivery mode
BAL-CC1101-01D3	SS	Flip-Chip	2.21 mg	5000	Tape and reel (7”)

4 Revision history

Table 5. Document revision history

Date	Revision	Changes
23-Jan-2014	1	Initial release
18-Sep-2015	2	Updated Figure 10. Added Figure 11, Figure 12, Figure 13, Figure 14 and Table 3.
02-May-2016	3	Updated *Figure 10* and *Table 3*.

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