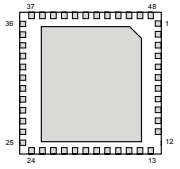
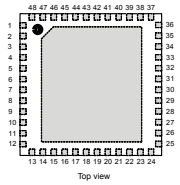
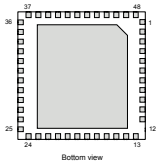
CLT01-38SQ7

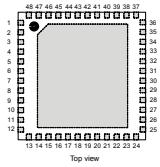
Datasheet

High speed digital input current limiter









Product status link
CLT01-38SQ7

Features

- 8 inputs - 8-bit SPI output
- High side input with common ground
- 5 V voltage regulator
- Package: QFN 7x7 - 48L
- 35 V reverse polarity capable
- Adjustable current limiters
- LED output for visual status
- Optional: 16-bit mode with parity check, temperature and voltage alarms
- Daisy chain capable
- Input digital filter with adjustable delay: 20 µs to 3 ms
- Power dissipation: 78 mW per channel
- **Complies with the following standards**:
  - IEC 61000-4-2: ±8 kV (contact discharge), ±15 kV (air discharge)
  - IEC 61000-4-4: ±4 kV
  - IEC 61000-4-5: Input: ±1 kV, power supply: ±2.5 kV

Applications

- Programmable logic controller and remote input modules
- High speed protected termination for digital input with serialized SPI output
- IEC61131-2 type 1, 2 and 3
- Compliant with EN60947-5-2
- Benefits
  - Simplified design due to
    - Built-in over voltage robustness and immune data transfer
    - Compliance with sensors and PLC's standards
  - Space saving in cost effective solution with
    - Integrated QFN 7x7 package
    - SPI output reducing opto-couplers quantity
  - Energy efficient solution
    - Energy-less input LED visual status powered by inputs current
    - Low overall dissipation versus discrete

Description

The CLT01-38SQ7 provides an 8-line protected digital input termination with serialized state transfer.

This device enhances the I/O module density by cutting the dissipation (78 mW per input) and reducing the count of opto-transistors.

Its 6.25 MHz SPI peripheral output serializes the input state transfer to the I/O module controller.

1 Circuit block diagrams

Figure 1. **Circuit block diagram**

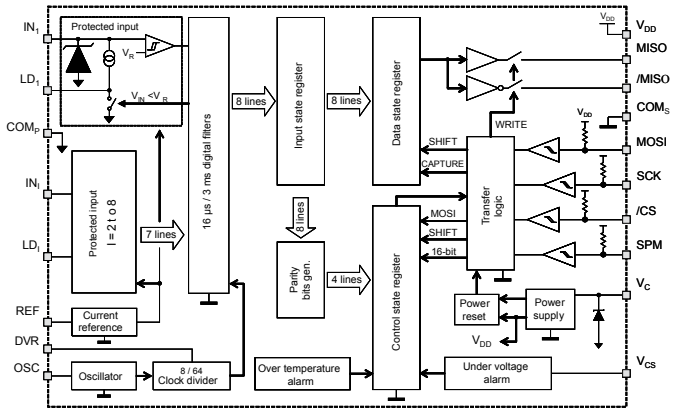
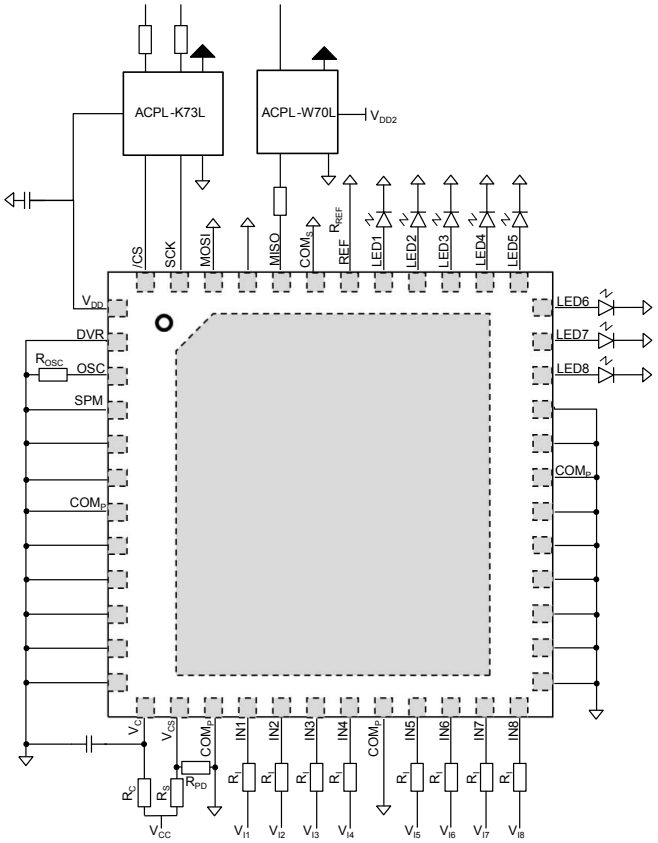


Figure 2. **Basic application schematic**



1.1 I/O pin description

Table 1. **I/O pin description**

Symbol	Parameter		Pin #
IN_I	Power input	Logic input with current limitation, I = 1 to 8	16, 17, 18, 19, 21, 22, 23, 24
LD_I	Power output	LED output driver with current regulation, I = 1 to 8	34, 35, 36, 37, 38, 39, 40, 41
V_C	Power input	24 Vsensorpowersupply	13
V_{CS}	Signal input	24 V sensor power supply sensing input	14
COM_P	Ground	Power ground of power sensor supply	7, 15, 20, 31
V_{DD}	Power output	5 V logic power supply	1
COM_S	Ground	Signal ground of logic / output section	43
REF	Signal input	Input current limiter reference setting	42
SPM	Signal input	SPI shift register length selector: • SPM to GND = 16 bits • SPM to V_{DD} = 8 bits	4
/CS	Logic input	SPI chip Select signal	48
SCK	Logic input	SPI serial clock signal	47
MOSI	Logic input	SPI serial data input signal	46
DVR	Logic input	SPI data selector: • DVR to GND: pin 31 = MISO • DVR to VDD: pin 31 = /MISO	2
MISO or / MISO	Logic output	SPI serial data output signal or inverting SPI serial data output signal	44
TAB	Subtrate	Exposed pad: connected to die substrate, to be connected to COM_P	TAB
NC		Not connected (or to be connected to COM_P)	3, 5, 6, 8, 9, 10, 11, 12, 25, 26, 27, 28, 29, 30, 32, 33, 45

Figure 3. **Pinout description of the QFN7x7-48L version (top view)**

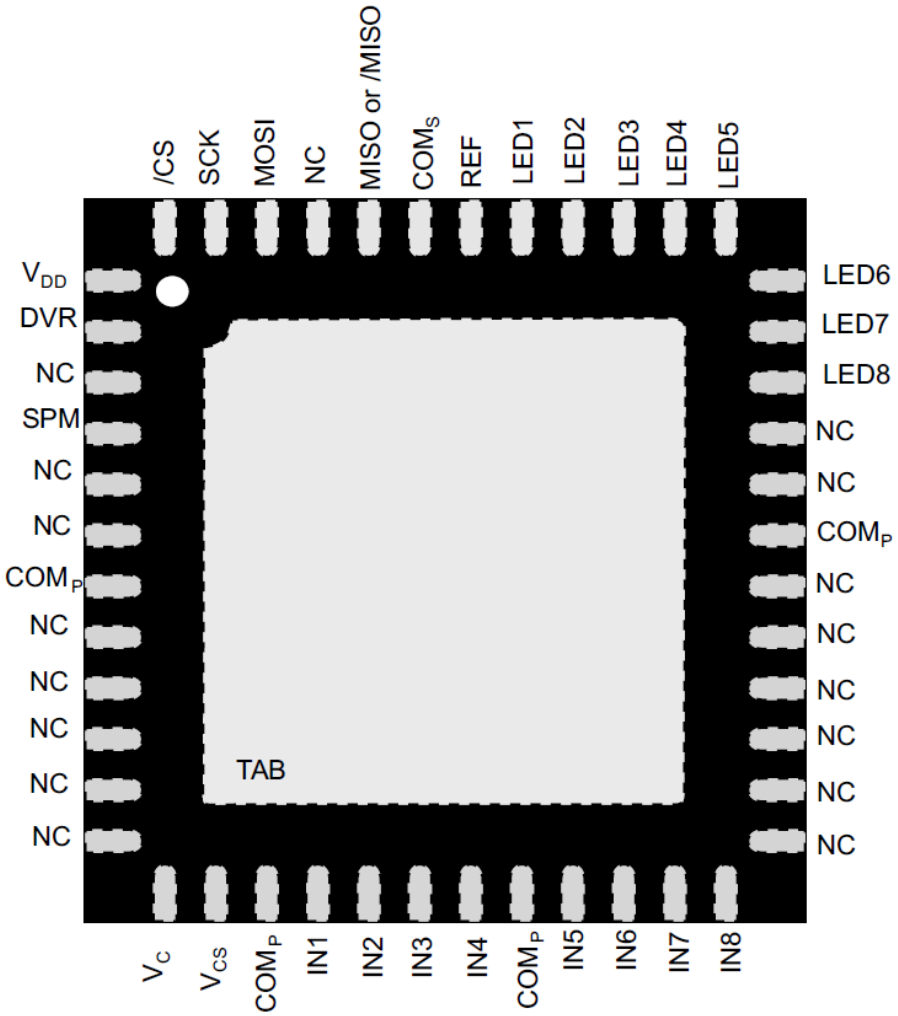
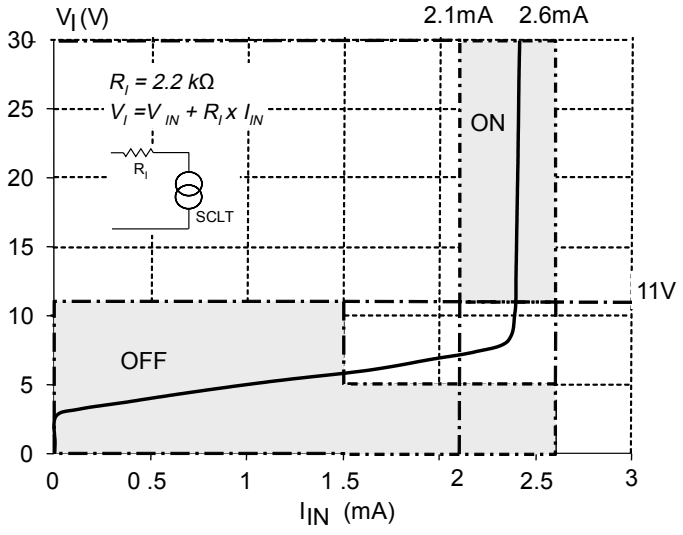


Figure 4. **Basic module input characteristics in type 3**



2 Characteristics

Table 2. Absolute maximum ratings

Symbol	Pin	Parameter name	Conditions	Value	Unit
V_{CC}	V_C	Bus power supply DC voltage	500 Ω < R_C < 2.2 kΩ	-0.3 to 35	V
V_C	V_C	CLT01-38SQ7 power supply voltage	R_C = 0 kΩ	-0.3 to 30	V
I_{CC}	V_C	Maximum bus power supply current		15	mA
V_{CS}	V_{CS}	Sensing bus power supply voltage		-0.3 to 6	V
I_{DD}	V_{DD}	Maximum output power supply current	R_C = 500 Ω	12	mA
V_I	IN_I	Input steady state voltage, I = 1 to 8	R_I = 2.2 kΩ	-35 to 35	V
I_{IN}	IN_I	Input forward current range		-20 to 10	mA
LV_I	SCK, /CS, MOSI	Logic input voltage		-0.3 to 6	V
T_{stg}		Storage temperature range		-40 to 150	°C
T_{amb}		Ambient temperature range		-40 to 105	°C

Table 3. Operating conditions

Symbol	Pin	Parameter name	Conditions	Value	Unit
V_{CC}	V_C	Bus power supply DC voltage	R_C > 500 Ω	15 to 35(1)	V
V_{DD}	V_{DD}	Internal logic power supply voltage		5	V
I_{DD}	V_{DD}	Internal logic power supply voltage	R_C > 500 Ω	10	mA
V_I	IN	Input repetitive steady state voltage	R_I = 2.2 kΩ(2)	-30 to 35	V
V_{LD}	LD_I	Maximum LED output voltage, I = 1 to 8		2.7	V
F_{IN}max	IN	Maximum single input frequency, 8-bit mode		200	kHz
F_{SCK}max		Maximum SPI clock frequency		6.25	MHz
LV	SCK, / CS, MOSI, MISO, /MISO	Logic input / output voltage		0 to 5.5	V
T_{amb}	All	Operating ambient temperature range	V_{CC} ≤ 30 V	-40 to 85	°C
			V_{CC} ≤ 24 V, $R_{th(j-a)}$ = 70 °C/W	-40 to 105	
T_j		Operating junction temperature range		-40 to 150	°C

1. *32 V in DC; 35 V during 0.5 s max*
2. *$V_I = V_{IN} + R_I \times I_{IN}$*

Table 4. DC electrical characteristics based on figure 2 application environment

Symbol	Pin	Name	Conditions	Min.	Typ.	Max.	Unit
Input current limitation							
I_{LIM}	IN	Input limiting current	V_{IN} = 5.5 to 26 V, R_I = 2.2 kΩ	2.1	2.35	2.6	mA
I_{ON}	LD_I	On state LED current	V_I = 11 V	2			mA

Table 5. SPI electrical characteristics (T_j = 25 °C, V_{CC} = 24 V, V_{DD} = 5 V respect to COM ground pin; unless otherwise specified)

Symbol	Pin	Name	Conditions	Min.	Typ.	Max.	Unit
F_{CK}	SCK	Clock frequency				6.25	MHz
$T_{CAPTURE}$		Minimum data capture time	F_{CK} = 6.25 MHz	2.5			µs
T_{PROPA}		Data transfer / Propagation time		4			ns
T_S	MOSI	Data setup time	MOSI toggling to SCK rising	25			ns
T_D	MISO	Write out propagation time	SCK falling to MISO toggling, C_{OUT} = 10 pF			50	ns
T_{LD}	SCK	Enable lead time	/CK falling to SCK rising	80			ns
T_{HC}	SCK	Clock hold time	SCK falling to /CS rising	160			ns
T_{DT}	/CS	Transfer delay time	/CS rising to /CS falling			150	ns
T_H	MOSI	Data hold time	SCK rising to MOSI toggling	25			ns
T_{DIS}	MISO	Data output disable time	/CS rising to MISO disabled			200	ns
LV_{IH}	MOSI, SCK, /CS	Logic input high voltage	Share of V_{DD}			70	%
LV_{IL}		Logic input low voltage	Share of V_{DD}	30			%
LV_{OH}	MISO, /MISO	Logic output high voltage	I_{OH} = 3 mA	4	4.75		V
LV_{OL}		Logic output low voltage	I_{OL} = 3 mA		0.25	1	V
T_{RO}, T_{FO}	MISO, /MISO	MISO signal fall/rise time	I_{MISO} = 3 mA		20		ns
T_A	MISO	Output access time	/CS falling to MISO toggling		40	80	ns
D_UC_Y	SCK	Clock duty cycle		25		75	%

Figure 5. Time diagram

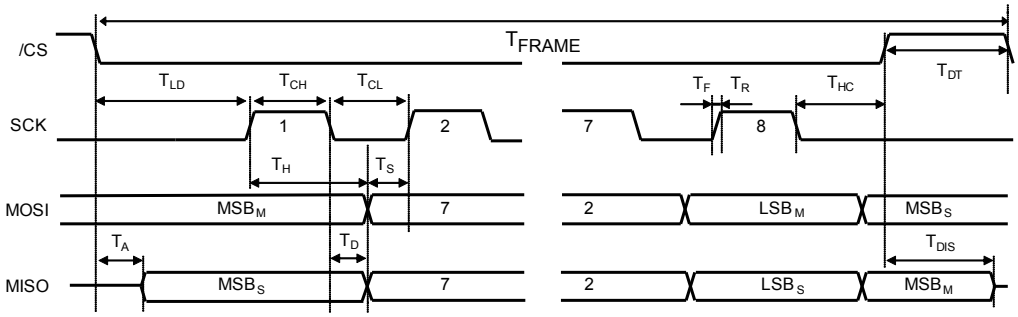


Table 6. Electromagnetic compatibility ratings

Symbol	Pin	Parameter name (1)	Value	Unit
V_{PPB}	V_I	Peak pulse voltage burst, IEC61000-4-4 (2)	4	kV
V_{PP}	V_I	Peak pulse voltage surge, IEC61000-4-5	1	kV
V_{PP}	V_{CC}	Peak pulse voltage surge, IEC61000-4-5	2.5	kV
V_{ESD}	V_{IN}	ESD protection, IEC 61000-4-2, per input: Air Contact	 15 8	kV

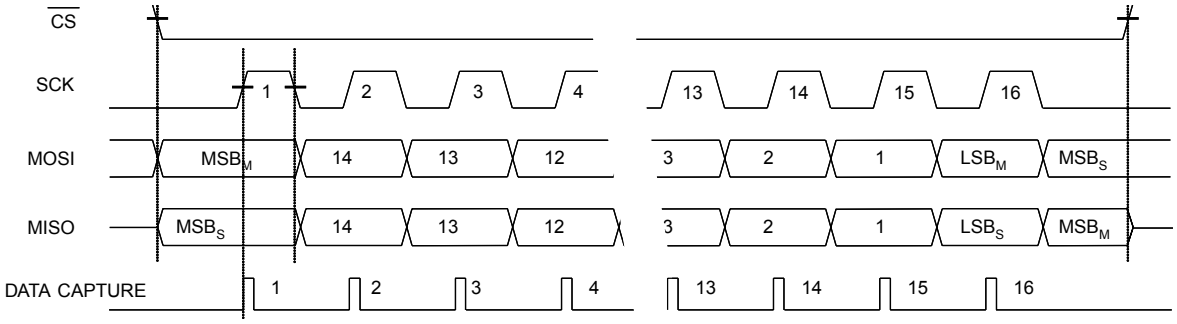
1. *Test set-up, see application Figure 2*
2. *See AN3031.*

3 Functional description

3.1 Operation of the CLT01-38SQ7 with SPI bus (C_{POL} = 0, C_{PHA} = 0)

The SPI bus master controller manages the data transfer with the chip select signal /CS and controls the data shift in the register with the clock SCK signal.

Figure 6. Serial data format frame



The transfer of the CLT01-38SQ7 input states in the SPI registers starts when the Chip Select /CS signal falls and ends when this /CS is rising back.

The transfer of data out of the CLT01-38SQ7 slave MISO output starts immediately when the chip select /CS goes low.

Then, the input MOSI is captured and presented to the shift register on each rising edge of the clock SCK. And the data are shifted in this register on each falling edge of the serial clock SCK, the data bits being written on the output MISO with the most significant bit first.

3.1.1 The serial data Input MOSI

This input signal MOSI is used to shift external data bits into the CLT01-38SQ7 register from the most significant MSB bit to the lower significant one LSB. The data bits are captured by the CLT01-38SQ7 on the rising edge of the serial clock signal SCK.

3.2 The SPI data transfer operation

3.2.1 The SPI data frame

Depending on the biasing of the SPM pin, the data frame is 8-bits or 16-bits. The selected structure of the SPI is a 16-bit word in order to be able to implement the input state data and some control bits such as the UVA alarm, the 4 checksum bits and the two low and high state stop bits.

3.2.2 The SPI data transfer

The CLT01-38SQ7 transfers its 16 data bits through the SPI within one chip select Hi-Lo-Hi sequence. So, this length defines the minimum length that the shift register of the SPI master controller is able to capture: 16 bits.

The Table 7 shows the 16-bit mode way the data are transferred starting from the data bits, the control bits and ending by a stop bit.

Table 7. SPI data transfer organization versus CLT input states with SPM = 0

Bit #	LSB	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
Control	High(1)	Low	PC4	PC3	PC2	PC1	/OTA	/UVA
Bit #	Bit 8	Bit 9	Bit 10	**Bit 11**	Bit 12	Bit 13	Bit 14	MSB
Data	IN 1	IN 2	IN 3	IN 4	IN 5	IN 6	IN 7	IN 8(2)

1. *Last OUT*
2. *First OUT*

3.3 Control bit signals of the SPI transferred data frame

3.3.1 The power bus voltage monitoring

The UVA circuit generates the alarm /UVA that is active low when the power bus voltage is lower than the activation threshold V_{CON}, 17 V typical, and it is disabled high when the power bus voltage rises above the threshold V_{COFF}, 18 V typical.

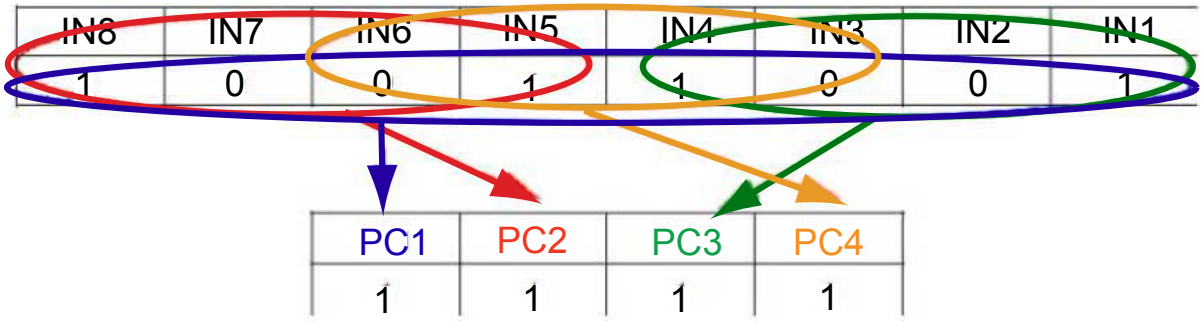
3.3.2 The over temperature alarm

The alarm signal /OTA is enabled, low state active, when the junction temperature is higher than the activation threshold T_{ON}, 150 °C typical, and it is disabled when the junction temperature falls below the threshold T_{OFF}, 140 °C typical.

3.3.3 The parity checksum bits calculation and transfer

The aim of the parity checksum bit is to detect one error in the transferred SPI word. Several parity checksum bits are generated and transmitted through the SPI on the control bit #2 to #5. In order to calculate parity bit, “exclusive NOR” operations are performed as follow:

Figure 7. CLT01-38SQ7 parity bit calculation example



3.4 Loss of VCC power supply

The operation of the CLT01-38SQ7 is extended below the levels required in the IEC 61131-2 standard to allow the implementation of the under voltage alarm UVA as described the SPI control bit section.

If there is no more power feeding on the V_{CC} input, the CLT01-38SQ7 chip goes to sleep mode, and the MISO output is forced in low state during SPI transfer attempt. The last SPI control data bit is a stop bit placed normally in high state all time: the loss of power supply is detected by checking its state: if low, the output is disabled by the internal power reset POR.

This POR signal is active in low state when VC is less than 9 V or the internal power supply V_{DD} is less than 3.25 V.

Table 8. Logic state of the SPI output versus the power loss signal POR and the SPI chip select /CS

POR	/CS	MISO	/MISO	SPI status
1	1	Z	Z	Normal with no communication
1	0	1	0	Normal with communication
1	0	0	1	Normal with communication
0	1	Z	Z	Power loss with no communication
0	0	0	1	Power loss with communication attempt

Figure 8. Logic status of the CLT01-38SQ7 power supply

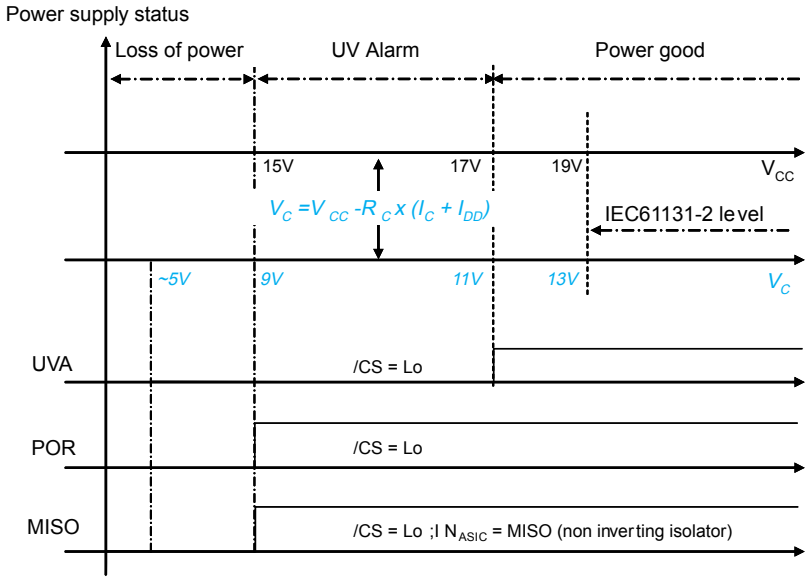


Figure 9. Typical limiting current I_{LIM} versus reference resistance R_{REF}

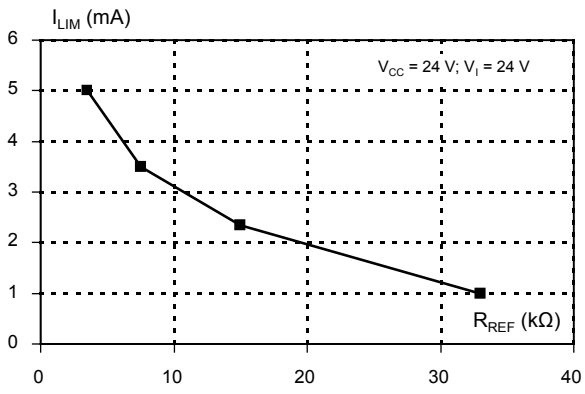


Figure 10. Typical limiting current I_{LIM} versus junction temperature T_j

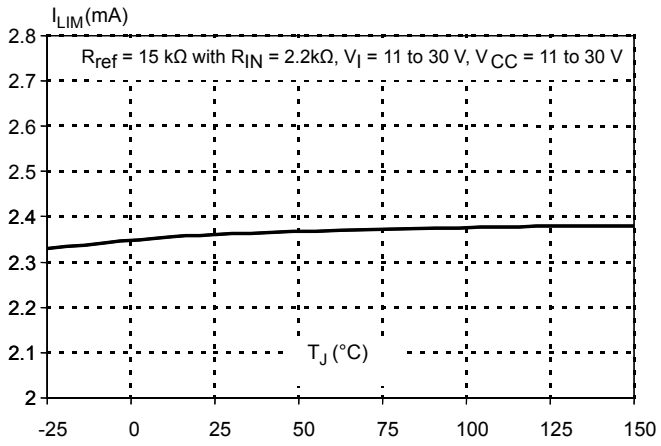


Figure 11. Relative variation of minimum filter time t_{FT} versus junction temperature T_J

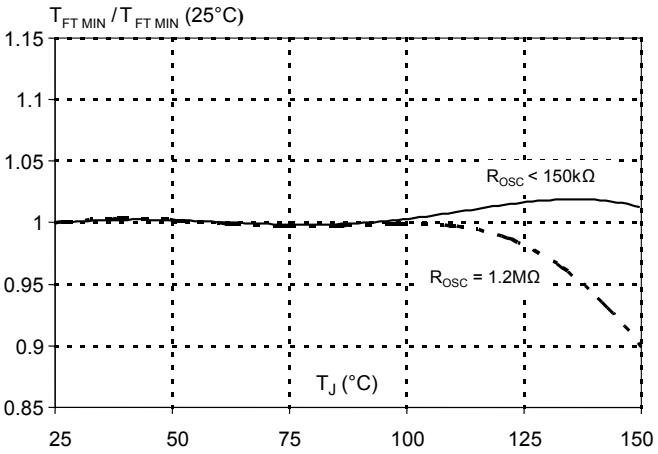
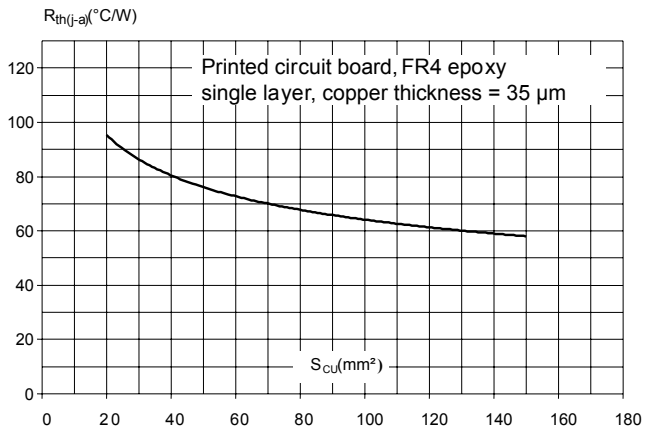


Figure 12. Variation of junction to ambient thermal resistance $R_{th(j-a)}$ versus printed circuit board copper surface S_{CU}



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 QFN 7X7-48 L package information

Figure 13. QFN 7X7-48 L package outline

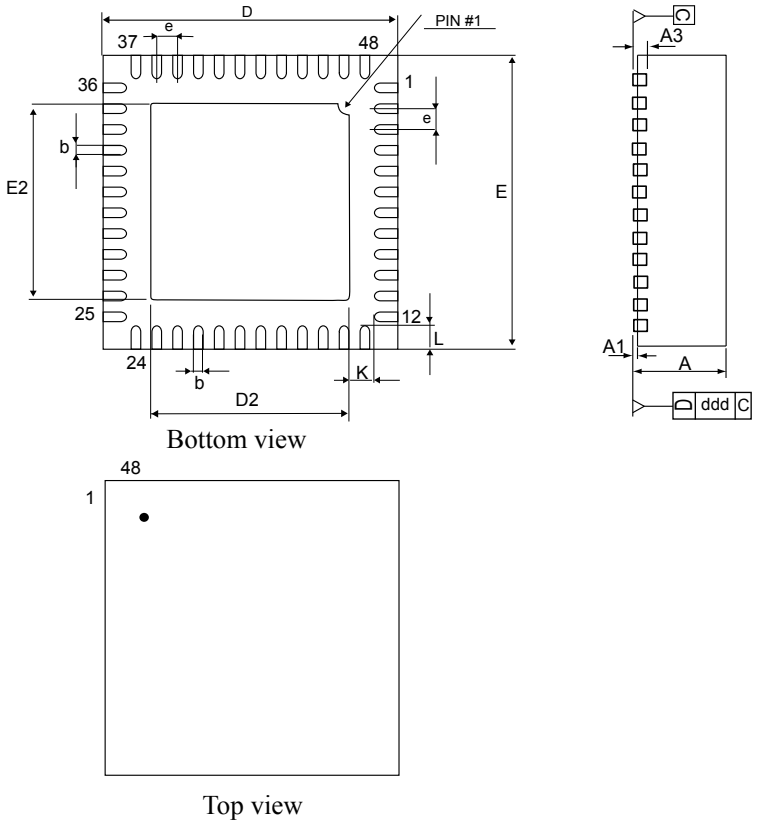


Table 9. QFN 7X7-48 L package mechanical data

Ref.	Dimensions					
	Millimeters			Inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.80	0.90	1.00	0.0315	0.0354	0.0394
A1		0.02	0.05		0.0008	0.0020
A3		0.203			0.008	
b	0.18	0.25	0.30	0.0071	0.0100	0.0118
D		7.00			0.275	
E		7.00			0.275	
e		0.50			0.019	
D2	5.00	5.15	5.25	0.197	0.203	0.206
E2	5.00	5.15	5.25	0.197	0.203	0.206
K	0.20			0.008		
L	0.30	0.40	0.50	0.011	0.015	0.019

1. *Values in inches are converted from mm and rounded to 4 decimal digits.*

5 Ordering information

Figure 14. **Ordering information scheme**

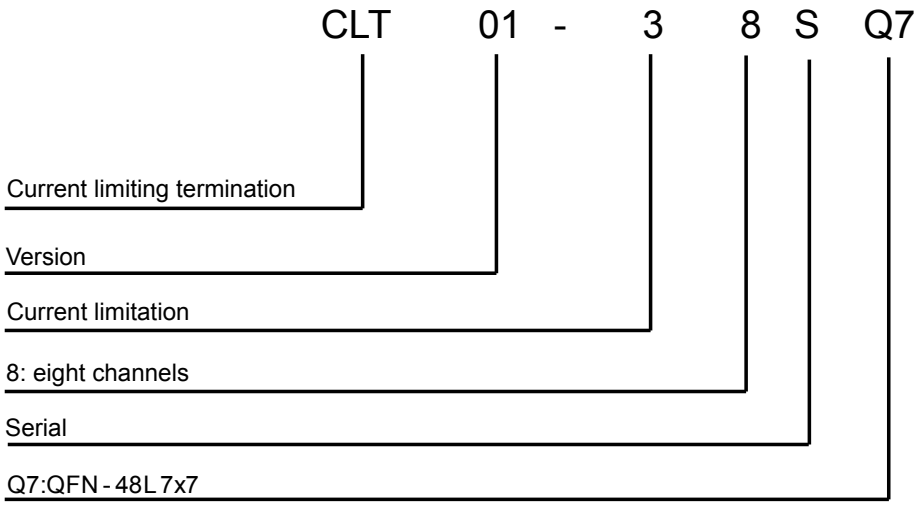


Table 10. **Ordering information**

Order code	Marking	Package	Weight	Base qty.	Delivery mode
CLT01-38SQ7	CLT01-38SQ7	QFN7x7-48L	114 mg	2500	Tape and reel

Revision history

Table 11. **Document revision history**

Date	Revision	Changes
31-July-2015	1	Initial release.
04-Nov-2021	2	Updated Figure 2.

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