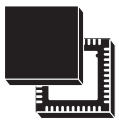
LIS3L02DQ

MEMS INERTIAL SENSOR: 3-Axis - ±2g DIGITAL OUTPUT LINEAR ACCELEROMETER

1 Features

- 2.7V TO 3.6V SINGLE SUPPLY OPERATION
- 1.8V COMPATIBLE IOs
- 12 BIT RESOLUTION
- I^2C/SPI DIGITAL OUTPUT INTERFACES
- INTERRUPT ACTIVATED BY MOTION
- PROGRAMMABLE INTERRUPT THRESHOLD
- EMBEDDED SELF TEST
- HIGH SHOCK SURVIVABILITY
- ECO-PACK COMPLIANT

Figure 1. Package



QFN-44

Table 1. Order Codes

Part Number	Package	Finishing
LIS3L02DQ	QFN44	Tray
LIS3L02DQ-TR	QFN44	Tape & Reel

2 Description

The LIS3L02DQ is a three axes digital output linear accelerometer that includes a sensing element and an IC interface able to take the information from the sensing element and to provide the measured acceleration signals to the external world through an I^2C/SPI serial interface.

The sensing element, capable of detecting the acceleration, is manufactured using a dedicated process developed by ST to produce inertial sensors and actuators in silicon.

The IC interface instead is manufactured using a CMOS process that allows high level of integration to design a dedicated circuit which is factory trimmed to better match the sensing element characteristics.

A self-test capability allows the user to check the functioning of the system.

The device may be configured to generate an inertial wake-up/interrupt signal when a programmable acceleration threshold is exceeded at least along one of the three axes.

The LIS3L02DQ is available in plastic SMD package and it is specified over a temperature range extending from -20°C to +70°C.

The LIS3L02DQ belongs to a family of products suitable for a variety of applications:

- Motion activated functions in mobile terminals
- Antitheft systems and Inertial navigation
- Gaming and Virtual Reality input devices
- Vibration Monitoring and Compensation

Figure 2. Block Diagram

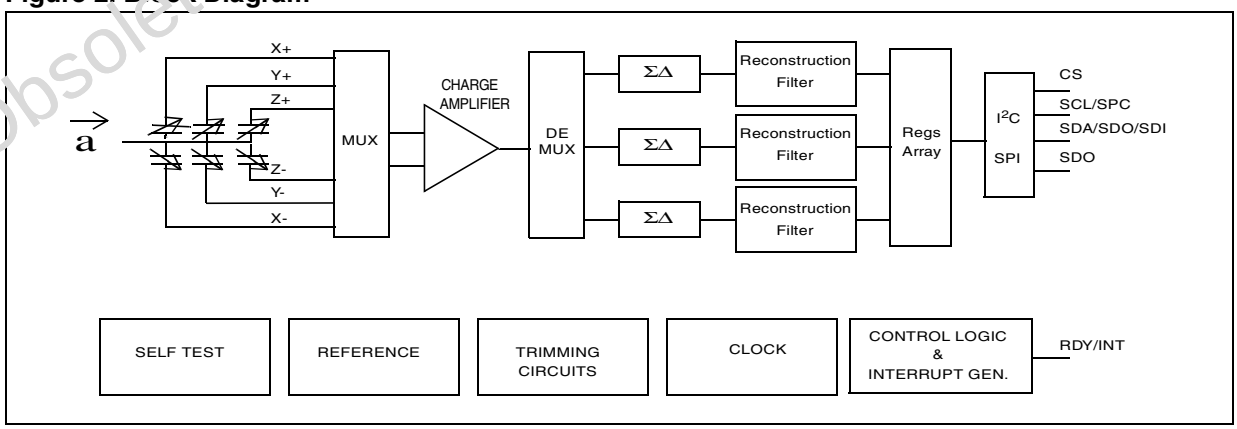


Table 2. Pin Description

N°	Pin	Function
1 to 2	NC	Internally not connected
3	GND	0V supply
4	Vdd	Power supply
5 to 12	NC	Internally not connected
13	Reserved	Leave unconnected or connect to Vdd_IO
14	Reserved	Leave unconnected or connect to GND
15	RDY/INT	Data ready/inertial wake-up interrupt
16	SDO	SPI Serial Data Output
17	SDA/ SDI/ SDO	I^2C Serial Data (SDA) SPI Serial Data Input (SDI) 3-wire Interface Serial Data Output (SDO)
18	SCL/SPC	I^2C Serial Clock (SCL) SPI Serial Port Clock (SPC)
19	CS	SPI enable I^2C/SPI mode selection (1: I^2C mode; 0: SPI enabled)
20	Vdd_IO	Power supply for I/O pads
21	Vdd	Power supply
22	GND	0V supply
23 to 44	NC	Internally not connected

Figure 3. Pin Connection (Top view)

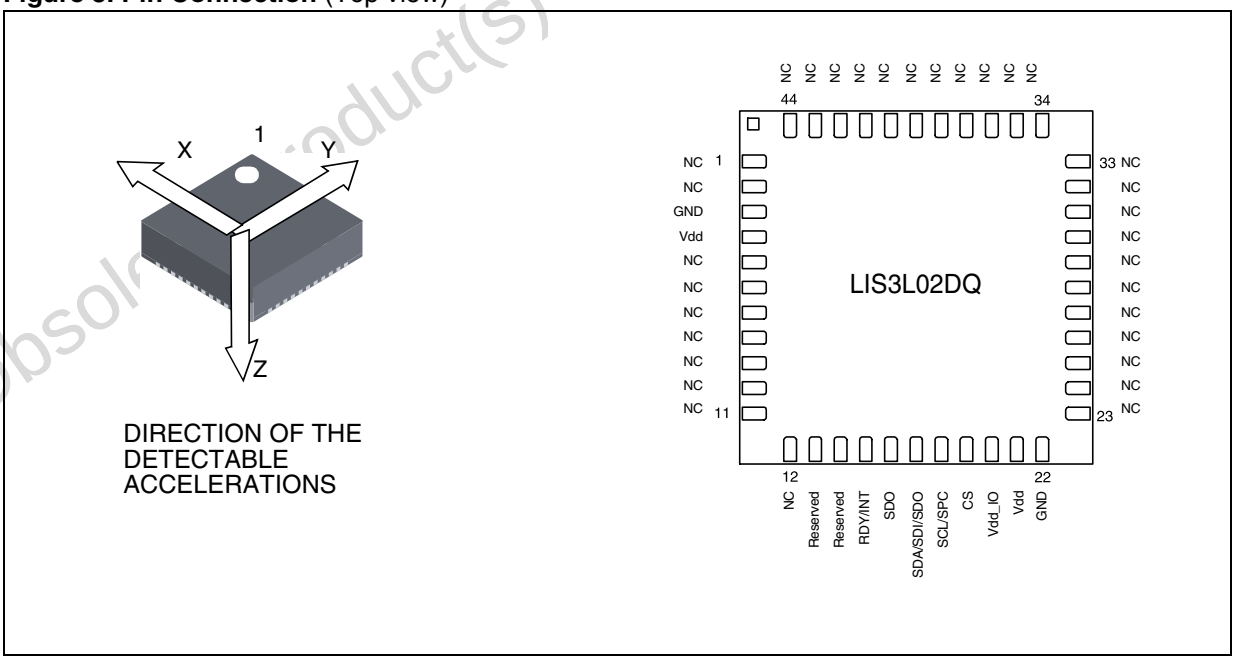


Table 3. Mechanical Characteristics[1]

(Temperature range -20°C to +70°C). All the parameters are specified @ Vdd = 3.3V and T = 25°C unless otherwise noted.

Symbol	Parameter	Test Condition	Min.	Typ.[2]	Max.	Unit
Ar	Acceleration Range[3]			±2.0		g
So	Sensitivity[4]		974	1024	1074	LSB/g
SoDr	Sensitivity Change Vs Temperature	Delta from +25°C		±0.2		LSB/°C
Off_{LSB}	Zero-g Level	T = 25°C	-52	0	+52	LSB
OffDr	Zero-g Level Change Vs Temperature	Delta from +25°C		±0.8		LSB/°C
NL	Non Linearity[5]	Best fit straight line X, Y axis		±0.3	±1.5	% FS
		Best fit straight line; Z axis		±0.6	±2.0	% FS
CrossAx	Cross-Axis[6]			±2	±4	%
V_{st}	Self test Output Change[7]	T = 25°C Vdd=3.3V X axis Ratiometric Vs Vdd	+100	+250	+400	LSB
		T = 25°C Vdd=3.3V Y axis Ratiometric Vs Vdd	-100	-250	-400	LSB
		T = 25°C Vdd=3.3V Z axis Ratiometric Vs Vdd	-100	-250	-400	LSB
Fres	Sensing Element Resonance Frequency[8]	all axes	1.5			kHz
Top	Operating Temperature Range		-20		+70	°C
Wh	Product Weight			0.2		gram

Notes: 1. Product is factory calibrated at 3.3 Volts.The device can be used from 2.7 V to 3.6 V.
2. Typical specifications are not guaranteed
3. Verified by wafer level test and measurement of initial offset and sensitivity.
4. 1 LSB is equal to 0.97mg=(4g / 4096)
5. Zero g level output is in two's complement encode.
6. Contribution to the measuring output of the inclination/acceleration along any perpendicular axis.
7. Contribution of the inclination/acceleration along any perpendicular axis to the measuring output.
8. Self test output changes linearly with the power supply. "Selftest output change" describes the output signal change if the "ST" bit in CRT_REG1 is changed from normal mode to self test enable.
9. Sensor bandwidth is defined by the Decimation Factor (see table 4)

Table 4. Electrical Characteristics[1]

(Temperature range -20°C to +70°C). All the parameters are specified @ Vdd=3.3V and T=25°C unless otherwise noted.

Symbol	Parameter	Test Condition	Min.	Typ.[2]	Max.	Unit
Vdd	Supply Voltage		2.7	3.3	3.6	V
Vdd_IO	I/O pads Supply Voltage		1.8		Vdd+0.1	V
Idd	Supply Current	T = 25°C		1	1.5	mA
IddPdn	Current Consumption in Power-Down Mode	T = 25°C			15	µA
BW	Digital Filter Cut-Off frequency (-3dB)	Dec factor = 128		70		Hz
		Dec factor = 64		140		Hz
		Dec factor = 32		280		Hz
		Dec factor = 8		1120		Hz
DR	Output Data Rate	Dec factor = 128		280		Hz
		Dec factor = 64		560		Hz
		Dec factor = 32		1120		Hz
		Dec factor = 8		4480		Hz
F_{max}	SPI Frequency	Vdd_IO<2.4V			4	MHz
		Vdd_IO>2.4V			8	MHz
Ton	Turn on time at exit from Power Down Mode [3]			6/DR		ms

Notes: 1. Product is factory calibrated at 3.3V.The device can be used from 2.7 V to 3.6 V
2. Typical specifications are not guaranteed.
3. Turn on time is related to output rate and it's defined as: Ton =6/DR.Ton time is the time between leaving Power Down mode and reaching 99% of actual acceleration value.

3 Absolute Maximum Rating

Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 5. Absolute Maximum Rating

Symbol	Ratings	Maximum Value	Unit
Vdd	Supply Voltage	-0.3 to 6	V
Vdd_IO	I/O pads Supply Voltage	-0.3 to Vdd +0.1	V
Vin	Input Voltage on any control pin (CS, SCL/SPC, SDA/SDI/SDO,SDO,RDY/INT)	-0.3 to Vdd +0.3	V
A_{POW}	Acceleration (Any axis, Powered, Vdd=3.3V)	3000g for 0.5 ms	
		10000g for 0.1 ms	
A_{UNP}	Acceleration (Any axis, Not Powered)	3000g for 0.5 ms	
		10000g for 0.1 ms	
T_{STG}	Storage Temperature Range	-40 to +125	°C
ESD	Electrostatic Discharge Protection	1 (HBM)	kV
		200 (MM)	V
		1.5 (CDM)	kV


This is a Mechanical Shock sensitive device, improper handling can cause permanent damages to the part


This is an ESD sensitive device, improper handling can cause permanent damages to the part

3.1 Terminology

3.1.1 Sensitivity

Sensitivity describes the gain of the sensor and can be determined e.g. by applying 1g acceleration to it. As the sensor can measure DC accelerations this can be done easily by pointing the axis of interest towards the center of the earth, note the output value, rotate the sensor by 180 degrees (point to the sky) and note the output value again. By doing so, ±1g acceleration is applied to the sensor. Subtracting the larger output value from the smaller one and divide the result by 2 leads to the actual sensitivity of the sensor. This value changes very little over temperature (see sensitivity temperature change) and also very little over time. The Sensitivity Tolerance describes the range of Sensitivities of a large population of sensors.

3.1.2 Zero g level

Zero-g level (Offset) describes the deviation of an actual output signal from the ideal output signal if there is no acceleration present. A sensor in a steady state on a horizontal surface will measure 0g in X axis and 0g in Y axis whereas the Z axis will measure 1g. The output is ideally in the middle of the dynamic range of the sensor (0000 0000 0000). A deviation from this value is called zero-g offset; the coding is based two's complement. Offset is to some extend a result of stress to a precise MEMS sensor and therefore the offset can slightly change after mounting the sensor onto a printed circuit board or exposing it to extensive mechanical stress. Offset changes little over temperature, see “Zero g level change vs. temperature”. The Zero-g level of an individual sensor is very stable over lifetime. The Zero g level tolerance describes the range of zero g levels of a population of sensors.

3.1.3 Self Test

Self Test allows to test the mechanical and electrical part of the sensor. By applying a digital code via the serial interface to the sensor an internal reference is switched to a certain area of the sensor and creates a defined deflection of the moveable structure. The sensor will generate a defined signal and the interface chip will perform the signal conditioning. If the output signal changes within the specified amplitude than the sensor is working properly and the parameters of the interface chip are within tolerance. Self Test changes linearly with power supply.

4 Functionality

4.1 Sensing element

A proprietary process is utilized to create a surface micro-machined accelerometer. The technology allows to carry out suspended silicon structures which are attached to the substrate in a few points called anchors and are free to move on a plane parallel to the substrate itself. To be compatible with the traditional packaging techniques a cap is placed on top of the sensing element to avoid blocking the moving parts during the moulding phase of the plastic encapsulation.

When an acceleration is applied, the proof mass displaces from its nominal position, causing an imbalance in the capacitive half-bridge. This imbalance is measured using charge integration in response to a voltage pulse applied to the sense capacitors.

The nominal value of the capacitors, at steady state, are a few pF and when an acceleration is applied the maximum variation of the capacitive load is up to 100 fF.

4.2 IC Interface

The complete measurement chain is composed of a low-noise capacitive charge amplifier which converts the capacitive unbalanced signal of the MEMS sensor into an analog voltage. Three ΣΔ analog-to-digital converters, one for each axis, translate the signal into a digital bitstream.

The ΣΔ converters are tightly coupled with dedicated reconstruction filters which remove the high frequency components of the quantization noise and provide high resolution digital words.

The charge amplifier and the ΣΔ converters are operated at 107.5 kHz and 35.8 kHz.

The data rate at the output of the reconstruction filters depends on the user selected Decimation Factors (DF) and are selectable from 280 Hz to 4.48 kHz.

The acceleration data may be accessed through an I^2C/SPI interface thus making the device particularly suitable for direct interfacing with a microcontroller.

The LIS3L02DQ features a Data-Ready signal (RDY) which indicates when a new set of measured acceleration data is available thus simplifying data synchronization in digital systems.

The LIS3L02DQ may also be configured to generate an inertial wake-up/interrupt signal when a programmable acceleration threshold is exceeded along one of the three axes.

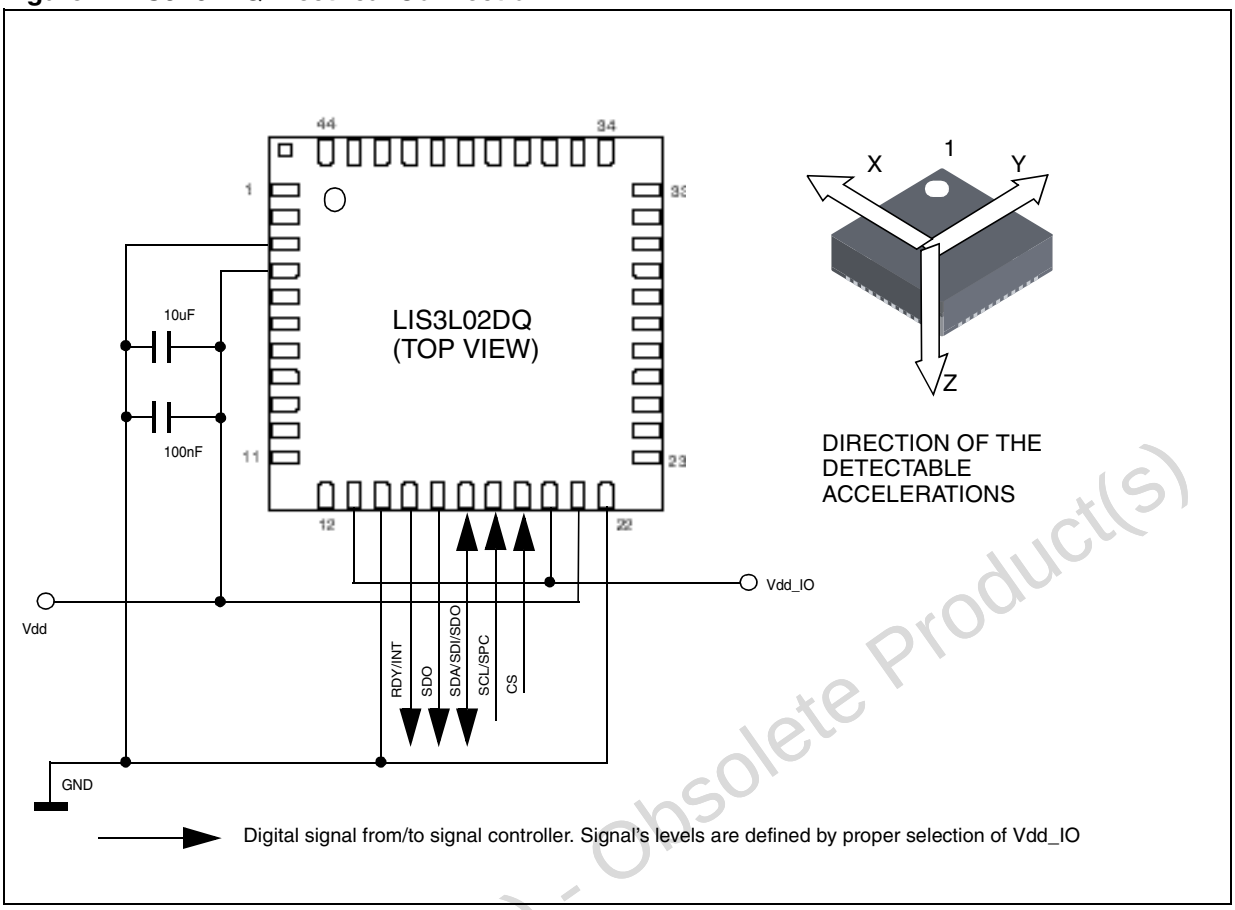
4.3 Factory calibration

The IC interface is factory calibrated to provide a ready to use device. The parameters which are trimmed are: gain, offset, common mode and internal clock frequency.

The trimming values are stored inside the device by a non volatile structure. Any time the device is turned on, the trimming parameters are downloaded into the registers to be employed during the normal operation.This allows the user to employ the device without any further calibration.

5 Application Hints

Figure 4. LIS3L02DQ Electrical Connection



The device core is supplied through Vdd line (Vdd typ=3.3V) while the I/O pads are supplied through Vdd_IO. Power supply decoupling capacitors (100 nF ceramic, 10 μF Al) should be placed as near as possible to the device (common design practice). All the voltage and ground supplies must be present at the same time to have proper behavior of the IC (refer to Fig 4).The functionality of the device and the measured acceleration data is selectable and accessible through the I^2C/SPI interface.When using the I^2C, CS must be tied high while SDO must be left floating.

5.1 Soldering Information

The QFN-44 package is lead free and green package qualified for soldering heat resistance according to JEDEC J-STD-020D. Land pattern and soldering recommendations are available upon request.

6 Digital Interfaces

The registers embedded inside the LIS3L02DQ may be accessed through both the I^2C and SPI serial interfaces. The latter may be software configured to operate either in SPI mode or in 3-wire interface mode.

The serial interfaces are mapped onto the same pads. To select the I^2C interface, CS line must be tied high (i.e connected to Vdd).

Table 6. Serial Interface Pin Description

PIN Name	PIN Description
CS	SPI enable I^2C/SPI mode selection (1: I^2C mode; 0: SPI enabled)
SCL/SPC	I^2C Serial Clock (SCL) SPI Serial Port Clock (SPC)
SDA/SDI/SDO	I^2C Serial Data (SDA) SPI Serial Data Input (SDI) 3-wire Interface Serial Data Output (SDO)
SDO	SPI Serial Data Output (SDO)

6.1 I^2C Serial Interface

The LIS3L02DQ I^2C is a bus slave. The I^2C is implemented in the way that the data can be written into the registers whose content can also be read back.

The relevant I^2C terminology is given in the table below:

Table 7. Serial Interface Pin Description

Term	Description
Transmitter	The device which sends data to the bus
Receiver	The device which receives data from the bus
Master	The device which initiates a transfer, generates clock signals and terminates a transfer
Slave	The device addressed by the master

There are two signals associated with the I^2C bus: the Serial Clock Line (SCL) and the Serial Data line (SDA). The latter is a bidirectional line used for sending and receiving the data to/from the interface. Both the lines are connected to Vdd through a pull-up resistor embedded inside the LIS3L02DQ. When the bus is free both lines are high.

The I^2C interface is compliant with Fast Mode (400 kHz) I^2C standards as well as the Normal Mode.

6.2 I^2C Operation

The transaction on the bus is started through a START signal. A START condition is defined as a HIGH to LOW transition on the data line while the SCL line is held HIGH. After this has been transmitted by the Master, the bus is considered busy. The next byte of data transmitted after the start condition contains the address of the slave in the first 7 bits and the eighth bit tells whether the Master is receiving data from the slave or transmitting data to the slave. When an address is sent, each device in the system compares the first seven bits after a start condition with its address. If they match, the device considers itself addressed by the Master.The Slave ADdress (SAD) associated to the LIS3L02DQ is 0011101.

It's mandatory to use "acknowledge" during data transfer. The transmitter must release the SDA line dur-

ing the acknowledge pulse. The receiver must then pull the data line LOW so that it remains stable low during the HIGH period of the acknowledge clock pulse. A receiver which has been addressed is obliged to generate an acknowledge after each byte of data has been received.

The I^2C embedded inside the LIS3L02DQ behaves like a slave device and the following protocol must be adhered to. After the start condition (ST) a slave address is sent, once a slave acknowledge has been returned, a 8-bit sub-address will be transmitted: the 7 LSB represent the actual register address while the MSB enables address autoincrement. If the MSB of the SUB field is 1, the SUB (register address) will be automatically incremented to allow multiple data read/write.

If the LSB of the slave address is '1' (read), a repeated START condition will have to be issued after the two sub-address bytes; if the LSB is '0' (write) the Master will transmit to the slave with direction unchanged.

Transfer when Master is writing one byte to slave

Master	ST	SAD + W		SUB		DATA		SP
Slave			SAK		SAK		SAK	

Transfer when Master is writing multiple bytes to slave:

Master	ST	SAD + W		SUB		DATA		DATA		SP
Slave			SAK		SAK		SAK		SAK	

Transfer when Master is receiving (reading) one byte of data from slave:

Master	ST	SAD + W		SUB		SR	SAD + R			NMAK	SP
Slave			SAK		SAK			SAK	DATA		

Transfer when Master is receiving (reading) multiple bytes of data from slave

Master	ST	SAD + W		SUB		SR	SAD + R			MAK
Slave			SAK		SAK			SAK	DATA	

Master	SR		MAK		NMAK	SP
Slave		DATA		DATA		

Data is transmitted in byte format. Each data transfer contains 8 bits. The number of bytes transferred per transfer is unlimited. Data is transferred with the Most Significant Bit (MSB) first. If a receiver can't receive another complete byte of data until it has performed some other function, it can hold the clock line, SCL LOW to force the transmitter into a wait state. Data transfer only continues when the receiver is ready for another byte and releases the data line. If a slave receiver doesn't acknowledge the slave address (i.e. it is not able to receive because it is performing some real time function) the data line must be left HIGH by the slave. The Master can then abort the transfer. A LOW to HIGH transition on the SDA line while the SCL line is HIGH is defined as a STOP condition. Each data transfer must be terminated by the generation of a STOP condition.

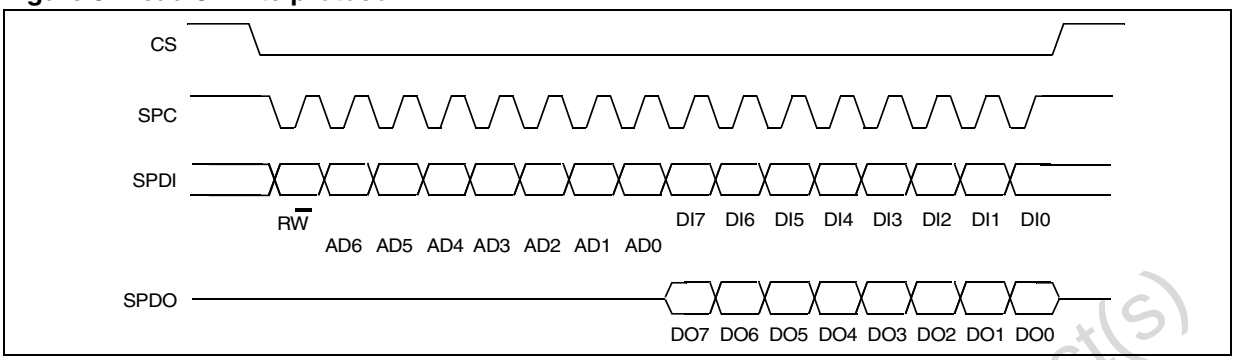
In order to read multiple bytes, it is necessary to assert the most significant bit of the sub-address field. In other words, SUB(7) must be equal to 1 while SUB(6-0) represents the address of first register to read.

6.3 SPI Bus Interface

The SPI interface present inside the LIS3L02DQ is a bus slave. The SPI allows to write and read the registers of the device. The Serial Interface interacts with the outer world with 4 wires: CS, SPC, SDI and SDO.The maximum frequency is related to the Vdd_IO supply voltage.In particular in the 2.4 V - 3.6 V range is 8 MHz while under 2.4 V is 4 MHz.

6.3.1 Read & Write registers

Figure 5. Read & write protocol



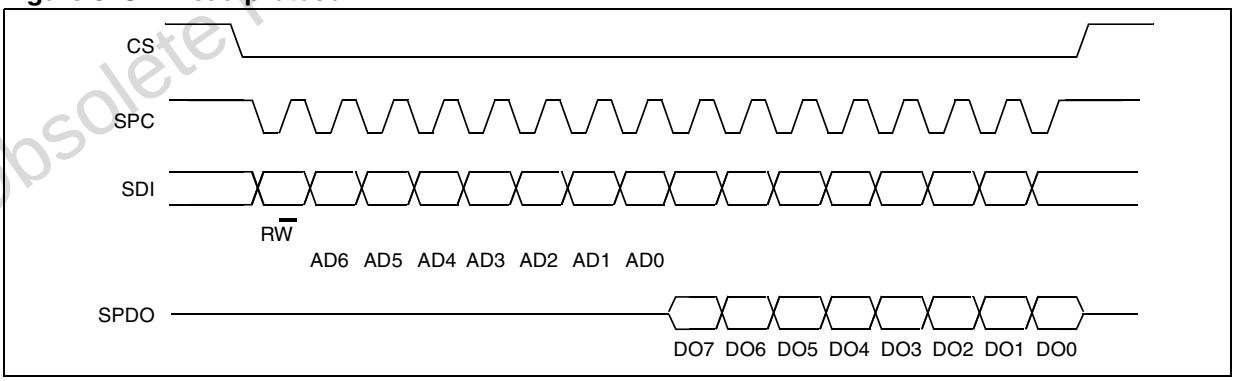
CS is the Serial Port Enable and it is controlled by the SPI master. It goes low at the start of the transmission and goes back high at the end. SPC is the Serial Port Clock and it is controlled by the SPI master. It is stopped high when CS is high (no transmission). SDI and SDO are respectively the Serial Port Data Input and Output. Those lines are driven at the falling edge of SPC and should be captured at the rising edge of SPC.

Both the Read Register and Write Register commands are completed in 16 clock pulses. Bit duration is the time between two falling edges of SPC. The first bit (bit 0) starts at the first falling edge of SPC after the falling edge of CS while the last bit (bit 15) starts at the last falling edge of SPC just before the rising edge of CS.

- bit 0: RW bit. When 0, the data DI(7:0) is written into the device. When 1, the data DO(7:0) from the device is read. In latter case, the chip will drive SDO at the start of bit 8.
- bit 1-7: address AD(6:0). This is the address field of the indexed register.
- bit 8-15: data DI(7:0) (write mode). This is the data that will be written into the device (MSB first).
- bit 8-15: data DO(7:0) (read mode). This is the data that will be read from the device (MSB first).

6.3.2 SPI Read

Figure 6. SPI Read protocol



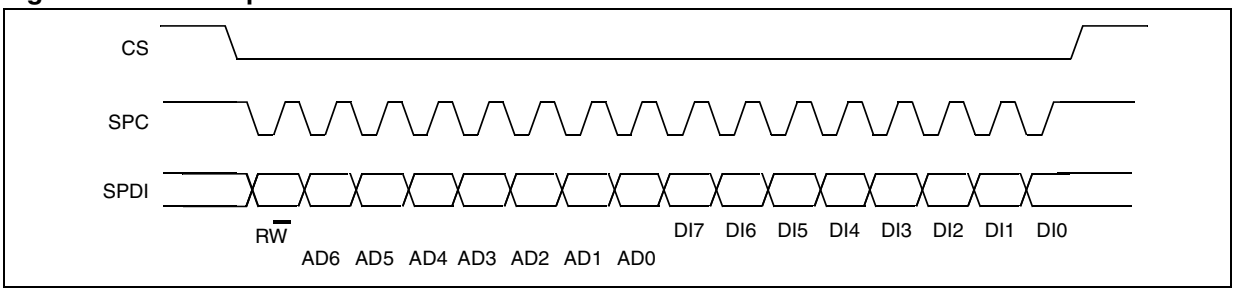
The SPI Read command consists of 16 clock pulses:

- bit 0: READ bit. The value is 1.

– bit 1-7: address AD(6:0). This is the address field of the indexed register.
– bit 8-15: data DO(7:0) (read mode). This is the data that will be read from the device (MSB first).

6.3.3 SPI Write

Figure 7. SPI Write protocol

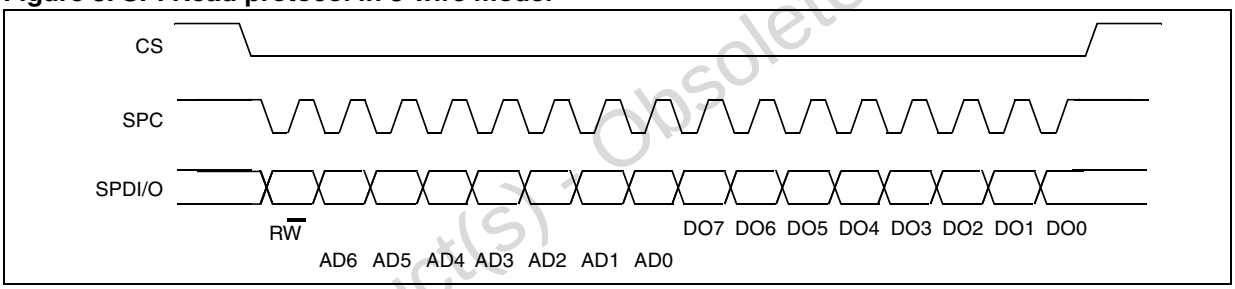


The SPI Write command consists of 16 clock pulses.
– bit 0: WRITE bit. The value is 0.
– bit 1-7: address AD(3:0). This is the address field of the indexed register.
– bit 8-15: data DI(7:0) (write mode). This is the data that will be written inside the device (MSB first).

6.3.4 SPI Read in 3-wire mode

3-wire mode is entered by setting SIM mode (SPI Serial Interface Mode selection) in CTRL_REG2.

Figure 8. SPI Read protocol in 3-wire model



The SPI Read command consists of 16 clock pulses:
– bit 0: READ bit. The value is 1.
– bit 1-7: address AD(6:0). This is the address field of the indexed register.
– bit 8-15: data DO(7:0) (read mode). This is the data that will be read from the device (MSB first).

7 Registers mapping

The table given below provides a listing of the registers embedded in the device and the related addresses.

Table 8. Registers address map

Reg. Name	Type	Register Address		Size (Bit)	Comment
		Binary	Hex		
		0000000 - 0010101	00 - 15		Reserved
OFFSET_X	rw	0010110	16	8	Loaded at boot
OFFSET_Y	rw	0010111	17	8	Loaded at boot
OFFSET_Z	rw	0011000	18	8	Loaded at boot
GAIN_X	rw	0011001	19	8	Loaded at boot
GAIN_Y	rw	0011010	1A	8	Loaded at boot
GAIN_Z	rw	0011011	1B	8	Loaded at boot
		0011100 - 0011111	1C - 1F		Reserved
CTRL_REG1	rw	0100000	20	8	
CTRL_REG2	rw	0100001	21	8	
		0100010	22		Reserved
WAKE_UP_CFG	rw	0100011	23	8	
WAKE_UP_SRC	r	0100100	24	8	
WAKE_UP_ACK	r	0100101	25	8	
		0100110	26		Reserved
STATUS_REG	rw	0100111	27	8	
OUTX_L	r	0101000	28	8	
OUTX_H	r	0101001	29	8	
OUTY_L	r	0101010	2A	8	
OUTY_H	r	0101011	2B	8	
OUTZ_L	r	0101100	2C	8	
OUTZ_H	r	0101101	2D	8	
THS_L	rw	0101110	2E	8	
THS_H	rw	0101111	2F	8	
		0110000 - 1111111	30 - 3F		Reserved

8 Registers Description

The device contains a set of registers which are used to control its behavior and to retrieve acceleration data. For normal mode operation it is not necessary to program offset and gain code as they are loaded at boot.

8.1 OFFSET_X (16h)

Offset of the three axes can be changed individually. It's represented in two's complement code

OX7	OX6	OX5	OX4	OX3	OX2	OX1	OX0

OX7, OX0	Digital Offset Trimming for X-Axis

8.2 OFFSET_Y (17h)

OY7	OY6	OY5	OY4	OY3	OY2	OY1	OY0

DOY7, DOY0	Digital Offset Trimming for Y-Axis

8.3 OFFSET_Z (18h)

OZ7	OZ6	OZ5	OZ4	OZ3	OZ2	OZ1	OZ0

OZ7, OZ0	Digital Offset Trimming for Z-Axis

8.4 GAIN_X (19h)

The gain/sensitivity of the three axes can be changed individually.The gain range covers 0/256.

GX7	GX6	GX5	GX4	GX3	GX2	GX1	GX0

GX7, GX0	Digital Gain Trimming for X-Axis

8.5 GAIN_Y (1Ah)

GY7	GY6	GY5	GY4	GY3	GY2	GY1	GY0

GY7, GY0	Digital Gain Trimming for Y-Axis

8.6 GAIN_Z (1Bh)

GZ7	GZ6	GZ5	GZ4	GZ3	GZ2	GZ1	GZ0

GZ7, GZ0	Digital Gain Trimming for Z-Axis

8.7 CTRL_REG1 (20h)

Control Register 1 and 2 allow to influence the signal chain and start up conditions as well as the communication setup.

PD1	PD0	DF1	DF0	ST	Zen	Yen	Xen

PD1, PD0	Power Down Control. Default value: 00 (00: power-down mode; x1,1x: normal mode)
DF1, DF0	Decimation Factor Control. Default value: 00 (00: decimate by 128; 01: decimate by 64; 10: decimate by 32; 11: decimate by 8)
ST	Self Test Enable.Default value: 0 (0: normal mode; 1: self-test enable)
Zen	Z-axis enable. Default value: 1 (0:channel disabled; 1: channel enabled)
Yen	Y-axis enable. Default value: 1 (0:channel disabled; 1: channel enabled)
Xen	X-axis enable. Default value: 1 (0:channel disabled; 1: channel enabled)

8.8 CTRL_REG2 (21h)

RES	BDU	BLE	BOOT	IEN	DRDY	SIM	DAS

RES	Reserved.Default value: 0 (The Default value must not be changed)
BDU	Block Data Update. Default value: 0 (0: continuous update; 1: output registers not updated until MSB and LSB reading)
BLE	Big/Little Endian selection. Default value: 0 (0: little endian; 1: big endian)
BOOT	Reboot memory content. Default value: 0 (0: normal mode; 1:reboot memory content)
IEN	Interrupt Enable. Default value: 0 (0: data ready on RDY pad; 1: int req on RDY pad)
DRDY	Enable Data-Ready generation. Default value: 0 (0:data-ready gen. disabled; 1: enable data-ready generation)
SIM	SPI Serial Interface Mode selection.Default value: 0 (0: 4-wire interface; 1: 3-wire interface)
DAS	Data Alignment Selection. Default value: 0 (0: 12 bit right justified; 1: 16 bit left justified)

8.9 WAKE_UP_CFG (23h)

AOI	LIR	ZHIE	ZLIE	YHIE	YLIE	XHIE	XLIE

AOI	And/Or combination of Interrupt events. Default value: 0 (0: OR combination of interrupt events; 1: AND combination of interrupt events)
LIR	Latch interrupt request into WAKE_UP_SOURCE reg with the WAKE_UP_SOURCE reg cleared by reading WAKE_UP_ACK reg. (0: interrupt request non latched 1: interrupt request latched)
ZHIE	Enable interrupt generation on Z high event. Default value:0 (o: disable interrupt request;1: enable int req on measured accel. value higher than preset threshold)
ZLIE	Enable interrupt generation on Z low event. Default value:0 (0: disable interrupt request; 1: enable int req on measured accel. value higher than preset threshold)
YHIE	Enable interrupt generation on Y high event. Default value:0 (0: disable interrupt request; 1: enable int req on measured accel. value higher than preset threshold)
YLIE	Enable interrupt generation on Y low event. Default value:0 (0: disable interrupt request; 1: enable int req on measured accel. value higher than preset threshold)
XHIE	Enable interrupt generation on X high event. Default value:0 (0: disable interrupt request; 1: enable int req on measured accel. value higher than preset threshold)
XLIE	Enable interrupt generation on X low event. Default value:0 (0: disable interrupt request; 1: enable int req on measured accel. value higher than preset threshold)

8.10 WAKE_UP_SOURCE (24h)

x	IA	ZH	ZL	YH	YL	XH	XL

IA	Interrupt Active.Default value:0 (0: no interrupt has been generated; 1:one or more interrupt event has been generated)
ZH	Z High. Default value: 0 (0: no interrupt; 1:ZH event has occurred)
ZL	Z Low.Default value: 0 (0: no interrupt; 1:ZL event has occurred)
YH	Y High. Default value: 0 (0: no interrupt; 1:YH event has occurred)
YL	Y Low. Default value: 0 (0: no interrupt; 1:ZH event has occurred)
XH	X High. Default value: 0 (0: no interrupt; 1:XH event has occurred)
XL	X Low. Default value: 0 (0: no interrupt; 1:XL event has occurred)

8.11 WAKE_UP_ACK (25h)

Reading at this address resets the **WAKE_UP_SOURCE** register.

8.12 A_STATUS_REG (27h)

ZYXOR	ZOR	YOR	XOR	ZYXDA	ZDA	YDA	XDA

ZYXOR	X, Y and Z axis Data Overrun
ZOR	Z axis Data Overrun
YOR	Y axis Data Overrun
XOR	X axis Data Overrun
ZYXDA	X, Y and Z axis new Data Available
ZDA	Z axis new Data Available
YDA	Y axis new Data Available
XDA	X axis new Data Available

8.13 OUTX_L (28h)

XD7	XD6	XD5	XD4	XD3	XD2	XD1	XD0

XD7, XD0	X axis acceleration data LSB

8.14 OUTX_H (29h)

When reading the register in “12 bit right justified” mode the most significant bits (7:4) are replaced with bit 3 (i.e. XD15-XD12=XD11, XD11, XD11, XD11).

XD15	XD14	XD13	XD12	XD11	XD10	XD9	XD8

XD15, XD8	X axis acceleration data MSB

8.15 OUTY_L (2Ah)

YD7	YD6	YD5	YD4	YD3	YD2	YD1	YD0

YD7, YD0	Y axis acceleration data LSB

8.16 OUTY_H (2Bh)

When reading the register in “12 bit right justified” mode the most significant bits (7:4) are replaced with bit 3 (i.e. YD15-YD12=YD11, YD11, YD11, YD11).

YD15	YD14	YD13	YD12	YD11	YD10	YD9	YD8

YD15, YD8	Y axis acceleration data MSB

8.17 OUTZ_L (2Ch)

ZD7	ZD6	ZD5	ZD4	ZD3	ZD2	ZD1	ZD0

ZD7, ZD0	Z axis acceleration data LSB

8.18 OUTZ_H (2Dh)

When reading the register in “12 bit right justified” mode the most significant bits (7:4) are replaced with bit 3 (i.e. ZD15-ZD12=ZD11, ZD11, ZD11, ZD11).

ZD15	ZD14	ZD13	ZD12	ZD11	ZD10	ZD9	ZD8

ZD15, ZD8	Z axis acceleration data MSB

8.19 THS_L (2Eh)

The registers THS_L and THS_H contain the upper and lower threshold that is valid for all three axes.

Each axis can be enabled/disabled for interrupt generation and upper/lower limits crossing can be used for interrupt generation on a channel by channel basis

THS7	THS6	THS5	THS4	THS3	THS2	THS1	THS0

THS7, THS0	Inertial Wake Up Acceleration Threshold Lsb

8.20 THS_H (2Fh)

THS15	THS14	THS13	THS12	THS11	THS10	THS9	THS8

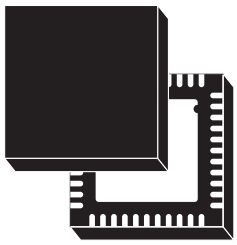
THS15, THS8	Inertial Wake Up Acceleration Threshold Msb

9 Package Information

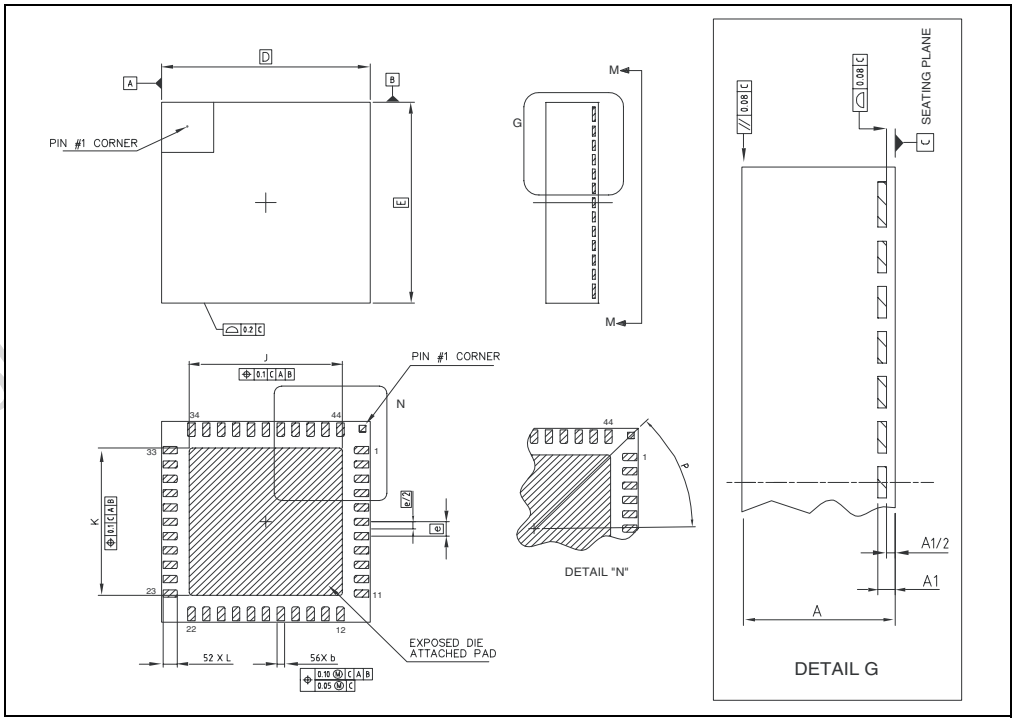
Figure 9. QFN-44 Mechanical Data & Package Dimensions

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	1.70	1.80	1.90	0.067	0.071	0.075
A1	0.19		0.21	0.007		0.008
b	0.20	0.25	0.30	0.008	0.01	0.012
D		7.0			0.276	
E		7.0			0.276	
e		0.50			0.020	
J	5.04		5.24	0.198		0.206
K	5.04		5.24	0.198		0.206
L	0.38	0.48	0.58	0.015	0.019	0.023
P		45 REF			45 REF	

OUTLINE AND MECHANICAL DATA



QFN-44 (7x7x1.8mm)
Quad **F**lat **P**ackage **N**o lead



10 Revision History

Table 9. Revision History

Date	Revision	Description of Changes
February 2004	1	First Issue
January 2005	2	Changed the Operating Temperature range: from -40°C to +85°C to -20°C to +70°C. Changed some data on the Table 3 Electrical Characteristics. Changed the section 6.8 CTRL_REG2 (21h).
20 January, 2005	3	The title in first page has been changed as the following: INERTIAL SENSOR: 3-Axis - 2g DIGITAL OUTPUT LINEAR ACCELEROMETER
May 2005	4	Revision of parameters. Major paragraph rearrangement.

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