

## EMIF08-1502M16

8-line IPAD™

low capacitance EMI filter and ESD protection in micro QFN package

#### **Features**

- EMI (I/O) low-pass filter
- High efficiency in EMI filtering:
  - Greater than 30 dB attenuation at frequencies from 900 MHz to 1.8 GHz
- Cut-off frequency: 300 MHz
- Very low PCB space consumption:3.3 mm x 1.5 mm
- Very thin package: 0.6 mm max.
- High efficiency in ESD suppression on inputs pins (IEC 61000-4-2 level 4)
- High reliability offered by monolithic integration
- High reduction of parasitic elements through integration
- Lead-free package

#### Complies with following standards:

- IEC 61000-4-2 level 4 input pins
  - 15 kV (air discharge)
  - 8 kV (contact discharge)
- MIL STD 883G Method 3015-7 Class 3A (all pins)

### **Applications**

Where EMI filtering in ESD sensitive equipment is required:

- LCD and camera for Mobile phones
- Computers and printers
- Communication systems
- MCU boards

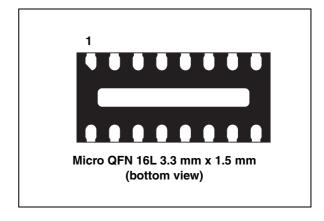
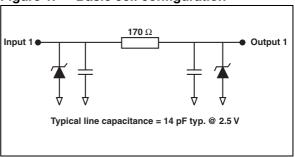


Figure 1. Basic cell configuration



### **Description**

The EMIF08-1502M16 is an 8-line, highly integrated device designed to suppress EMI/RFI noise in all systems exposed to electromagnetic interference.

This filter includes an ESD protection circuitry, which prevents damage to the application when subjected to ESD surges up to 15 kV on the input pins.

TM: IPAD is a trademark of STMicroelectronics

Characteristics EMIF08-1502M16

## 1 Characteristics

Figure 2. Pin configuration (top view)

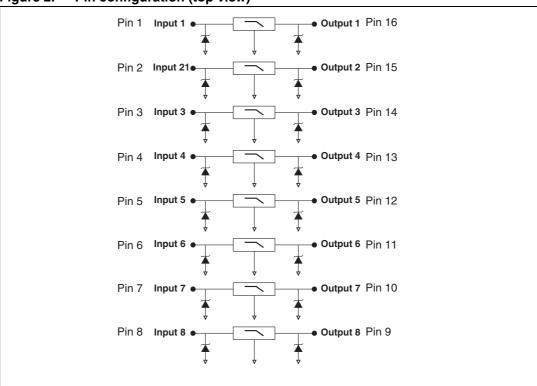


Table 1. Absolute ratings (limiting values)

Symbol	Parameter	Value	Unit			
	ESD IEC 61000-4-2, air discharge on input pins	15				
$V_{PP}$	ESD IEC 61000-4-2, contact discharge on input pins	8	kV			
	ESD IEC 61000-4-2, contact discharge on output pins	4				
Tj	Maximum junction temperature	125	°C			
T <sub>op</sub>	Operating temperature range	- 40 to + 85	°C			
T <sub>stg</sub>	Storage temperature range	- 55 to + 150	°C			

EMIF08-1502M16 Characteristics

Table 2. Electrical characteristics ( $T_{amb} = 25$  °C)

Symbol		Parameter		¹↑ .				
$V_{BR}$	Breakdow	n voltage		I <sub>F</sub>				
I <sub>RM</sub>	Leakage (	current @ V <sub>RM</sub>						
$V_{RM}$	Stand-off	voltage	V <sub>BR</sub>	V <sub>BR</sub> V <sub>CL</sub> V <sub>RM</sub> I <sub>RM</sub> V <sub>F</sub> V <sub>C</sub>				
V <sub>CL</sub>	Clamping	voltage	V <sub>CL</sub> V					
$R_d$	Dynamic	resistance	ſ		I <sub>R</sub>			
I <sub>PP</sub>	Peak puls	e current						
R <sub>I/O</sub>	Series res	sistance between Input & Output	ļ		I <sub>PP</sub>			
C <sub>line</sub>	Input capa	acitance per line	1					
Symbol Test conditions			Min.	Тур.	Max.	Unit		
$V_{BR}$		I <sub>R</sub> = 1 mA		6	8	10	٧	
V <sub>F</sub>			0.5	1.0	1.5	٧		
I <sub>RM</sub> V <sub>RM</sub> = 3 V per line					100	nA		

Figure 3. S21 attenuation measurement

 $R_{I\!/\!O}$ 

 $C_{\text{line}}$ 

Tolerance ± 10%

 $V_{LINE}$  = 2.5 V dc,  $V_{OSC}$  = 30 mV, F = 1 MHz

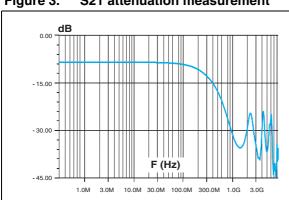


Figure 4. Analog cross talk measurements

170

187

16.5

Ω

153

12

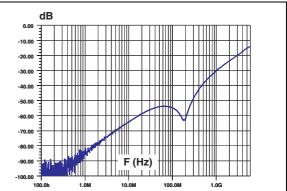


Figure 5. ESD response to IEC 61000-4-2 (+15 kV air discharge) on one input (V<sub>in</sub>) and on one output (V<sub>out</sub>)

Figure 6. ESD response to IEC 61000-4-2 (- 15 kV air discharge) on one input (V<sub>in</sub>) and on one output (V<sub>out</sub>)

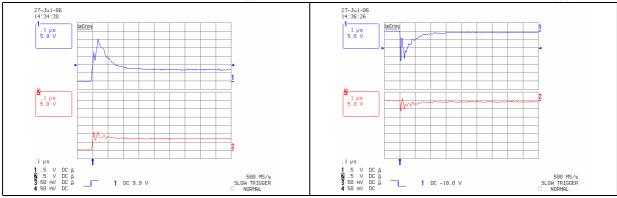
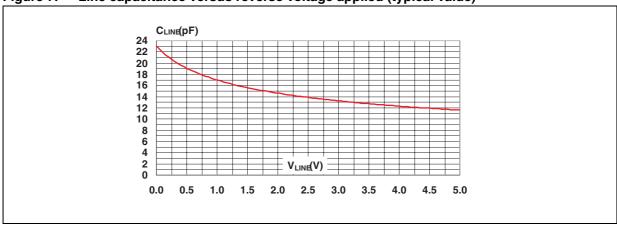
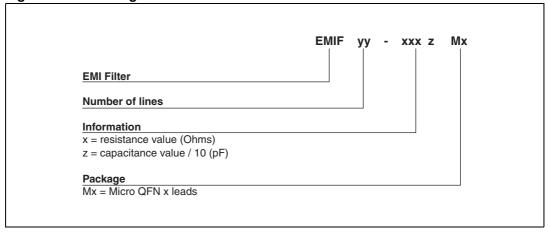


Figure 7. Line capacitance versus reverse voltage applied (typical value)



# 2 Ordering information scheme

Figure 8. Ordering information scheme



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Package information EMIF08-1502M16

#### 3 **Package information**

#### Epoxy meets UL94, V0

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at www.st.com.

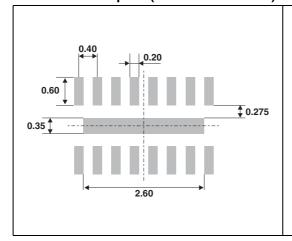
Micro QFN 3.3x1.5 16L dimensions Table 3.

TOP VIEW  D  INDEX AREA (0/2 x 8/2)
SIDE VIEW
BOTTOM VIEW  e  NOFYARFA    de   de   de   de   de   de   de   d
NOEXABEA (D/2 x E/Z)  PIN # 1 ID  D2  K

	Dimensions							
Ref.	Mi	illimete	ers	Inches				
	Min.	Тур.	Max.	Min.	Тур.	Max.		
Α	0.50	0.55	0.60	0.020	0.022	0.024		
A1	0.00	0.02	0.05	0.000	0.001	0.002		
b	0.15	0.20	0.25	0.006	0.008	0.010		
D	3.20	3.30	3.40	0.126	0.130	0.134		
D2	2.45	2.60	2.70	0.096	0.102	0.106		
Е	1.40	1.50	1.60	0.055	0.059	0.063		
E2	0.20	0.35	0.45	0.008	0.014	0.018		
е		0.40			0.016			
K	0.20			0.008				
L	0.20	0.30	0.40	0.008	0.012	0.016		

Figure 9. Micro QFN 3.3x1.5 16L footprint (dimensions in mm)

Figure 10. Marking



Dot: Pin 1 Identification X X= Marking WW= DataCode (week) Y=Data code(Year) P=Assembly plant



Package information EMIF08-1502M16

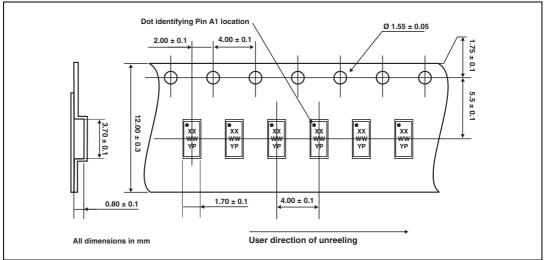


Figure 11. Tape and reel specification

Note:

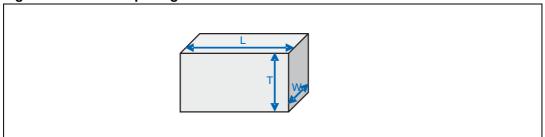
Product marking may be rotated by 90° for assembly plant differentiation. In no case should this product marking be used to orient the component for its placement on a PCB. Only pin 1 mark is to be used for this purpose.

## 4 Recommendation on PCB assembly

## 4.1 Stencil opening design

- 1. General recommendation on stencil opening design
  - a) Stencil opening dimensions: L (Length), W (Width), T (Thickness).

Figure 12. Stencil opening dimensions



b) General design rule

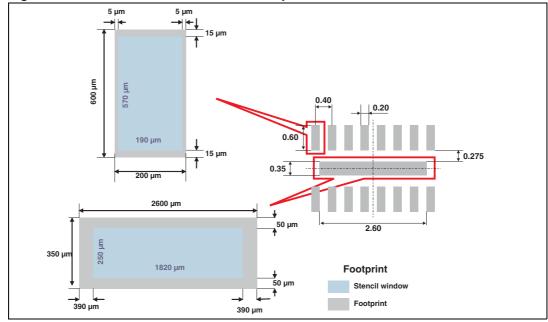
Stencil thickness (T) = 75 
$$\sim$$
 125  $\mu m$ 

Aspect Ratio = 
$$\frac{W}{T} \ge 1.5$$

Aspect Area = 
$$\frac{L \times W}{2T(L+W)} \ge 0.66$$

- 2. Reference design
  - a) Stencil opening thickness: 100 µm
  - b) Stencil opening for central exposed pad: Opening to footprint ratio is 50%.
  - c) Stencil opening for leads: Opening to footprint ratio is 90%.

Figure 13. Recommended stencil window position



### 4.2 Solder paste

- 1. Halide-free flux qualification ROL0 according to ANSI/J-STD-004.
- 2. "No clean" solder paste is recommended.
- 3. Offers a high tack force to resist component movement during high speed
- 4. Solder paste with fine particles: powder particle size is 20-45 μm.

#### 4.3 Placement

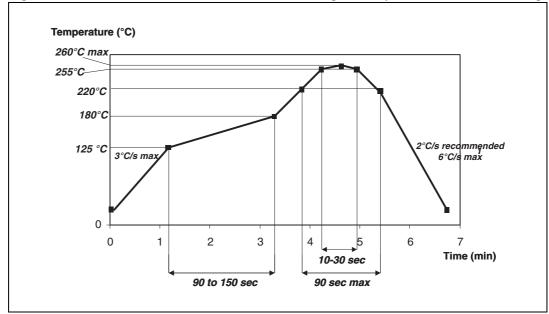
- 1. Manual positioning is not recommended.
- 2. It is recommended to use the lead recognition capabilities of the placement system, not the outline centering
- 3. Standard tolerance of  $\pm$  0.05 mm is recommended.
- 4. 3.5 N placement force is recommended. Too much placement force can lead to squeezed out solder paste and cause solder joints to short. Too low placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or badly centered packages.
- To improve the package placement accuracy, a bottom side optical control should be performed with a high resolution tool.
- For assembly, a perfect supporting of the PCB (all the more on flexible PCB) is recommended during solder paste printing, pick and place and reflow soldering by using optimized tools.

### 4.4 PCB design preference

- 1. To control the solder paste amount, the closed via is recommended instead of open vias.
- 2. The position of tracks and open vias in the solder area should be well balanced. The symmetrical layout is recommended, in case any tilt phenomena caused by asymmetrical solder paste amount due to the solder flow away.

## 4.5 Reflow profile

Figure 14. ST ECOPACK® recommended soldering reflow profile for PCB mounting



Note: Minimize air convection currents in the reflow oven to avoid component movement.

# 5 Ordering information

Table 4. Ordering information

Order code	Marking	Package	Weight	Base qty	Delivery mode
EMIF08-1502M16	G8 <sup>(1)</sup>	Micro QFN	7.2 mg	3000	Tape and reel (7")

<sup>1.</sup> The marking can be rotated by  $90^{\circ}$  to differentiate assembly location

## 6 Revision history

Table 5. Document revision history

Date	Revision	Changes
24-Oct-2006	1	Initial release.
04-Feb-2008	2	Reformatted to current standards. Updated ECOPACK statement. Added Section 4: Recommendation on PCB assembly.

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