

4-line bidirectional Transil™, transient voltage surge suppressor for ESD protection

Datasheet – production data

Features

- 4 bidirectional Transil diodes
- Breakdown voltage $V_{BR} = 5.5 \text{ V min.}$
- Low leakage current $< 60 \text{ nA}$
- Very small PCB area: 0.8 mm^2
- $400 \mu\text{m}$ pitch micro-package
- Lead-free and RoHS package

Complies with the following standards

- IEC 61000-4-2 level 4
 - 15 kV (air discharge)
 - 8 kV (contact discharge)

Applications

Where transient overvoltage protection in ESD sensitive equipment is required, such as:

- Mobile phones
- Portable multimedia devices and accessories
- Computers, tablets and peripherals
- Set top boxes
- Audio equipment

Description

The ESDALC5-4BN4 is a monolithic array designed to protect up to 4 bidirectional lines against ESD transients.

The device is ideal for applications where both reduced printed circuit board space and high ESD protection levels are required.

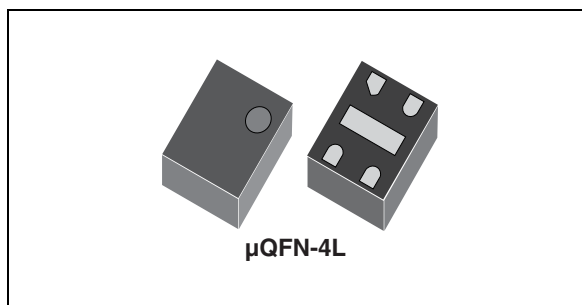
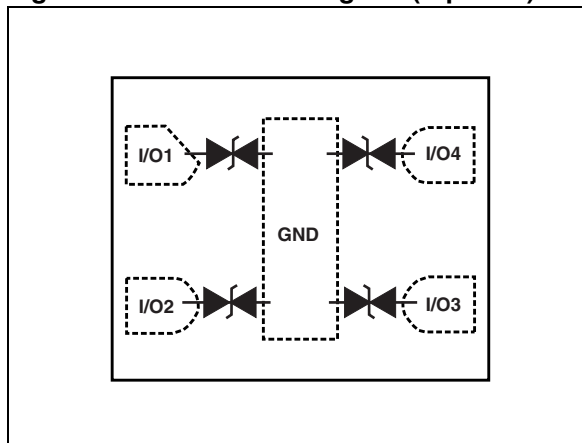


Figure 1. Functional diagram (top view)



1 Characteristics

Table 1. Absolute maximum ratings ($T_{amb} = 25\text{ }^{\circ}\text{C}$)

Symbol	Parameter	Value	Unit	
V_{PP}	Peak pulse voltage, IEC 61000-4-2, level 4: Contact discharge	30	kV	
	Air discharge	30		
I_{pp}	Peak pulse current (8/20 μs)	4	A	
P_{PP}	Peak pulse power dissipation (8/20 μs) ⁽¹⁾	GND to I/O	60	W
T_j	Operating junction temperature range	-40 to 125	$^{\circ}\text{C}$	
T_{stg}	Storage temperature range	-65 + 150	$^{\circ}\text{C}$	
T_L	Maximum lead temperature for soldering during 10 s	260	$^{\circ}\text{C}$	

1. For a surge greater than the maximum values, the diode will fail in short-circuit.

Figure 2. Electrical characteristics (definitions)

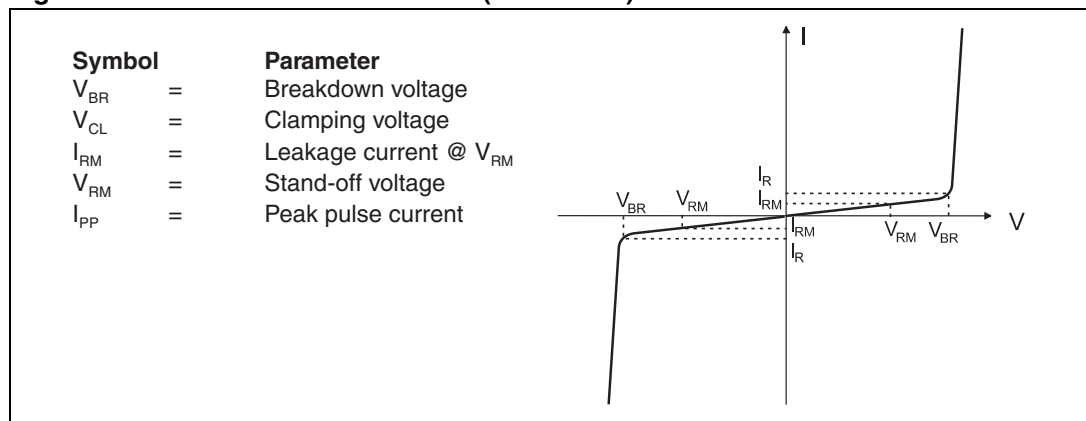


Table 2. Electrical characteristics (values, $T_{amb} = 25\text{ }^{\circ}\text{C}$)

Symbol	Test conditions	Min.	Typ.	Max.	Unit
V_{BR}	$I_R = 1\text{ mA}$, I/O to GND	11	13		V
	$I_R = 1\text{ mA}$, GND to I/O	5.5	8		
I_{RM}	$V_{RM} = 5\text{ V}$		1	60	nA
V_{CL}	$I_{pp} = 1\text{ A}$, 8/20 μs , I/O to GND			18	V
	$I_{pp} = 1\text{ A}$, 8/20 μs , GND to I/O			14.5	
C_{LINE}	$V_R = 0\text{ V}$, $F = 1\text{ MHz}$, $V_{osc} = 30\text{ mV}$		13	15	pF

Figure 3. Leakage current versus junction temperature (typical values)

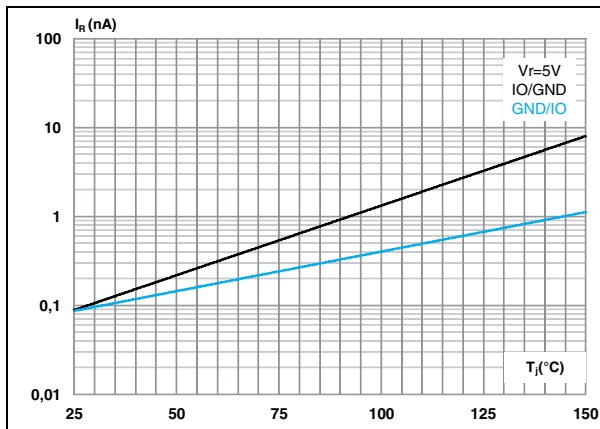


Figure 4. Junction capacitance versus reverse voltage applied (typical values)

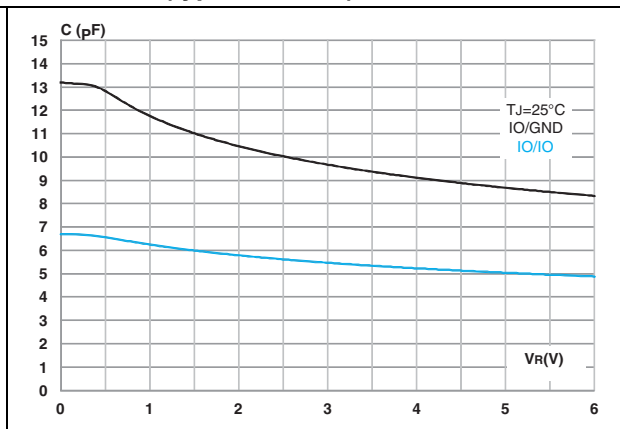


Figure 5. ESD response to IEC 61000-4-2 (+8 kV contact discharge)

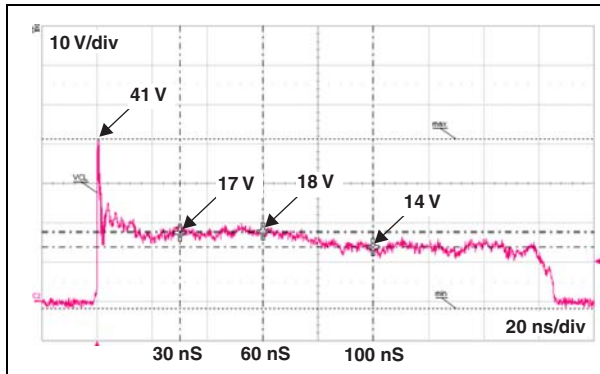


Figure 6. ESD response to IEC 61000-4-2 (-8 kV contact discharge)

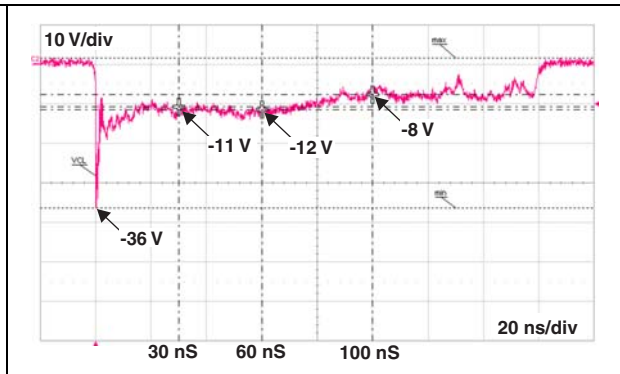


Figure 7. S21 attenuation measurements

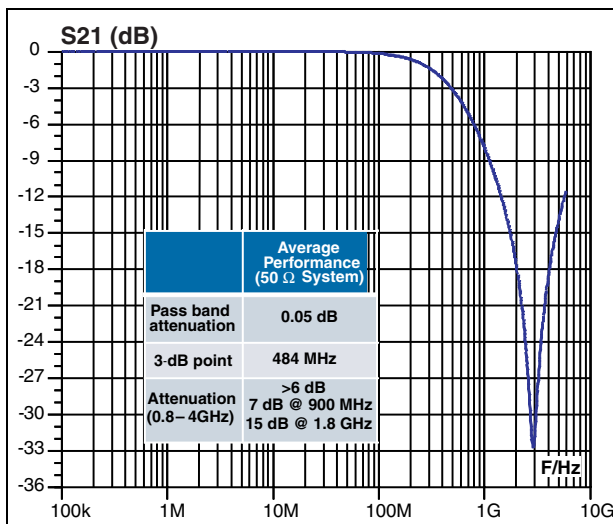
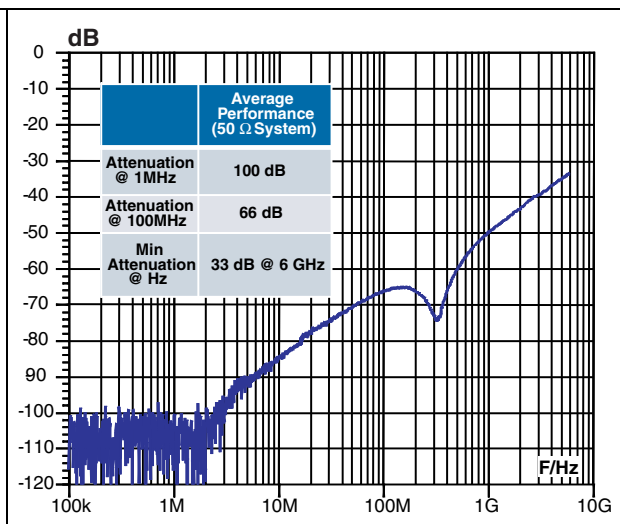
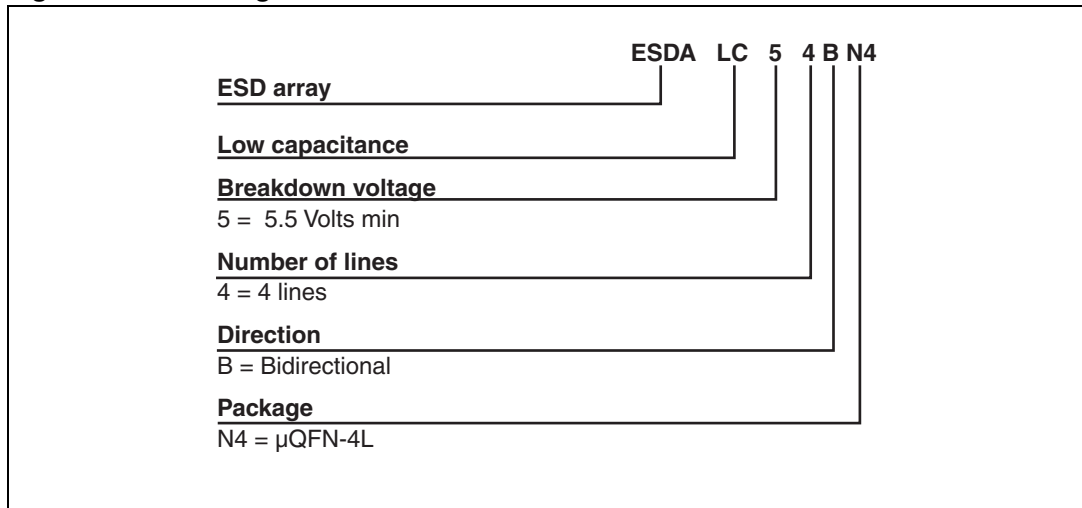


Figure 8. Analog crosstalk measurements between channels



2 Ordering information scheme

Figure 9. Ordering information scheme



3 Package information

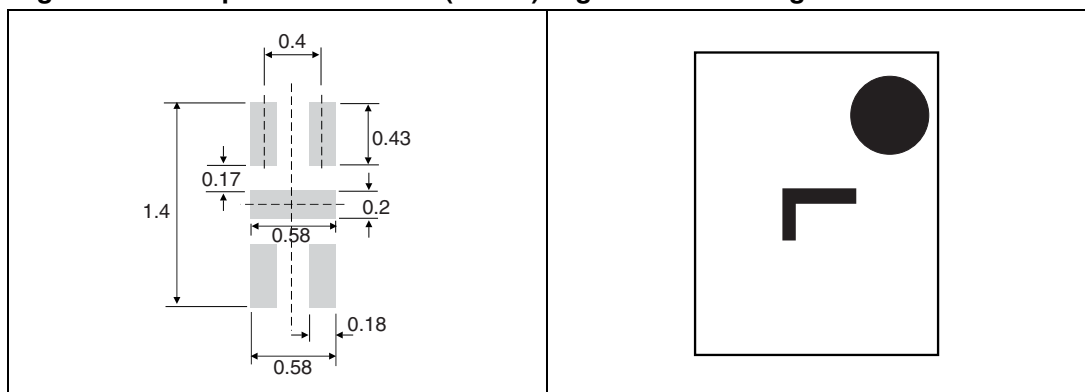
- Epoxy meets UL94, V0
- Lead-free package

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Table 3. μQFN-4L dimensions

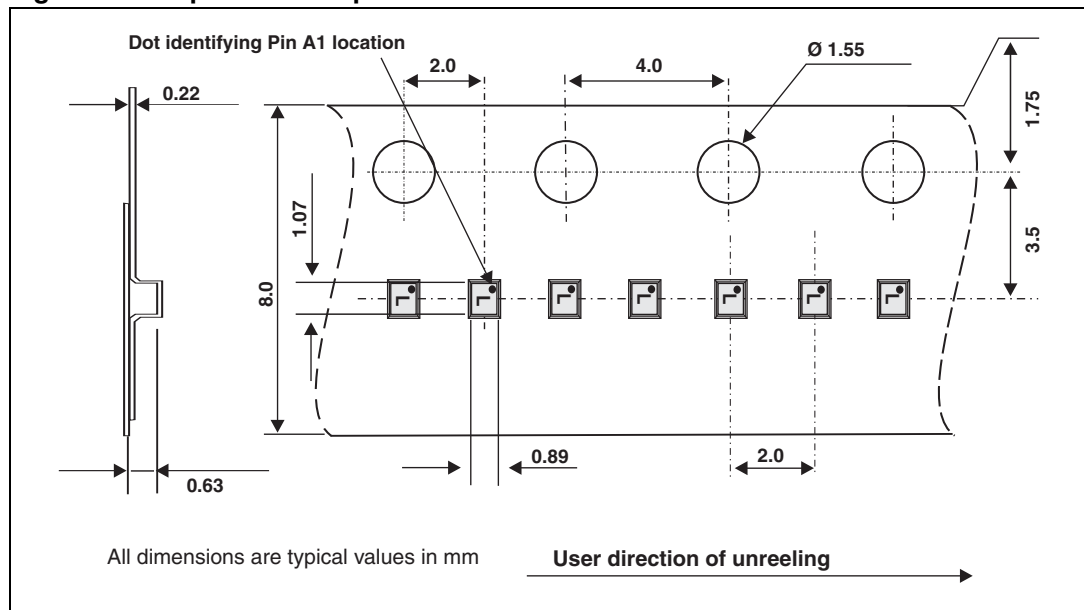
Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.31	0.38	0.40	0.012	0.015	0.016
A1	0.00	0.02	0.05	0.00	0.0008	0.002
b	0.10	0.15	0.20	0.004	0.006	0.008
D	0.70	0.80	0.90	0.028	0.031	0.035
D2	0.50	0.58	0.65	0.020	0.023	0.026
e	0.35	0.40	0.45	0.014	0.016	0.018
E	0.90	1.00	1.10	0.035	0.039	0.043
E2	0.15	0.20	0.25	0.006	0.008	0.010
L	0.18	0.23	0.28	0.007	0.009	0.011
L1	0.00	-	0.05	0.00	-	0.002

Figure 10. Footprint dimensions (in mm) Figure 11. Marking



Note: Product marking may be rotated by multiples of 90° for assembly plant differentiation. In no case should this product marking be used to orient the component for its placement on a PCB. Only pin 1 mark is to be used for this purpose.

Figure 12. Tape and reel specifications



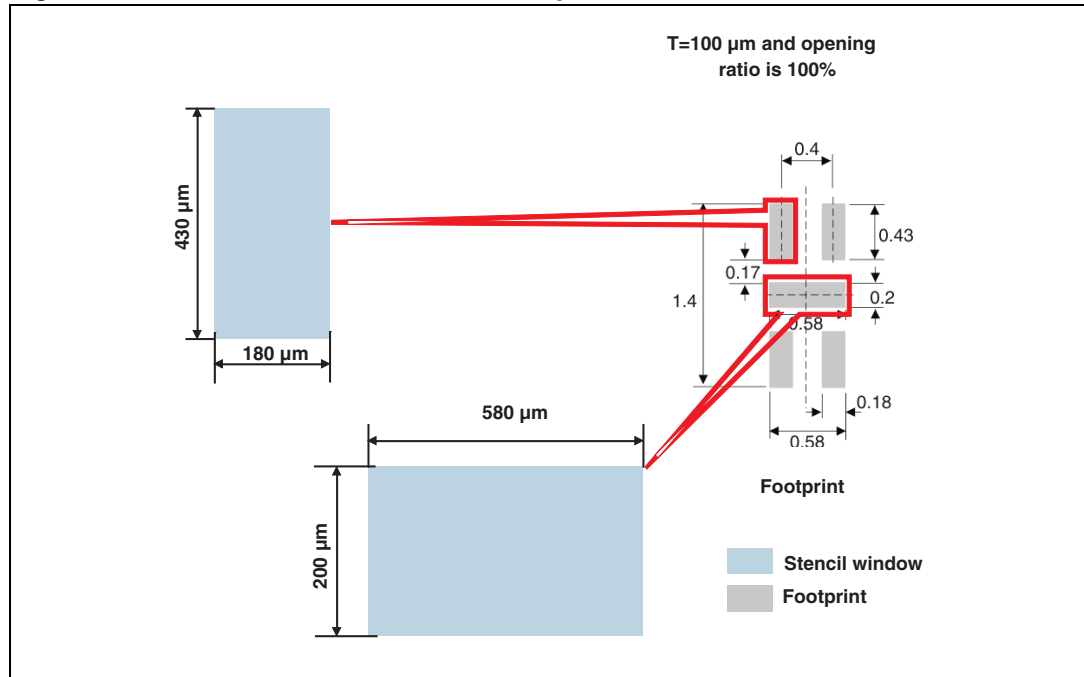
4 Recommendation on PCB assembly

4.1 Stencil opening design

Reference design

- Stencil opening thickness: 100 μm
- Stencil opening for leads: Opening to footprint ratio is 100%.

Figure 13. Recommended stencil window position



4.2 Solder paste

1. Halide-free flux qualification ROL0 according to ANSI/J-STD-004.
2. "No clean" solder paste is recommended.
3. Offers a high tack force to resist component movement during high speed.
4. Solder paste with fine particles: powder particle size is 20-45 μm .

4.3 Placement

1. Manual positioning is not recommended.
2. It is recommended to use the lead recognition capabilities of the placement system, not the outline centering.
3. Standard tolerance of ± 0.05 mm is recommended.

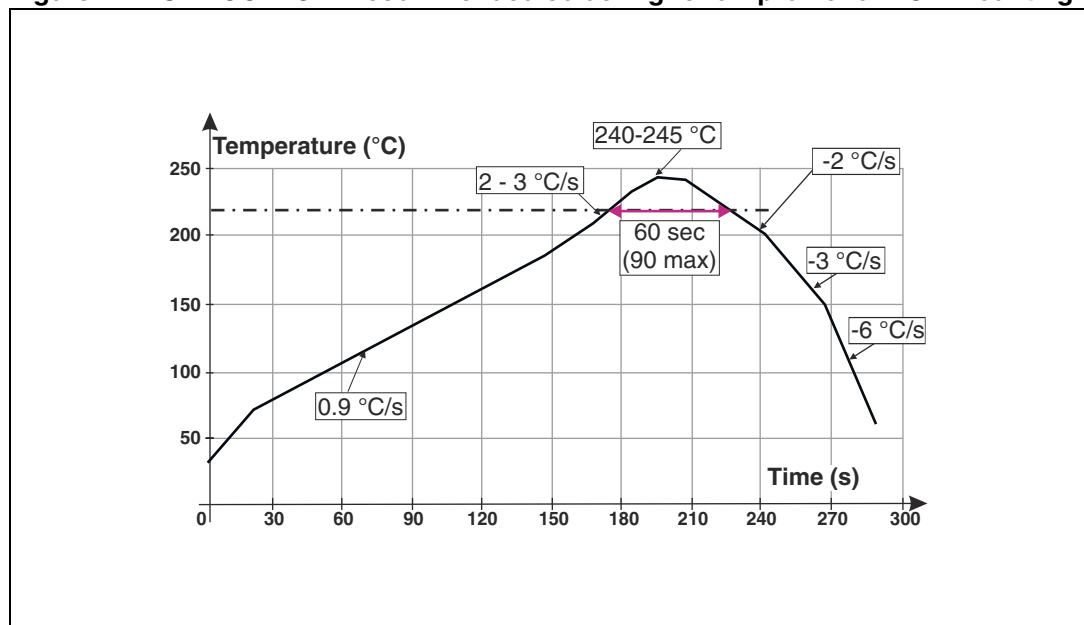
4. 3.5 N placement force is recommended. Too much placement force can lead to squeezed out solder paste and cause solder joints to short. Too low placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or badly centered packages.
5. To improve the package placement accuracy, a bottom side optical control should be performed with a high resolution tool.
6. For assembly, a perfect supporting of the PCB (all the more on flexible PCB) is recommended during solder paste printing, pick and place and reflow soldering by using optimized tools.

4.4 PCB design preference

1. To control the solder paste amount, the closed via is recommended instead of open vias.
2. The position of tracks and open vias in the solder area should be well balanced. The symmetrical layout is recommended, in case any tilt phenomena caused by asymmetrical solder paste amount due to the solder flow away.

4.5 Reflow profile

Figure 14. ST ECOPACK® recommended soldering reflow profile for PCB mounting



Note: Minimize air convection currents in the reflow oven to avoid component movement.

5 Ordering information

Table 4. Ordering information

Order code	Marking	Package	Weight	Base qty	Delivery mode
ESDALC5-4BN4	L ⁽¹⁾	μQFN-4L	0.77 mg	10 000	Tape and reel

1. The marking can be rotated by multiples of 90° to differentiate assembly location

6 Revision history

Table 5. Document revision history

Date	Revision	Changes
18-Jan-2013	1	Initial release.

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