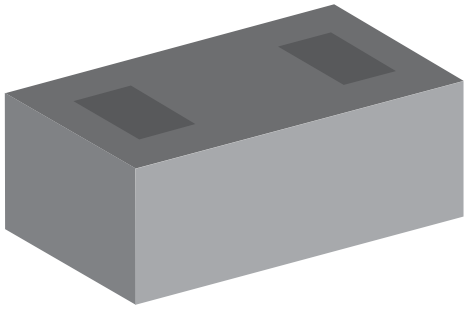
ESDAVLC6-1BV2

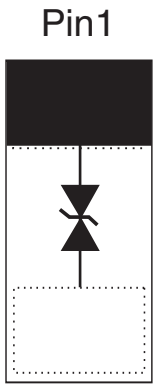
Single line low capacitance Transil™ for ESD protection

Datasheet – production data



ST01005
ESDAVLC6-1BV2

Figure 1. Functional diagram



Features

- PCB area: 0.09 mm²
- Bidirectional device
- Low capacitance: 8 pF max.
- Minimum breakdown voltage V_{BR} = 6 V
- Low leakage current: lower than 50 nA at 3 V
- RoHS compliant

Applications

Where transient over voltage protection in ESD sensitive equipment is required, such as:

- Portable multimedia devices and accessories
- MID, netbooks and notebooks
- Digital cameras and camcorders
- Communication systems
- Smart phones and accessories

Description

The ESDAVLC6-1BV2 is a single line bidirectional Transil diode designed specially for the protection of integrated circuits in portable equipment and miniaturized electronic devices subject to ESD transient overvoltage.

The device is ideal for applications where both reduced printed circuit board space and high ESD protection levels are required.

TM: Transil is a trademark of STMicroelectronics

1 Characteristics

Table 1. Absolute maximum ratings (T_{amb} = 25 °C)

Symbol	Parameter		Value	Unit
V_{PP}	Peak pulse voltage	IEC 61000-4-2 contact discharge IEC 61000-4-2 air discharge	12 15	kV
I_{PP}	Peak pulse current (8/20 µs)(1)		2.5	A
P_{PP}	Peak pulse power (8/20 µs)(1)		45	W
T_j	Operating temperature range		-55 to +150	°C
T_{stg}	Storage temperature range		- 65 to +150	°C
T_L	Maximum lead temperature for soldering during 10 s		260	°C

1. For a surge greater than the maximum values, the diode will fail in short-circuit.

Figure 2. Electrical characteristics (definitions)

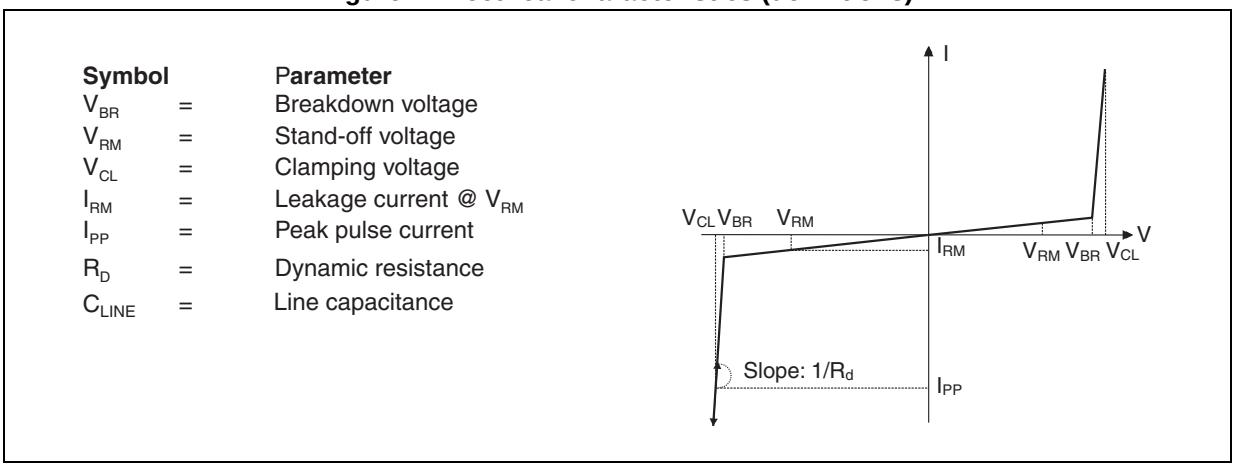


Table 2. Electrical characteristics (values, T_{amb} = 25 °C)

Symbol	Parameter	Test conditions	Value			Unit
			Min.	Typ.	Max.	
V_{BR}	Breakdown voltage	I_R = 1 mA	6			V
I_{RM}	Leakage current	V_{RM} = 3 V			50	nA
V_{CL}	Clamping voltage	I_{PP} = 1 A, 8/20 µs			12	V
		I_{PP} = 2.5 A maximum, 8/20 µs			18	
C_{line}	Line capacitance, I/O to GND	V_R = 0 V, F = 1 MHz, V_{osc} = 30 mV		7.5	8	pF
R_d	Dynamic resistance, pulse width 100 ns	I/O to GND		1.43		Ω
		GND to I/O		1.38		

Figure 3. ESD response to IEC 61000-4-2 (typical values, +8 kV contact discharge)

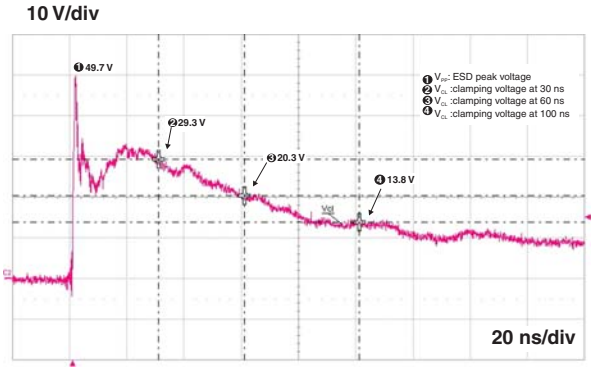


Figure 4. ESD response to IEC 61000-4-2 (typical values, -8 kV contact discharge)

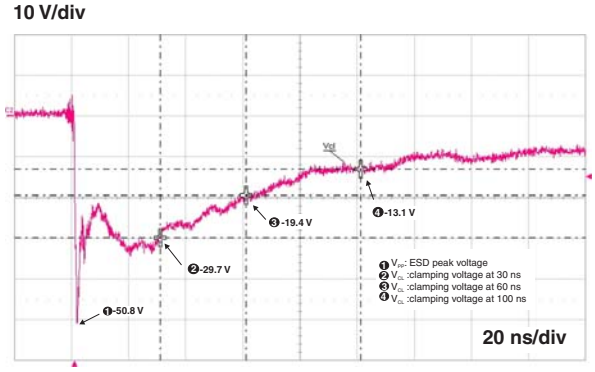


Figure 5. S21 attenuation measurement

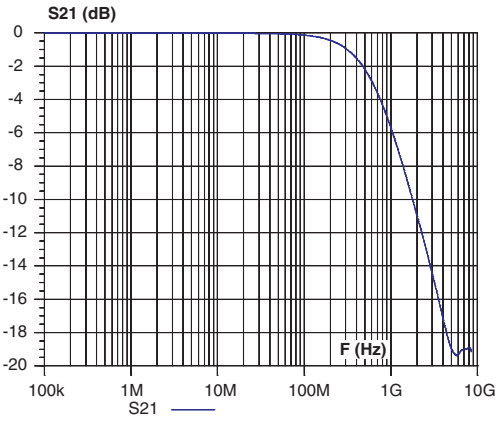


Figure 6. Junction capacitance versus reverse applied voltage (typical values)

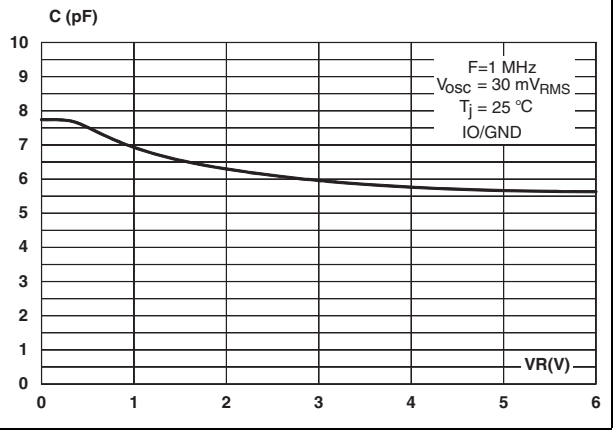
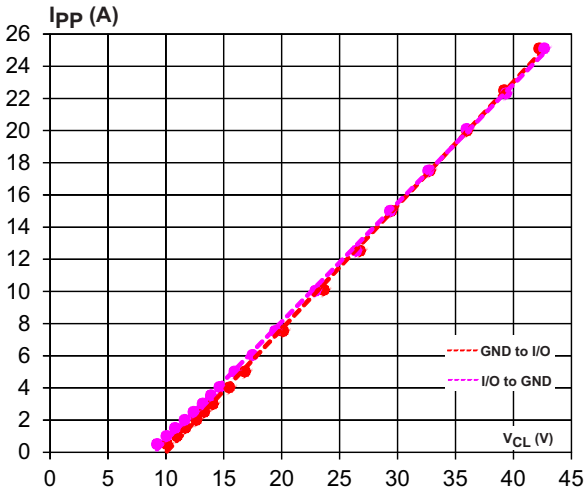


Figure 7. TLP measurement



2 Package information

- Epoxy meets UL94, V0
- Lead-free package

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com.* ECOPACK® is an ST trademark.

Figure 8. Package dimensions

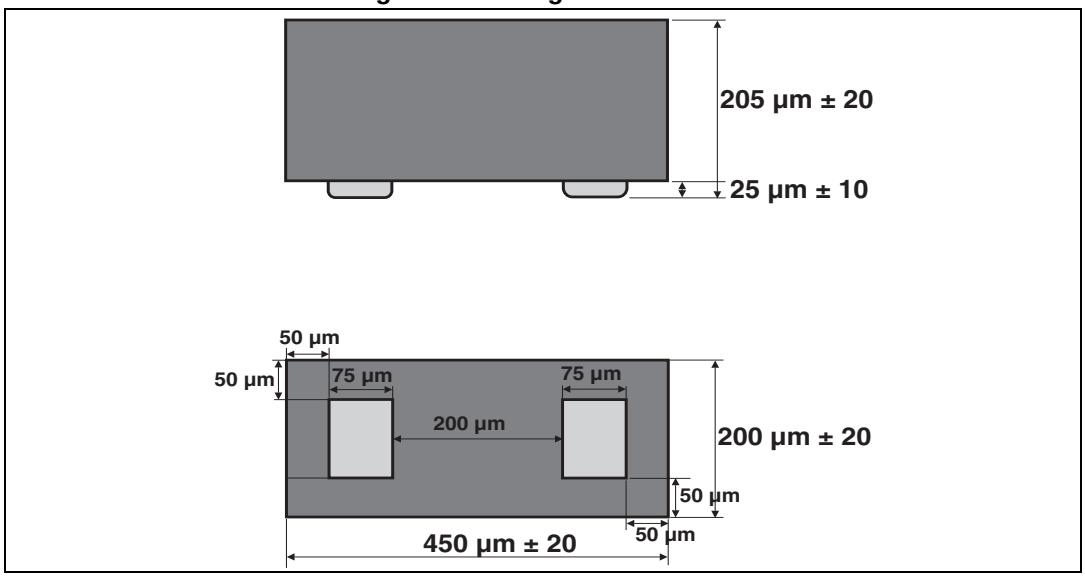


Figure 9. Footprint recommendation

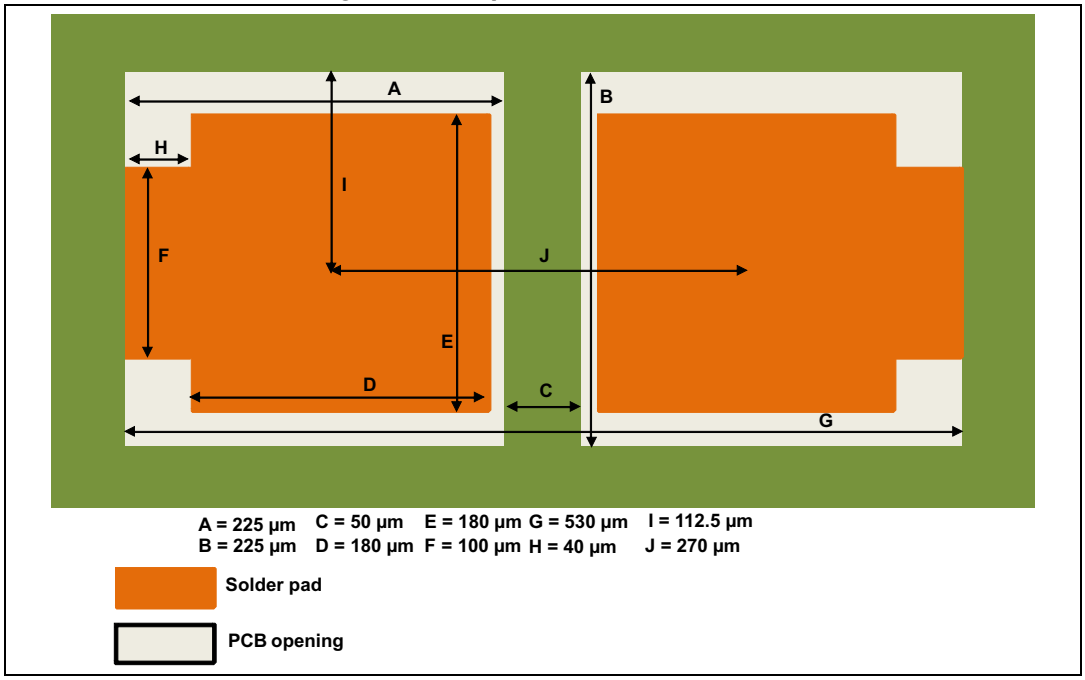
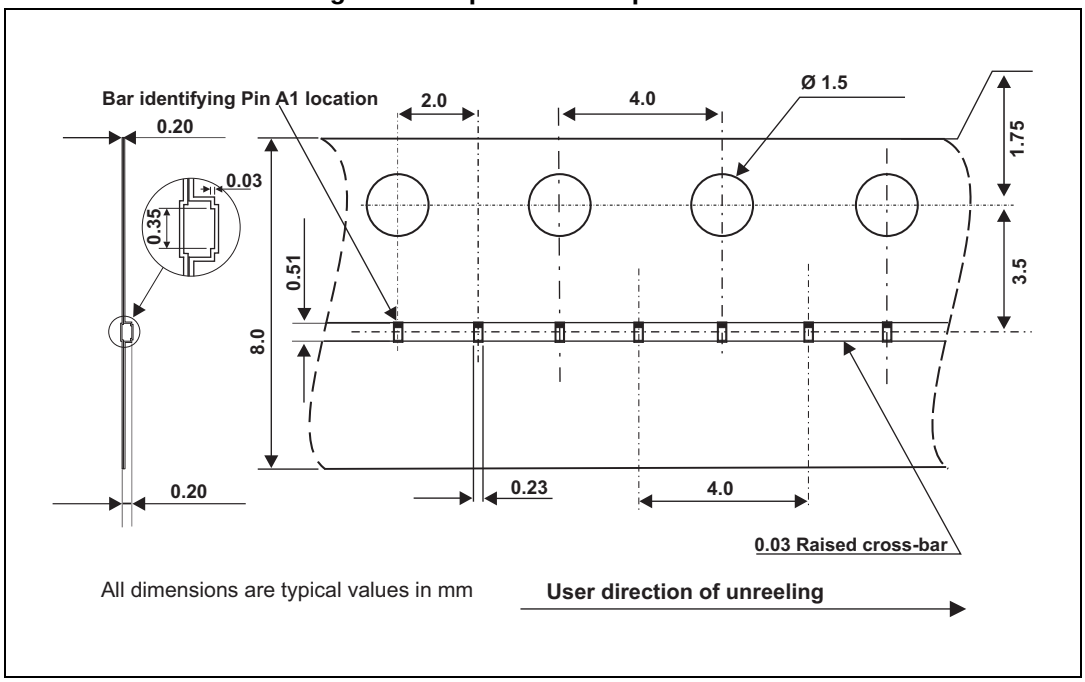


Figure 10. Tape and reel specification

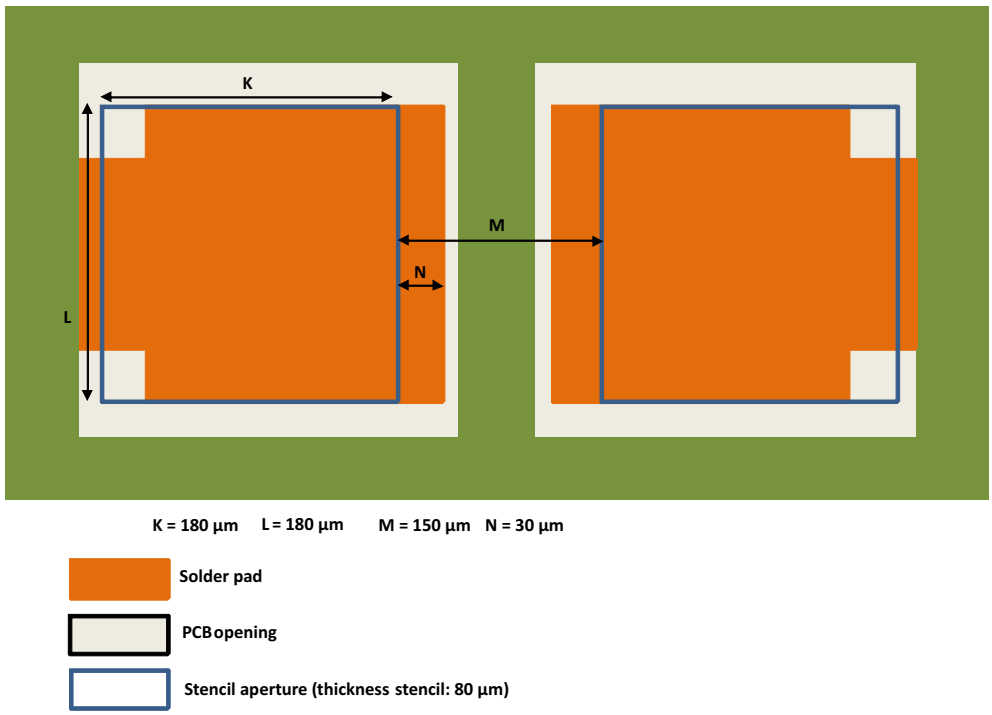


3 Recommendation on PCB assembly

3.1 Stencil opening design

Stencil opening thickness: 80 µm

Figure 11. Recommended stencil window position



3.2 Solder paste

1. Use halide-free flux, qualification ROL0 according to ANSI/J-STD-004.
2. “No clean” solder paste recommended.
3. Offers a high tack force to resist component displacement during PCB movement.
4. Solder paste with fine particles: type 4 (powder particle size 20-38 µm per IPC J STD 005).

3.3 Placement

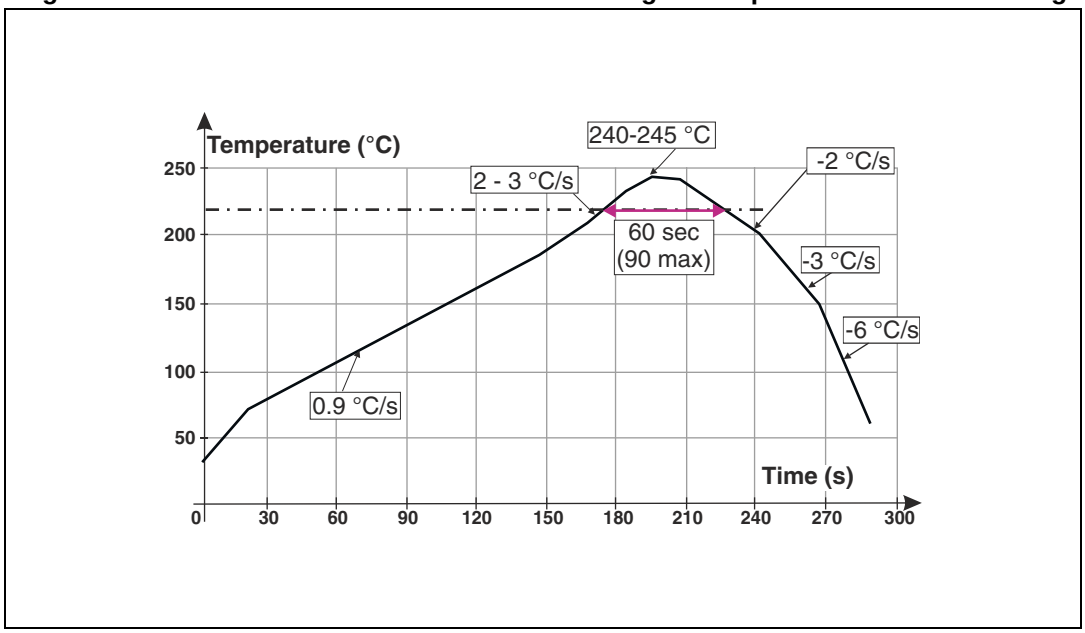
1. Manual positioning is not recommended.
2. It is recommended to use the lead recognition capabilities of the placement system, not the outline centering.
3. Tolerance of ± 0.02 mm is recommended.
4. 1.0 N placement force is recommended. Too much placement force can lead to squeezed out solder paste and cause solder joints to short. Too low placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or badly centered packages.
5. To improve the package placement accuracy, a bottom side optical control should be performed with a high resolution tool.
6. For assembly, a perfect supporting of the PCB (all the more on flexible PCB) is recommended during solder paste printing, pick and place and reflow soldering by using optimized tools.

3.4 PCB design preference

1. To control the solder paste amount, the closed via is recommended instead of open vias.
2. The position of tracks and open vias in the solder area should be well balanced. The symmetrical layout is recommended, in case any tilt phenomena caused by asymmetrical solder paste amount due to the solder flow away.

3.5 Reflow profile

Figure 12. ST ECOPACK® recommended soldering reflow profile for PCB mounting



Note: Minimize air convection currents in the reflow oven to avoid component movement.

4 Ordering information

Figure 13. Ordering information scheme

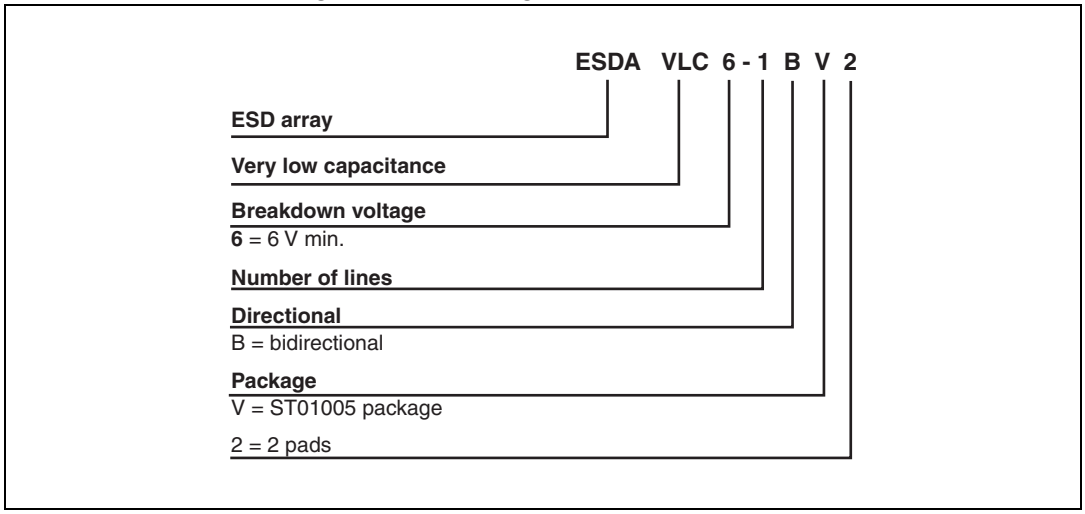


Table 3. Ordering information

Order code	Marking	Weight	Base qty	Delivery mode
ESDAVLC6-1BV2	No marking	0.041 mg	20 000	Tape and reel

5 Revision history

Table 4. Document revision history

Date	Revision	Changes
06-Nov-2012	1	First issue
20-Mar-2014	2	Updated *Figure 9*, and *Figure 11*. Updated values for dynamic resistance in *Table 2* and added *Figure 7* and *Figure 10*.

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