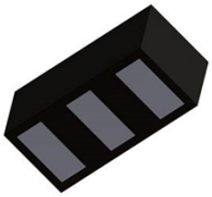
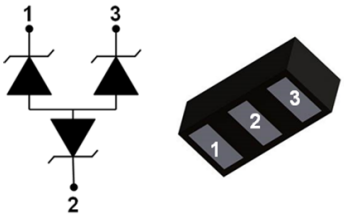
ESDX051-2BU3

Datasheet

2 lines ESD protection in bidirectional for high-speed differential interfaces



0201 package



Features

- Extra low diode capacitance: 0.13 pF
- Bidirectional device, 2 lines in 0201
- Low leakage current
- 0201 package
- ECOPACK2 compliant component
- Complies with IEC 61000-4-2 level 4
  - ±15 kV (air discharge)
  - ±8 kV (contact discharge)

Applications

Where transient over voltage protection in ESD sensitive equipment is required, such as:

- Smartphones, mobile phones and accessories
- Tablets and notebooks
- Portable multimedia devices and accessories
- Wearable, home automation, healthcare
- Highly integrated systems

Product status link
ESDX051-2BU3

Description

The ESDX051-2BU3 is a bidirectional single line TVS diode designed to protect the data line or other I/O ports against ESD transients.

The device is ideal for applications where reduced line capacitance and board space saving are required.

1 Characteristics

Table 1. Absolute maximum ratings (T_{amb} = 25 °C)

Symbol	Parameter		Value	Unit
V_{PP}	Peak pulse voltage	IEC 61000-4-2 contact discharge IEC 61000-4-2 air discharge	8 15	kV
P_{PP}	Peak pulse power dissipation (8/20 µs)		15	W
I_{PP}	Peak pulse current (8/20 µs)		1	A
T_j	Operating junction temperature range		-55 to +150	°C
T_{stg}	Storage temperature range		-65 to +150	°C
T_L	Maximum lead temperature for soldering during 10 s		260	°C

Figure 1. Electrical characteristics (definitions)

Symbol		Parameter
V_{BR}	=	Breakdown voltage
I_R	=	Breakdown current
V_{RM}	=	Stand-off voltage
I_{RM}	=	Leakage current at V_{RM}
V_{CL}	=	Clamping voltage
I_{PP}	=	Peak pulse current
R_D	=	Dynamic resistance
C_{LINE}	=	Input capacitance per line

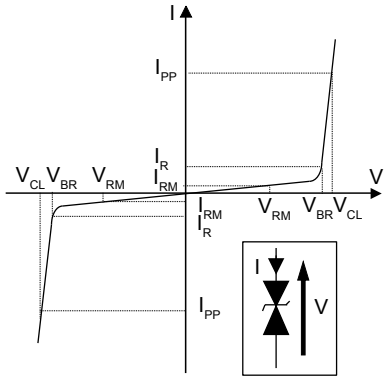


Table 2. Electrical characteristics (T_{amb} = 25 °C)

Symbol	Test condition	Min.	Typ.	Max.	Unit
V_{BR}	I_R = 1mA	6.0	6.8	10	V
V_{RM}				5	V
I_{RM}	V_{RM} = 5 V			100	nA
V_{CL}	8 kV contact discharge after 30 ns, IEC 61000-4-2, pin 1 to pin2, pin 3 to pin 2		34		V
	8/20 µs waveform, I_{PP} = 1 A		13	15	V
R_D	Pulse duration 100 ns		1.5		Ω
F_C	Cut-off frequency at -3 dB		> 40		GHz
C_{LINE}	F = 3 GHz, V_{LINE} = 0 V		0.13	0.19	pF
I_L	Insertion loss at F = 10 GHz		0.24		dB

1.1 Characteristics (curves)

Figure 2. Leakage current versus junction temperature (typical values)

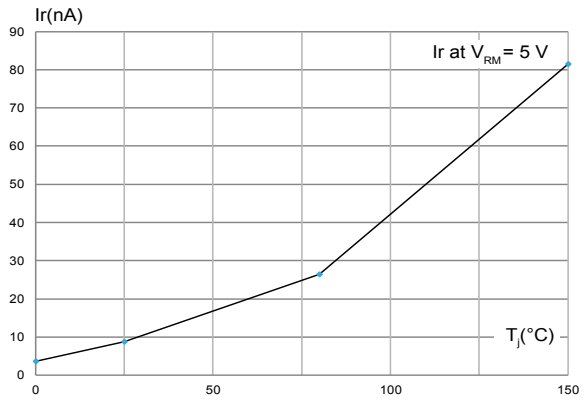


Figure 3. Junction capacitance versus applied voltage (typical values)

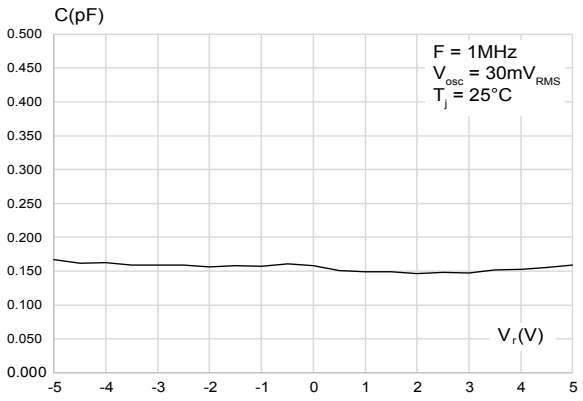


Figure 4. S21 attenuation measurement result

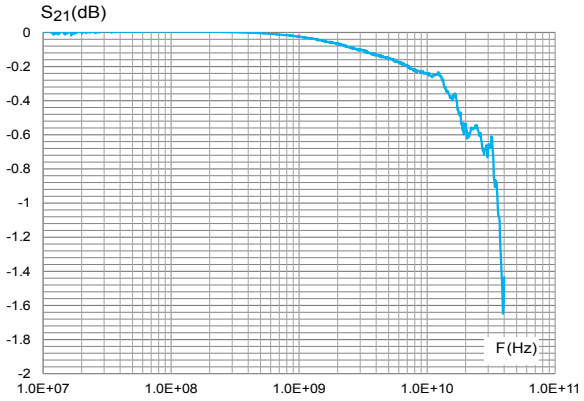


Figure 5. Junction capacitance versus applied frequency (typical values)

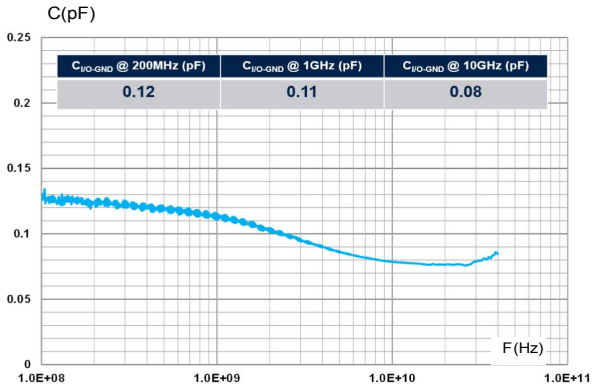


Figure 6. ESD response to IEC 61000-4-2 (+8 kV contact discharge)

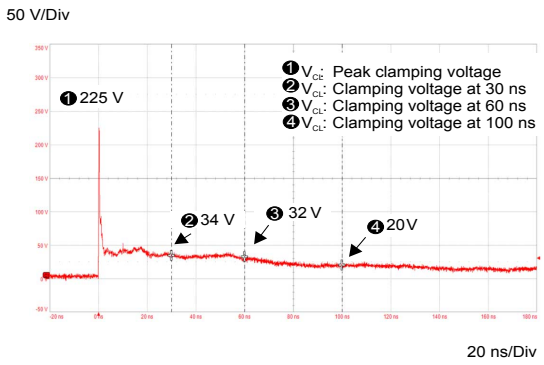


Figure 7. ESD response to IEC 61000-4-2 (-8 kV contact discharge)

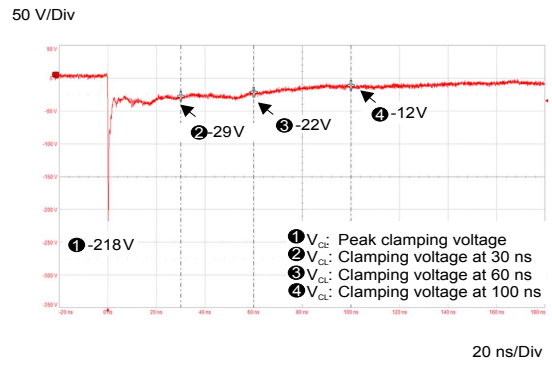


Figure 8. Positive TLP characteristic

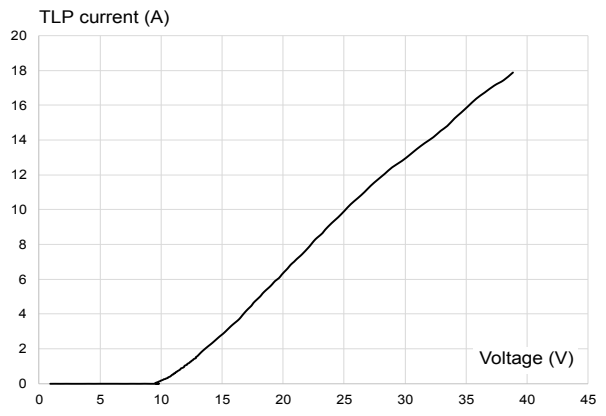
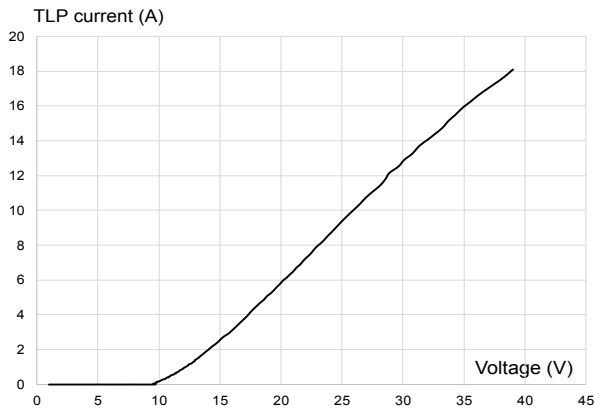


Figure 9. Negative TLP characteristic



2 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

2.1 ST0201 package information

Figure 10. 0201 package outline

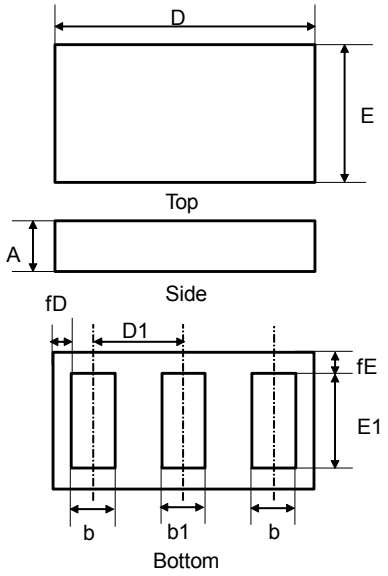


Table 3. 0201 package mechanical data

Ref.	Dimensions		
	Millimeters		
	Min.	Typ.	Max.
A	0.170	0.200	0.230
b	0.070	0.090	0.110
b1	0.080	0.100	0.120
D	0.600	0.620	0.640
D1		0.235	
E	0.300	0.320	0.340
E1	0.240	0.260	0.280
fD		0.030	
fE		0.030	

Figure 11. Tape and reel specification (in mm)

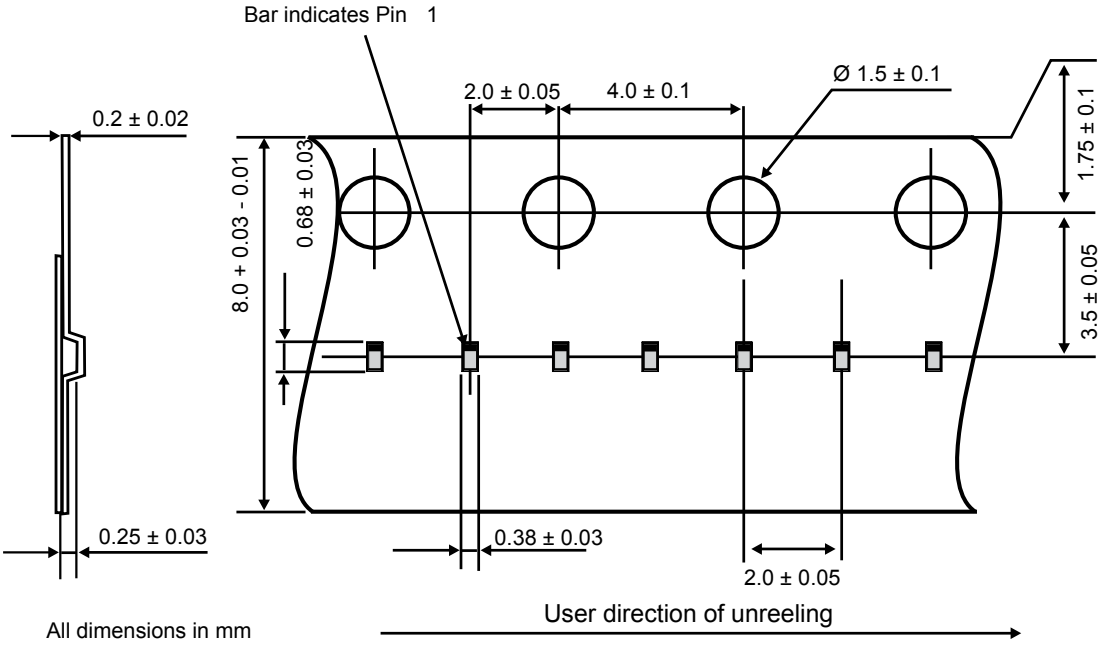
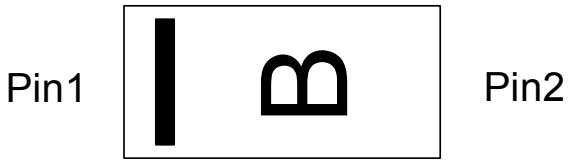


Figure 12. Marking



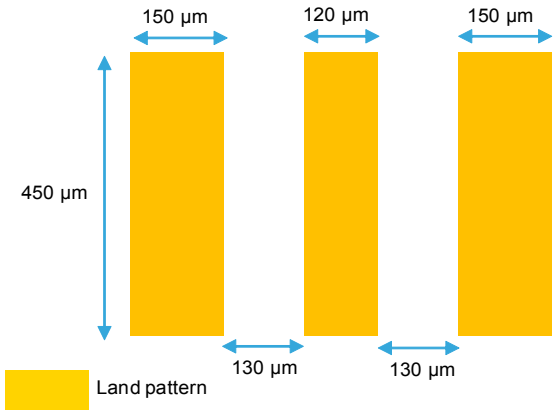
Note: The marking codes can be rotated by 90° or 180° to differentiate assembly location. In no case should this product marking be used to orient the component for its placement on a PCB. Only pin 1 mark is to be used for this purpose.

3 Recommendation on PCB assembly

3.1 Footprint

SMD footprint design is recommended.

Figure 13. Footprint in mm

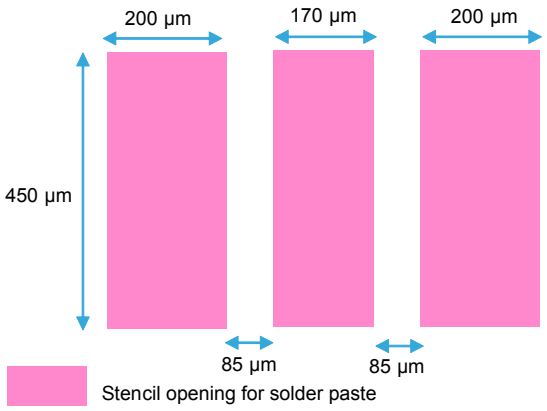


3.2 Stencil opening design

Recommended design reference:

1. Stencil opening thickness: 75 µm / 3 mils
2. Stencil aperture ratio : 100 %

Figure 14. Recommended stencil window position in mm



3.3 Solder paste

1. Halide-free flux qualification ROL0 according to ANSI/J-STD-004.
2. “No clean” solder paste is recommended.
3. Offers a high tack force to resist component movement during high speed.
4. Use solder paste with fine particles: powder particle size 20-38 µm.

3.4 Placement

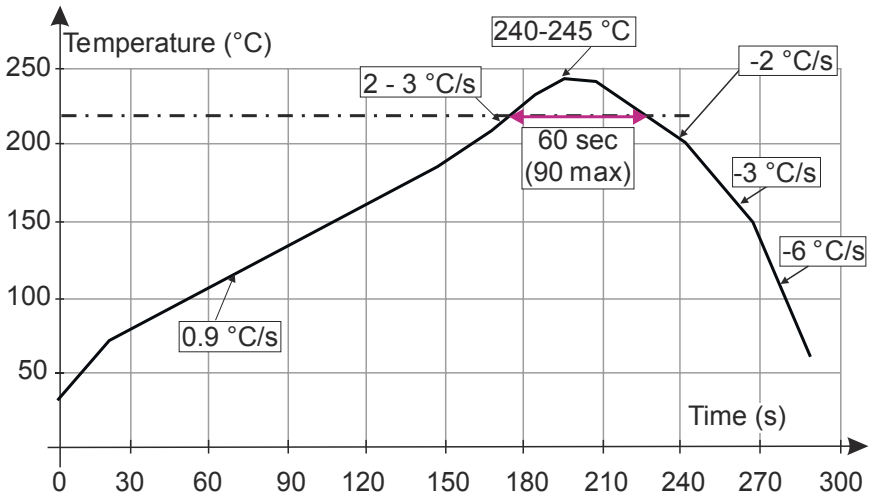
1. Manual positioning is not recommended.
2. It is recommended to use the lead recognition capabilities of the placement system, not the outline centering
3. Standard tolerance of ±0.05 mm is recommended.
4. 1.0 N placement force is recommended. Too much placement force can lead to squeezed out solder paste and cause solder joints to short. Too low placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or badly centered packages.
5. To improve the package placement accuracy, a bottom side optical control should be performed with a high resolution tool.
6. For assembly, a perfect supporting of the PCB (all the more on flexible PCB) is recommended during solder paste printing, pick and place and reflow soldering by using optimized tools.

3.5 PCB design preference

1. To control the solder paste amount, the closed via is recommended instead of open vias.
2. The position of tracks and open vias in the solder area should be well balanced. A symmetrical layout is recommended, to avoid any tilt phenomena caused by asymmetrical solder paste due to solder flow away.

3.6 Reflow profile

Figure 15. ST ECOPACK recommended soldering reflow profile for PCB mounting



Note: Minimize air convection currents in the reflow oven to avoid component movement. Maximum soldering profile corresponds to the latest IPC/JEDEC J-STD-020.

4 Ordering information

Figure 16. **Ordering information scheme**

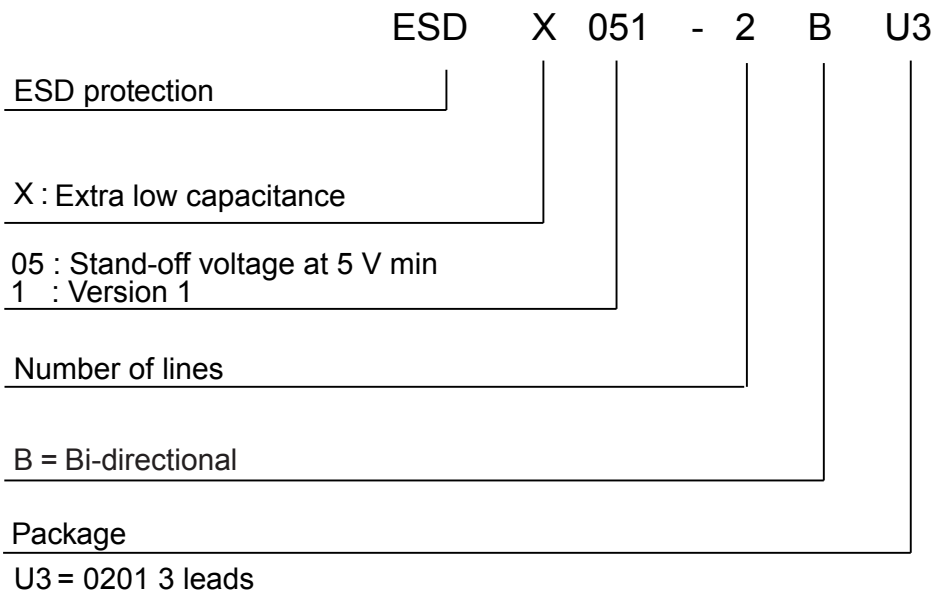


Table 4. **Ordering information**

Order code	Marking	Package	Weight	Base qty.	Delivery mode
ESDX051-2BU3	B	0201	0.086 mg	15000	Tape and reel

Revision history

Table 5. **Document revision history**

Date	Revision	Changes
08-Dec-2020	1	First issue.

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