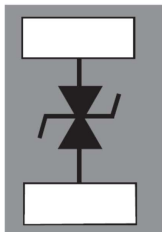


20 V low clamping, low capacitance single line bidirectional ESD protection



0201 package



Product status link

[ESDZV201-1BF4](#)

Features

- Low clamping voltage: 31 V at 16 A I_{PP} TLP
- Bidirectional device
- Stand-off voltage: 20 V
- 0201 thin package PCB area: 0.18 mm²
- Complies with the following standards: IEC 61000-4-2 level 4
 - ±15 kV (air discharge)
 - ±8 kV (contact discharge)
- **ECOPACK2** compliant component

Application

Where transient over voltage protection in ESD sensitive equipment is required, such as:

- Smartphones, mobile phones and accessories
- Tablet and notebooks
- Portable multimedia devices and accessories
- Wearable, home automation, healthcare
- Highly integrated systems

Description

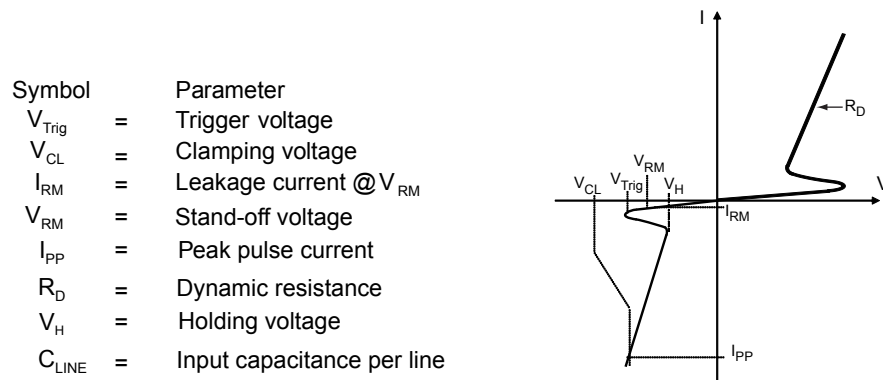
The **ESDZV201-1BF4** is a bidirectional single line TVS diode designed to protect the data line or other I/O ports against ESD transients.

The device is ideal for applications where both reduced line capacitance and board space saving are required.

1 Characteristics

Table 1. Absolute maximum ratings ($T_{amb} = 25\text{ }^{\circ}\text{C}$)

Symbol	Parameter		Value	Unit
V_{pp}	Peak pulse voltage	IEC 61000-4-2 contact discharge	± 8	kV
		IEC 61000-4-2 air discharge	± 15	
P_{pp}	Peak pulse power (8/20 μs)		140	W
I_{pp}	Peak pulse current (8/20 μs)		4.5	A
T_j	Operating junction temperature range		-55 to +150	$^{\circ}\text{C}$
T_{stg}	Storage junction temperature range		-65 to +150	
T_L	Maximum lead temperature for soldering during 10 s		260	

Figure 1. Electrical characteristics (definitions)

Table 2. Electrical characteristics (values) ($T_{amb} = 25\text{ }^{\circ}\text{C}$)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{trig}		Higher voltage than V_{TRIG} guarantees the protection turn-on	23		30	V
V_H		Lower voltage than V_H guarantees the protection turn-off	20			V
I_{RM}	Leakage current	$V_{RM} = 20\text{ V}$			0.3	μA
I_R	$V = 18\text{ V}$				100	nA
V_{CL}	Clamping voltage	IEC 61000-4-2, 8 kV contact discharge measured after 30 ns		30		V
V_{CL}	8/20 μs waveform, $I_{PP} = 1\text{ A}$			22	10	V
V_{CL}	8/20 μs waveform, $I_{PP} = 4.5\text{ A}$			29	31	V
R_D	Dynamic resistance, pulse duration 100 ns - I_{PP} [1 A – 16 A]			0.7		Ω
C_{LINE}	Line capacitance	$V_{LINE} = 0\text{ V}$, $F = 1\text{ MHz}$, $V_{OSC} = 30\text{ mV}$		3	5	pF

1.1 Characteristics (curves)

Figure 2. Leakage current versus junction temperature at V_{RM} 20 V (typical value)

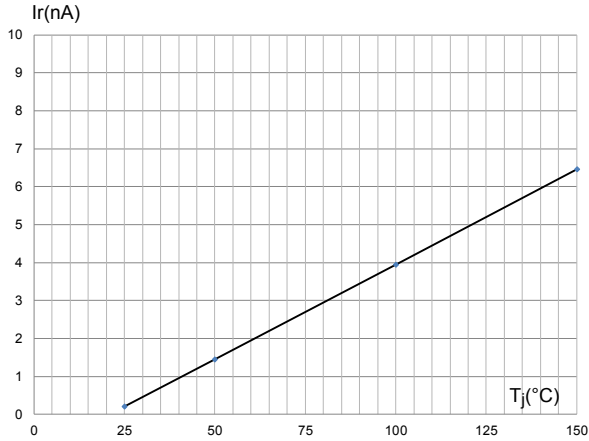


Figure 3. Junction capacitance versus applied voltage (typical values)

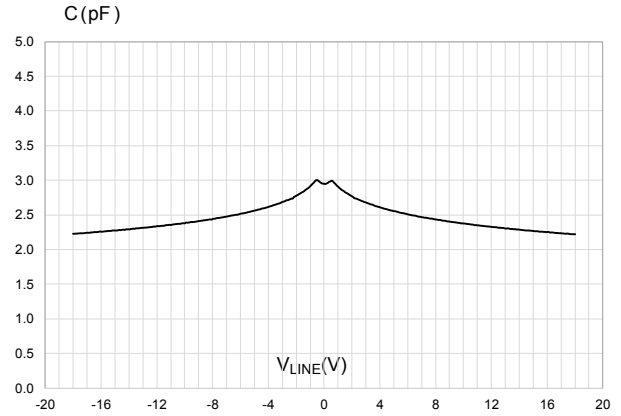


Figure 4. S21 attenuation

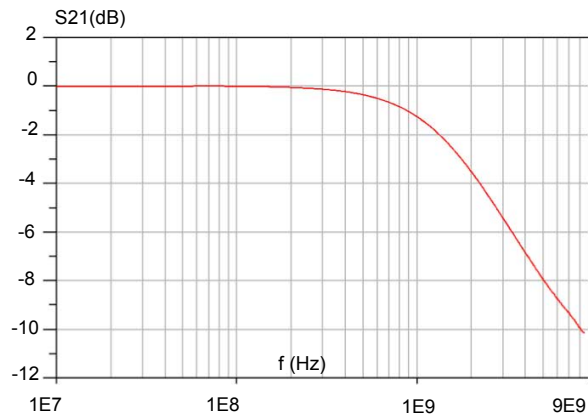


Figure 5. ESD response to IEC 61000-4-2 (+8 kV contact discharge)

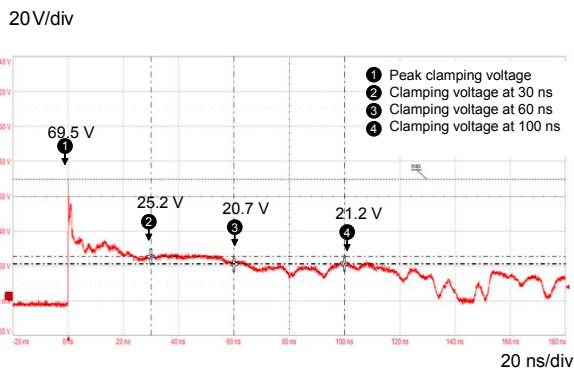


Figure 6. ESD response to IEC 61000-4-2 (-8 kV contact discharge)

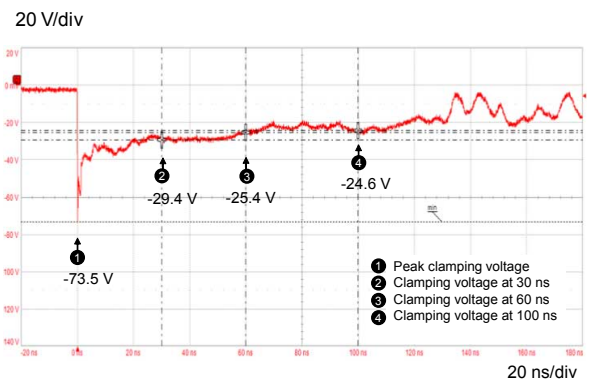


Figure 7. Positive TLP characteristic

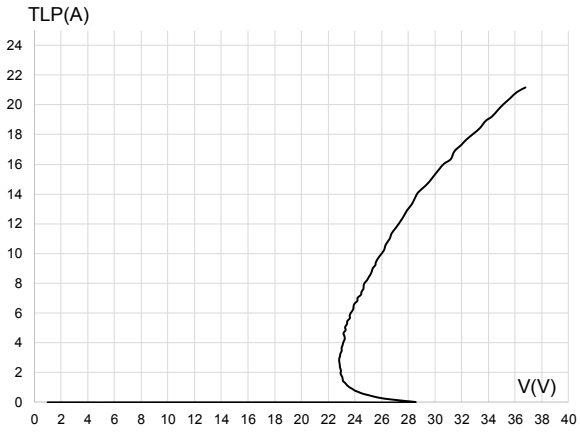
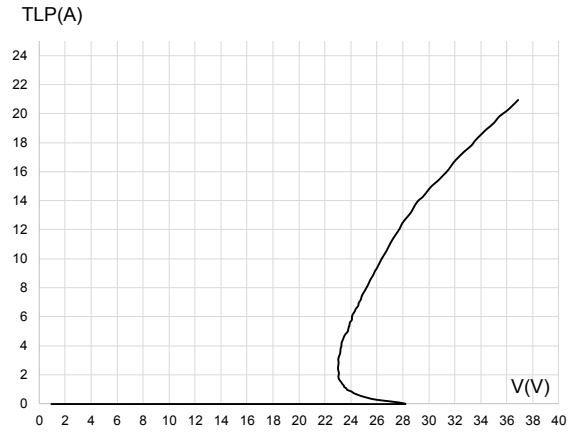


Figure 8. Negative TLP characteristic

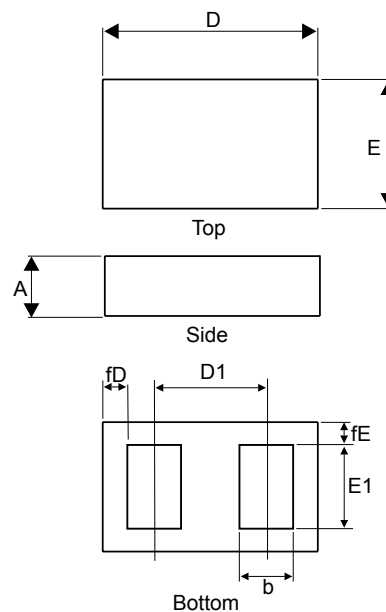


2 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

2.1 0201 package information

Figure 9. 0201 package outline



Note: The marking codes can be rotated by 90° or 180° to differentiate assembly location. In no case should this product marking be used to orient the component for its placement on a PCB. Only pin 1 mark is to be used for this purpose.

Table 3. 0201 package mechanical data

Ref.	Dimensions		
	Millimeters		
	Min.	Typ.	Max.
A	0.130	0.150	0.170
b	0.1675	0.1875	0.2075
D	0.560	0.580	0.600
D1		0.3375	
E	0.260	0.280	0.300
E1	0.205	0.225	0.245
fD	0.0175	0.0275	0.0375
fE	0.0175	0.0275	0.0375

Figure 10. Tape and reel specification

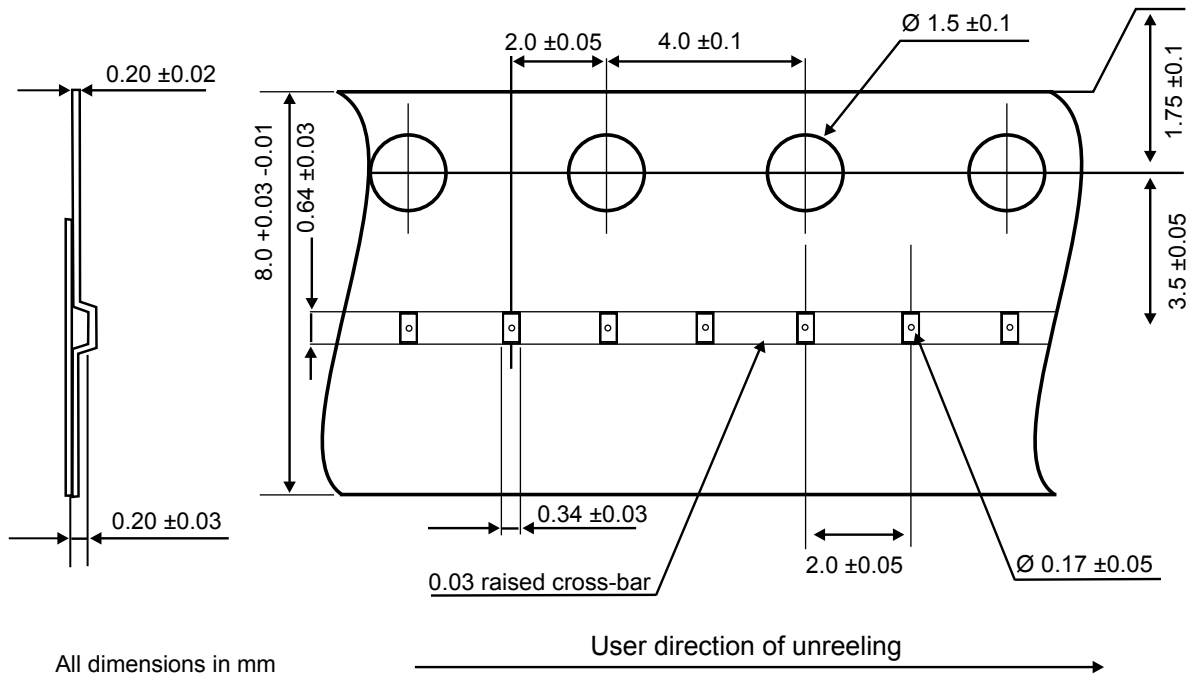
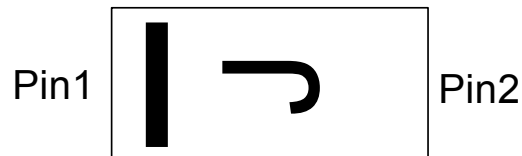


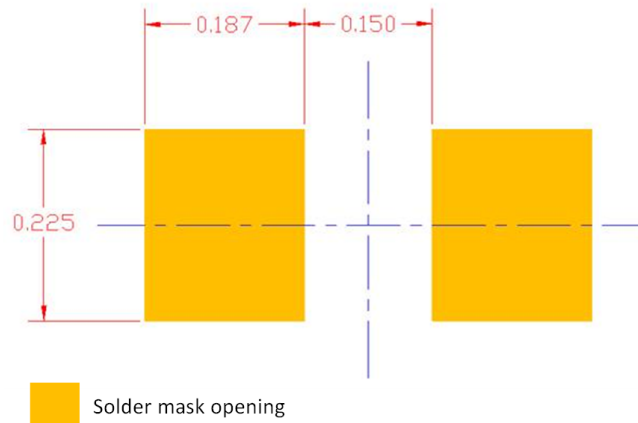
Figure 11. Marking



3 Recommendation PCB assembly

3.1 Footprint

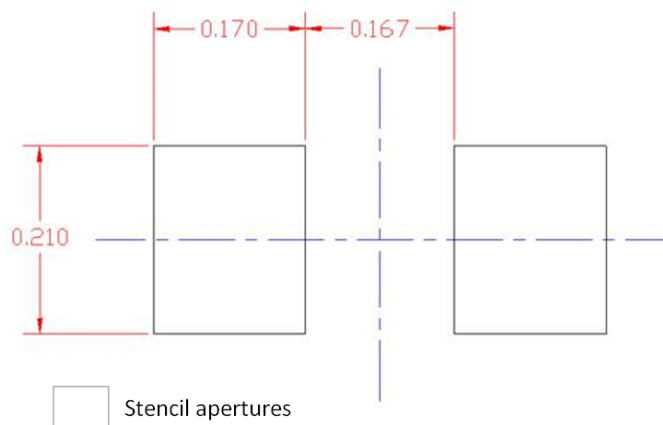
Figure 12. Footprint in mm



3.2 Stencil opening design

1. Recommended design reference
 - a. Stencil opening dimensions: 75 μm / 3 mils

Figure 13. Stencil opening recommendations



3.3 Solder paste

1. Halide-free flux qualification ROL0 according to ANSI/J-STD-004.
2. "No clean" solder paste is recommended.
3. Offers a high tack force to resist component movement during high speed.
4. Use solder paste with fine particles: powder particle size 20-38 μm .

3.4 Placement

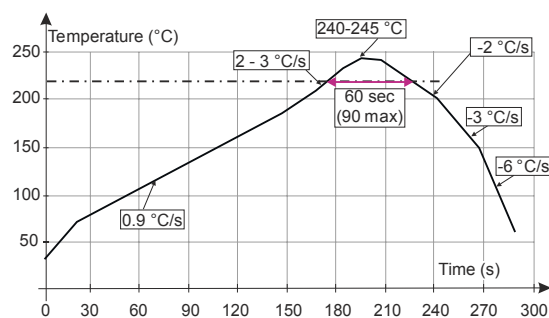
1. Manual positioning is not recommended.
2. It is recommended to use the lead recognition capabilities of the placement system, not the outline centering
3. Standard tolerance of ± 0.05 mm is recommended.
4. 1.0 N placement force is recommended. Too much placement force can lead to squeezed out solder paste and cause solder joints to short. Too low placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or badly centered packages.
5. To improve the package placement accuracy, a bottom side optical control should be performed with a high resolution tool.
6. For assembly, a perfect supporting of the PCB (all the more on flexible PCB) is recommended during solder paste printing, pick and place and reflow soldering by using optimized tools.

3.5 PCB design preference

1. To control the solder paste amount, the closed via is recommended instead of open vias.
2. The position of tracks and open vias in the solder area should be well balanced. A symmetrical layout is recommended, to avoid any tilt phenomena caused by asymmetrical solder paste due to solder flow away.

3.6 Reflow profile

Figure 14. ST ECOPACK® recommended soldering reflow profile for PCB mounting



Note: Minimize air convection currents in the reflow oven to avoid component movement. Maximum soldering profile corresponds to the latest IPC/JEDEC J-STD-020.

4 Ordering information

Figure 15. Ordering information scheme

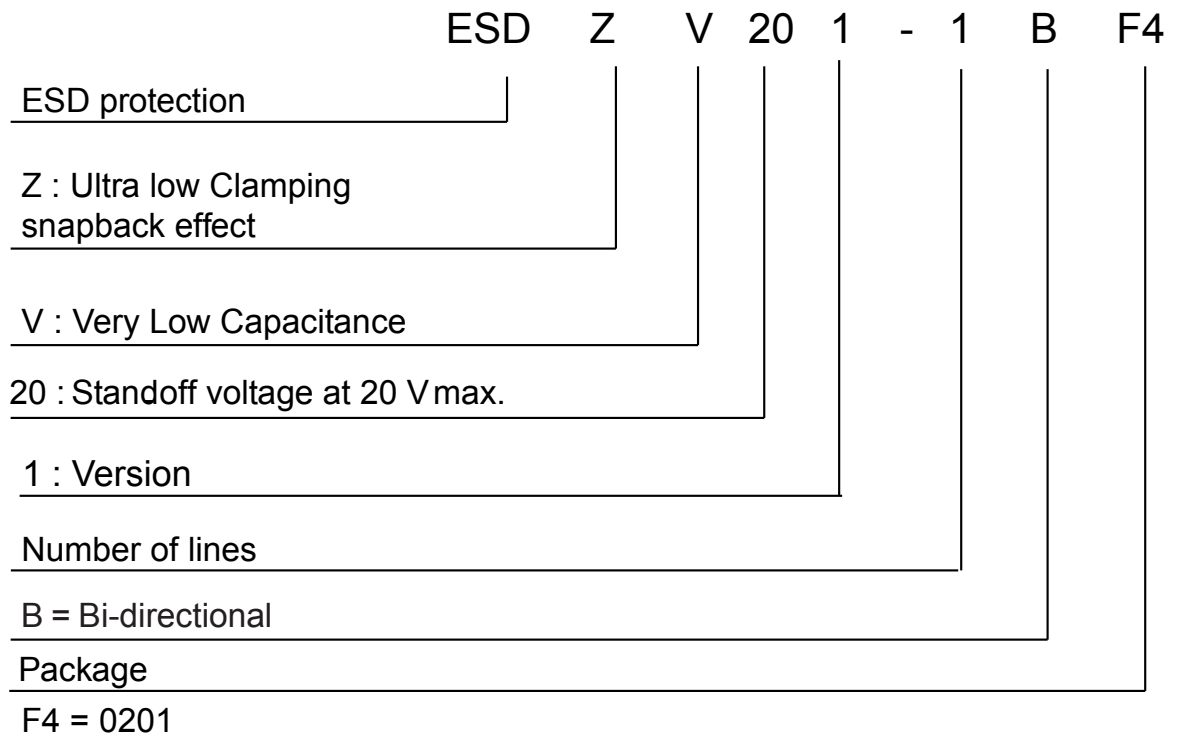


Table 4. Ordering information

Order code	Marking	Package	Weight	Base qty.	Delivery mode
ESDZV201-1BF4	J	0201	0.072 mg	15000	Tape and reel

1. The marking codes can be rotated by 90° or 180° to differentiate assembly location.

Revision history

Table 5. Document revision history

Date	Revision	Changes
07-Jan-2020	1	Initial release.

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