



Dual full bridge with integrated PWM current controllers

Data brief



Description

The EVAL6207Q is a dual full bridge driver board allowing the user to test the L6207Q functions.

The dual full bridges integrated into the L6207Q can be used to drive a single two phase stepper motor or up to four DC motors (unidirectional). The device also includes two independent constant OFF time PWM current controllers.

The board can be driven using the STEVAL-PCC009V2 communication board and the PractiSPINTM 2 evaluation software.

Features

- Voltage range from 8 V to 52 V
- Phase current up to 2.5 A_{r m s}
- Adjustable constant t_{OFF} PWM current control
- Logic inputs 5 V / 3.3 V compliant
- Small application footprint with high thermal performance
- Suitable to be used in combination with PractiSPINTM 2 software

Board description EVAL6207Q

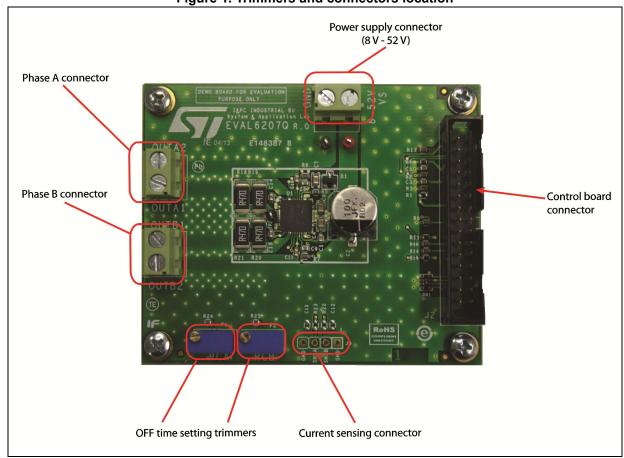
1 Board description

Table 1. Electrical specifications

Parameter	Value
Supply voltage (VS)	8 to 52 V
Maximum output current (each phase)	2.5 A _{r.m.s.}
Low level logic inputs voltage	0 V
High level logic input voltage	5 V / 3.3 V ⁽¹⁾
Maximum VREF _A /VREF _B input voltage	3.3 V ⁽²⁾
Switching frequency	Up to 100 kHz
Operating temperature	-25 to +125 °C
L6207Q thermal resistance junction-to-ambient	17° C/W

- 1. Logic inputs are 3.3 V and 5 V compliant.
- 2. Equivalent to about 3.1 A peak current.

Figure 1. Trimmers and connectors location



EVAL6207Q Board description

Table 2. Control board connector pinout (J2)

Pin	Туре	Function
2	Ground	Ground
3	Logic input	Input IN1A of L6207Q
4	Logic input	Input IN2A of L6207Q
5	Logic input	Input IN1B of L6207Q
6	Logic input	Input IN2B of L6207Q
11	Analog input	Overcurrent threshold regulation for A bridge
12	Analog input	Overcurrent threshold regulation for B bridge
13	Ground	Ground
14	Supply voltage	3.3 V supply voltage
16	Logic input	Input ENA of L6207Q
23	Ground	Ground
24	Analog output	Board identification system ID0
25	Analog output	Board identification system ID1
27	Logic output	Fault output for B bridge
28	Ground	Ground
29	Logic output	Fault output for A bridge
30	Logic input	Input ENB of L6207Q
Others	Unconnected	

Table 3. Current sensing connector (J9)

Pin	Туре	Function
1	Ground	Ground
2	Analog output	SENSEA pins of L6207Q ⁽¹⁾
3	Analog output	SENSEB pins of L6207Q ⁽¹⁾
4	Ground	Ground

R22/23 resistors and C12/13 capacitors must be added when output is used. The value of RC network should be chosen according to the target low pass frequency of the filter.

Schematic EVAL6207Q

2 Schematic

C2A OPTION PTH OPTION 220 nF/16 V 5 C6 + NC#1 NC#4 NC#5 NC#5 NC#8 NC#8 NC#8 R NZA A ENB INZB C4 100 nF /100 V C9 IN2B 5.6 nF/6.3 V C10 68 nF/6.3 V OCDB OCDA 4.3 kb 7 R16 S R14 RN1 56 kΩ 22 G Σ, Σ, Σ, NM C13 R23 M ≥ R22 NM

Figure 2. Schematic

EVAL6207Q Bill of material

3 Bill of material

Table 4. Bill of material

Index	Quantity	Reference	Value	Package
1	1	C2	100 μF/63 V	CAPES-R10H10
2	1	C2A	100 μF/63 V (option)	CAPE-R8H12-P35
3	1	C1	220 nF/16 V	CAPC-0603
4	2	C3, C5	100 nF/4 V	CAPC-0603
5	2	C4, C6	100 nF/100 V	CAPC-0805
6	1	C7	10 nF/100 V	CAPC-0805
7	2	C8, C9	5.6 nF/6.3 V	CAPC-0603
8	2	C10, C11	68 nF/6.3 V	CAPC-0603
9	2	C14, C15	820 pF/6.3 V	CAPC-0603
10	2	C12, C13	NM	CAPC-0603
11	1	D1	BAT54SFILM	SOT-23
12	3	J1, J5, J6	Screw connector 2 poles	MORSV-508-2P
13	1	J2	Pol. IDC male header vertical 30 poles	CON-FLAT-15X2-180M
14	1	J9	N.M.	STRIP254P-M-4
15	1	RN1	56 kΩ	RESN-CAY16
16	1	R1	N.M.	RESC-0603
17	1	R2	10 kΩ/1%	RESC-0603
18	1	R3	0	RESC-0603
19	1	R4	16.9 kΩ/1%	RESC-0603
20	1	R5	100	RESC-0603
21	4	R6, R7, R8, R17	100 kΩ	RESC-0603
22	2	R10, R14	4.3 kΩ	RESC-0603
23	2	R11, R16	1 kΩ	RESC-0603
24	4	R18, R19, R20, R21	0.4 Ω/1 W	RESC-2512
25	2	R22, R23	N.M.	RESC-0603
26	2	P1, P2	200 kΩ	TRIMM-100X50X110-64W
27	2	R24, R25	12 kΩ	RESC-0603
28	1	TP1	TPTH-RING-1MM RED	TPTH-RING-1MM
29	2	TP2, TP3	TPTH-RING-1MM BLACK	TPTH-RING-1MM
30	1	U1	L6207Q	QFN7X7_48L

Layout EVAL6207Q

4 Layout

Figure 3. Layout (silk screen)

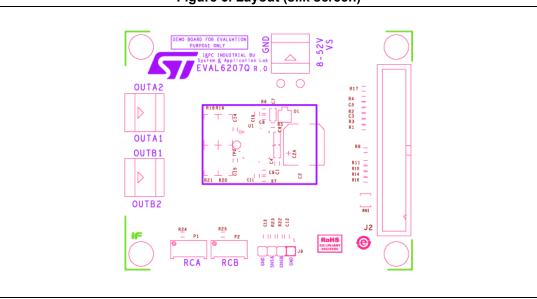
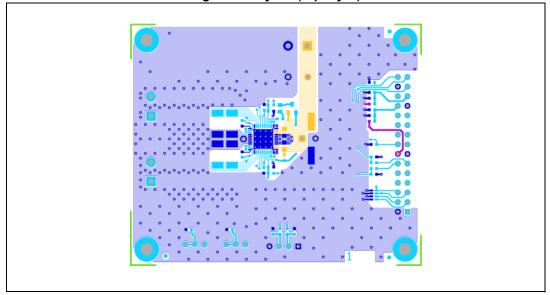


Figure 4. Layout (top layer)



EVAL6207Q Layout

Figure 5. Layout (inner layer 2)

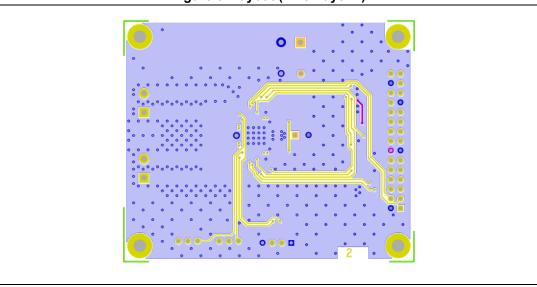
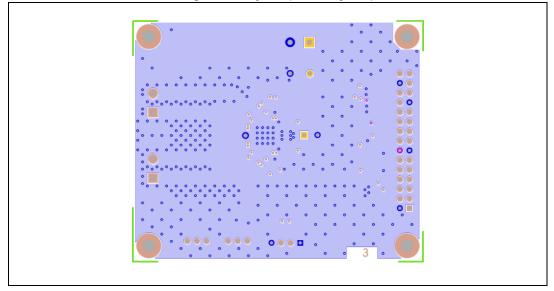


Figure 6. Layout (inner layer 3)



Layout EVAL6207Q

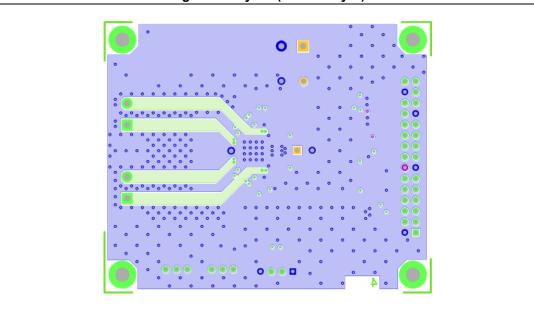


Figure 7. Layout (bottom layer)

OFF time setting EVAL6207Q

OFF time setting 5

Figure 8. OFF time vs. $\rm R_{\rm off}$ and $\rm C_{\rm off}$ 1·10³ tOFF [µs] 100 $C_{\mbox{off}}$ [nF] AM03295

Revision history 6

Table 5. Document revision history

Date	Revision	Changes
07-Aug-2013	1	Initial release.

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