EVAL6393FB

Low voltage full-bridge demonstration board based on the L6393 advanced high voltage gate driver

Data brief

Features

- ~150 W drive capability (50 V - 3.0 $A_{r.m.s.}$)
- Very low area occupation, all devices and power switches in SMD package (no heatsink)
- Fast-decay or slow-decay on-board constant off-time peak current control
- PWM voltage mode control with overcurrent protection possible via external logic signals
- Driver supply voltage on-board generation directly from BUS voltage
- Carefully optimized layout

EVAL6393FB

Description

The EVAL6393FB demonstrates how to use two L6393 drivers to drive a single-phase load through a full-bridge topology. This allows both the direction and the value of the current flowing into the load to be controlled. Typical loads, which can be effectively driven by using this topology, are single-phase BLDC motors, fans and HID lamps. Thanks to the integrated features of the L6393, the board has a very small footprint and an optimized layout, and can be simply run by applying the BUS voltage and a direction signal.

1 Board description

Table 1. EVAL6393FB electrical specifications

Parameter	Value
Supply voltage range (VS)(1) (2)	32 V to 52 V_{DC}
RMS output current rating (OUT x)	Up to 3.0 A
Driver supply voltage (V_{CC}) (3)	10 to 20 V
Logic control signals	0 to + 15 V
Operating temperature range	-40 to +125 °C

1. Minimum VS voltage restriction is due to biasing current of the Zener diode used to generate V_{cc}. This limit can be decreased by changing R29 value or by opening JP3 and providing an externally generated V_{cc} through connector J1.
2. Maximum VS voltage limit can be increased up to 580 V by replacing the power switches and bulk capacitor C15 with components with adequate voltage ratings. Resistor R29 should be removed and an externally generated V_{cc} should be provided through connector J1.
3. When externally supplied through J1 with JP3 opened, otherwise V_{cc} = 12 V.

Figure 1. Jumper and connector location

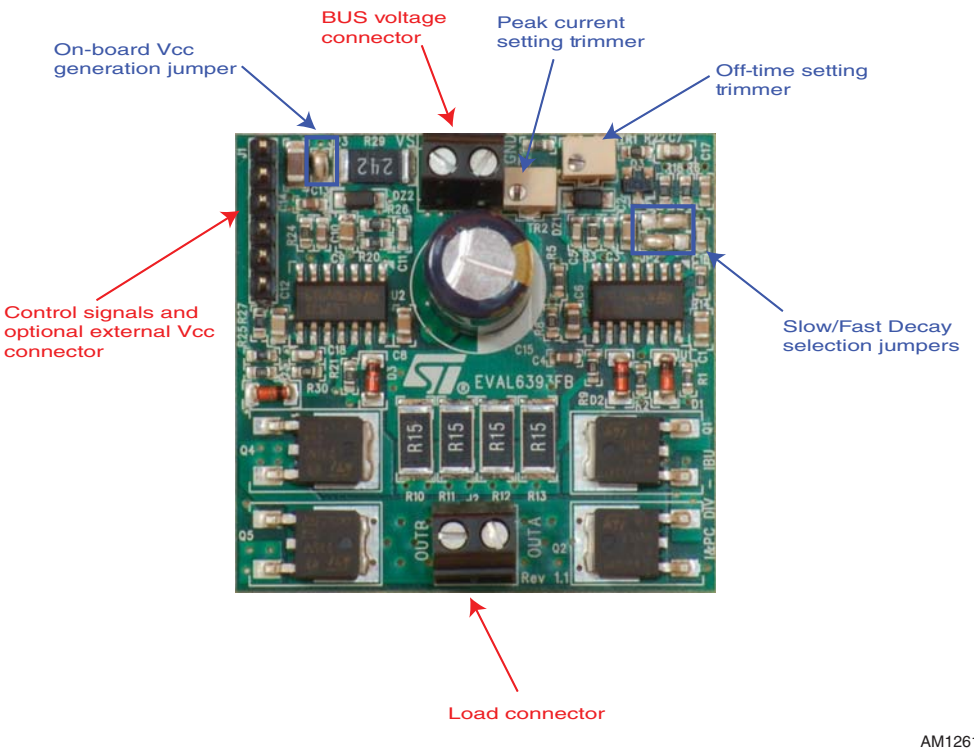


Table 2. Jumper and connector description

Name	Type	Function
J1	Control signal connector	Optional control signal and external V_{CC} connector
J2	Power output	Load connector
J3	Power supply	BUS power supply connector
JP1	Configuration jumper	To pull-up SD and/or BRAKE signal to V_{CC} /3
JP2	Configuration jumper	To pull-up SD and/or BRAKE signal to CPOUT
JP3	Configuration jumper	To connect the on-board generated V_{CC} to the supply pins of the drivers

Table 3. Control signal connector pinout (J1)

Pin	Type	Description
1	Power supply	Driver power supply V_{CC}, open JP3 to provide externally generated V_{CC}
2	Power supply	GND
3	Digital input	Driver SD signal
4	Digital input	Driver BRAKE signal
5	Analog PWM input	V_{ctrl} signal; used to change current limit threshold
6	Digital input	DIR signal; sets current direction

Table 4. Current peak detection settings

Pin	Type	Description
TR1	Variable resistor	Used to adjust constant off-time duration after overcurrent detection
TR2	Variable resistor	Used to adjust overcurrent detection threshold I_{pk} I_{pk} = V(CP-)/[R10//R11//R12//R13]

Table 5. Control scheme configuration

Description	Jumper configuration
Constant off-time peak current control with slow-decay	JP1 closed on !SD and JP2 closed on !BRAKE
Constant off-time peak current control with fast-decay	JP1 closed on !SD and JP2 closed on !SD
PWM voltage control with slow-decay overcurrent protection	JP1 open, JP2 closed on !BRAKE and !SD externally provided through J1
PWM voltage control with fast-decay overcurrent protection	JP1 open, JP2 closed on !SD and !BRAKE externally provided through J1

Figure 2. EVAL6393FB schematic

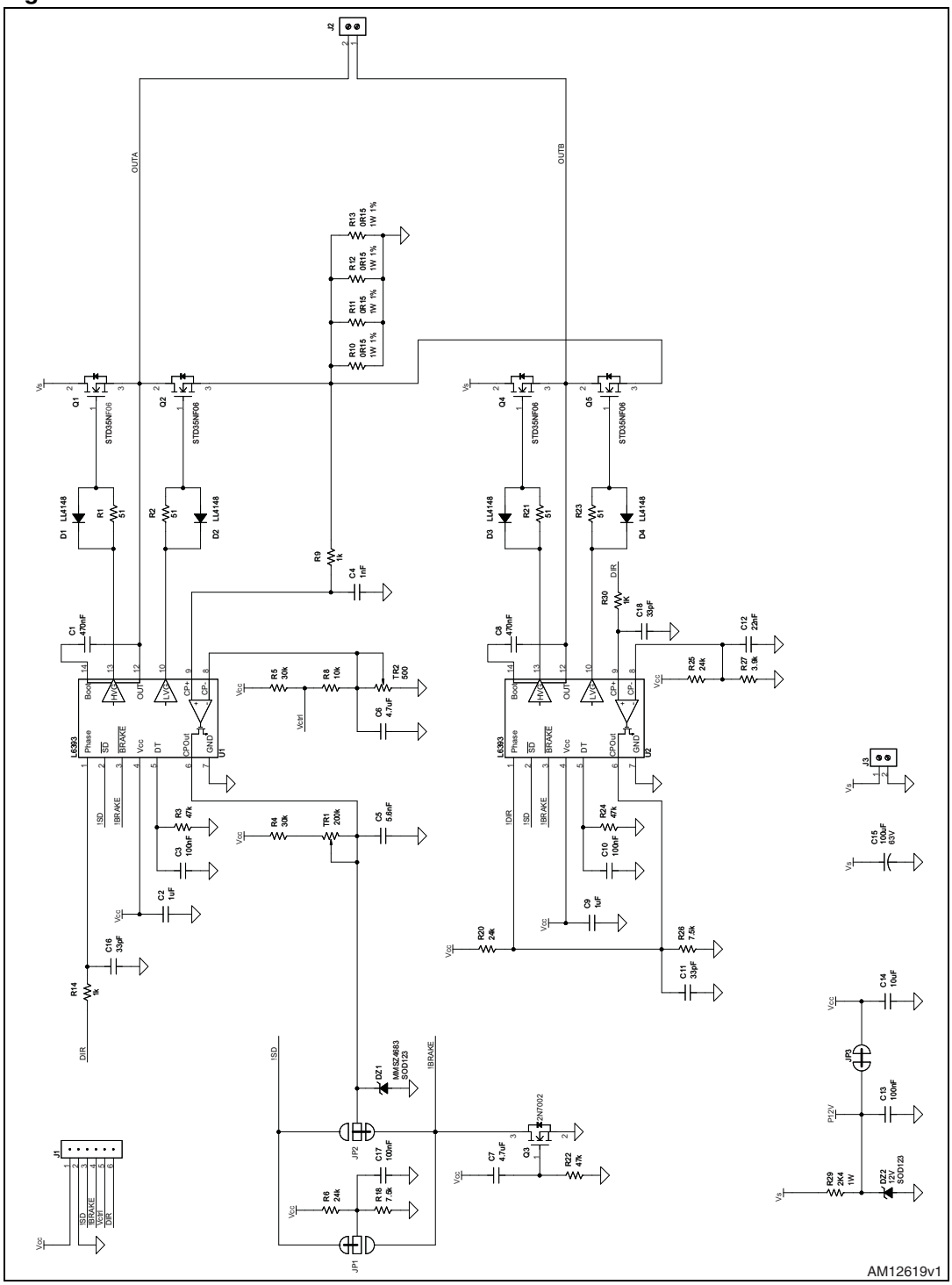


Table 6. EVAL6393FB bill of material

Reference	Value	Description
C1, C8	470 nF, 25 V	SMT ceramic capacitor, 0805
C2, C9	1 µF, 25 V	SMT ceramic capacitor, 0805
C3, C10, C13, C17	100 nF, 25 V	SMT ceramic capacitor, 0603
C4	1 nF, 25 V	SMT ceramic capacitor, 0603
C5	5.6 nF, 25 V	SMT ceramic capacitor, 0603
C6, C7	4.7 µF	SMT ceramic capacitor, 0805
C11, C16, C18	33 pF, 25 V	SMT ceramic capacitor, 0603
C12	22 nF, 25 V	SMT ceramic capacitor, 0805
C14	10 µF, 25 V	SMT ceramic capacitor, 1206
C15	100 µF, 63 V	Radial lead electrolytic capacitor (D 10 mm, H 12.5 mm)
D1, D2, D3, D4	LL4148	Fast switching diode, SOD80
DZ1	MMSZ4683	3 V Zener diode, SOD123
DZ2		12 V Zener diode, SOD123
J1		1x6 strip, 2.54 mm pitch
J2, J3		1x2 screw PCB terminal block, 5.08 mm pitch
JP1, JP2		2- way solder jumper
JP3		Solder jumper
Q1, Q2, Q4, Q5	STD35NF06	60 V, 35 A N-channel power MOSFET in DPAK
Q3	2N7002	60 V, 0.2 A N-channel power MOSFET in SOT23
R1, R2, R21, R23	51 Ω	SMT resistor, 0603
R3, R22, R24	47 kΩ	SMT resistor, 0603
R4, R5	30 kΩ	SMT resistor, 0603
R6, R20, R25	24 kΩ	SMT resistor, 0603
R8	10 kΩ	SMT resistor, 0603
R9, R14, R30	1 kΩ	SMT resistor, 0603
R10, R11, R12, R13		1% 1 W SMT resistor, 2512
R18, R26	7.5 kΩ	SMT resistor, 0603
R27	3.9 kΩ	SMT resistor, 0603
R29	Ω	5% 1W SMT resistor, 2512
TR1	200 kΩ	SMT trimmer
TR2	500 Ω	SMT trimmer
U1, U2	L6393D	Half-bridge gate driver, in SO14

Figure 3. EVAL6393FB – layout (top layer)

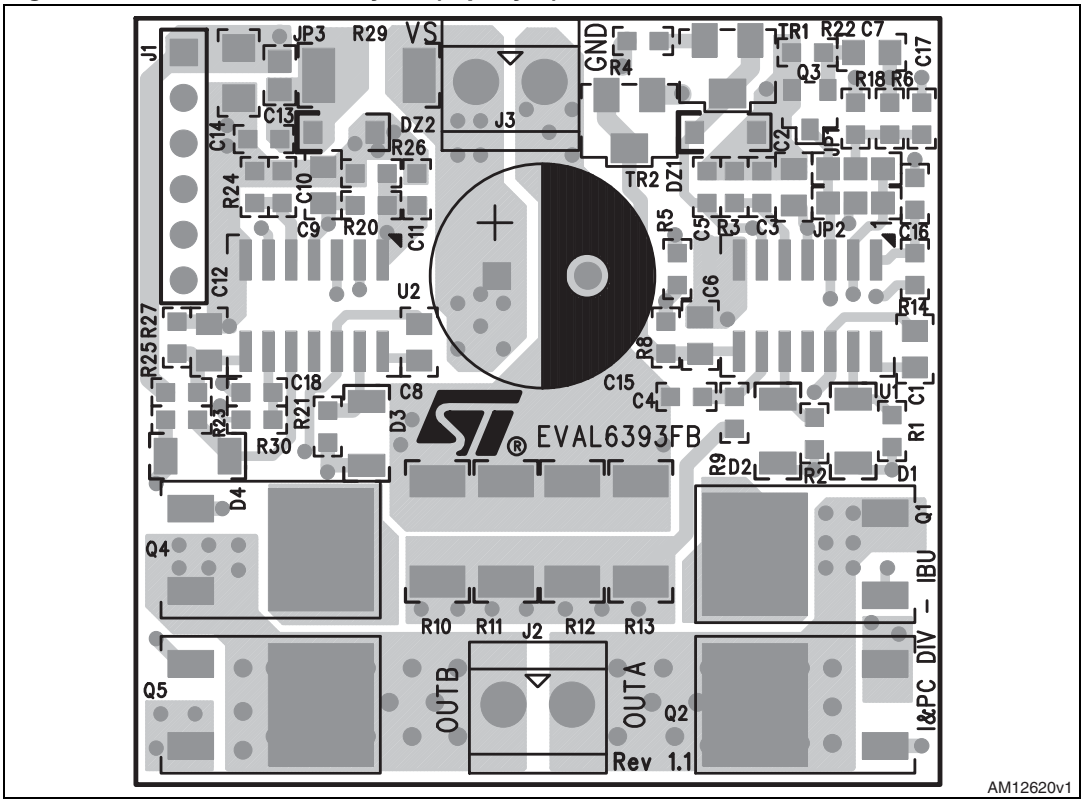


Figure 4. EVAL6393FB – layout (bottom layer)

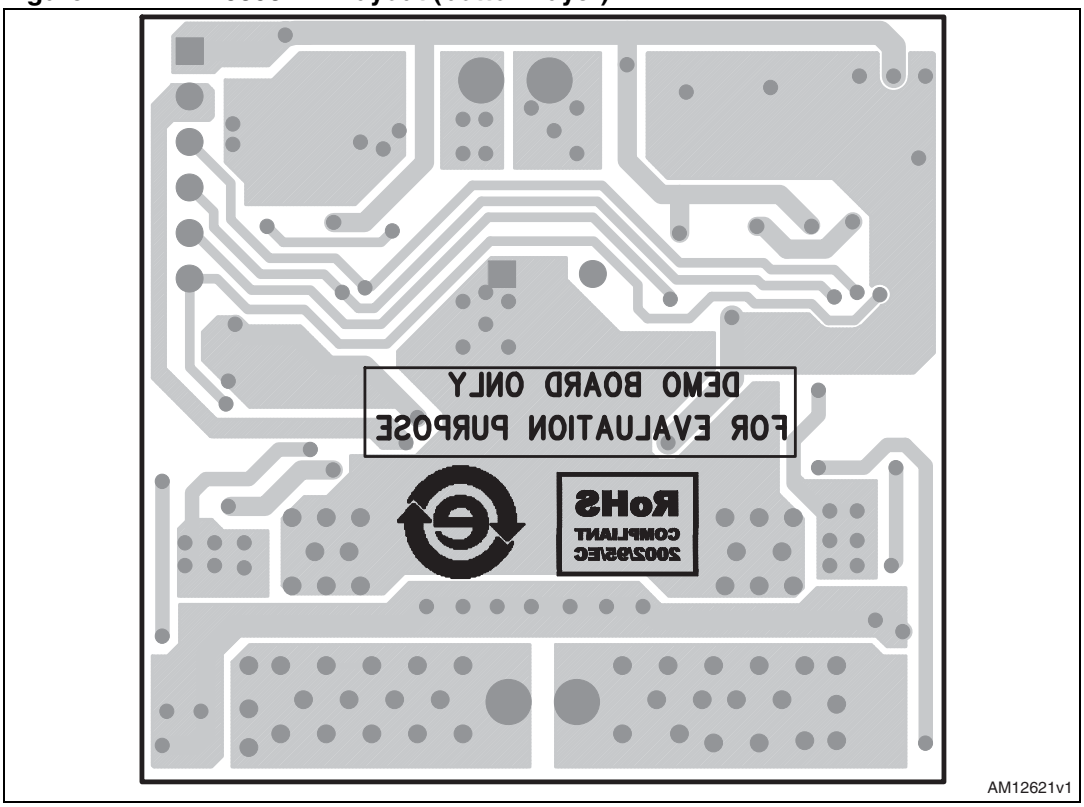
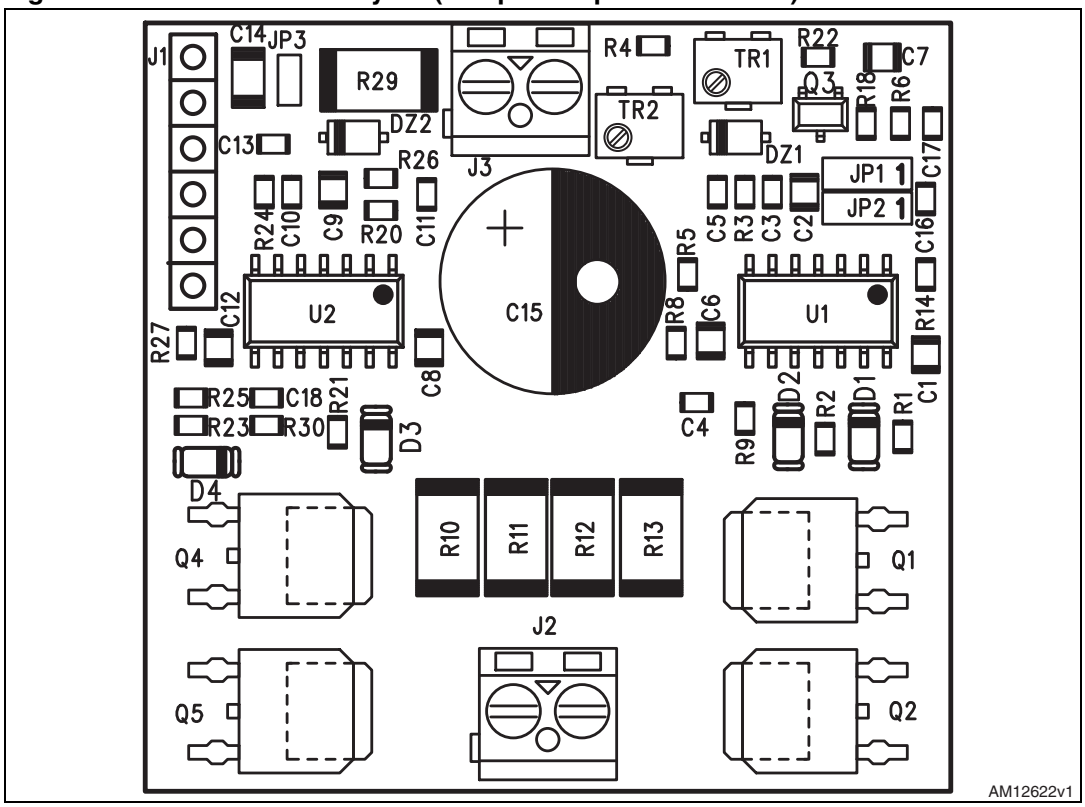


Figure 5. EVAL6393FB – layout (component placement view)



2 Revision history

Table 7. Document revision history

Date	Revision	Changes
23-Oct-2012	1	Initial release.

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