

ESD protection and signal booster for HDMI™ 1.3 Tx control links

Features

- HDMI 1.3. compliant from -40 to 85 °C
- CEC, DDC, 5 V and HPD 8 kV contact ESD protection
- Integrated I²C bi-directional reshaping circuit and level-shifter
- Integrated CEC bi-directional level-shifter with dV/dt limiter
- Supports direct connection to low-voltage HDMI ASICs (down to 1.8 V)
- Backdrive current protection on all I/O pins
- HDMI short-circuit and overcurrent protection on 5 V output
- Long HDMI cable drive support
- 500 µm pitch

Benefits

- Most stringent ESD standards compliance guaranteed at system level
- Full protection of ultra-sensitive HDMI ASICs
- Optimized HDMI control signal shapes guaranteed at connector level
- Signal booster for long HDMI cable support
- High integration
- Companion chip for HDMIULC6-xxx6 ultra-large bandwidth ESD protection for TMDS links
- Companion chip for STMicroelectronics' STixxxx HDMI HD decoders.
- Referenced in STi7111-SAT-MB-V1.2-011 reference design from STMicroelectronics

Complies with the following standards:

- IEC 61000-4-2 level 4
- JESD22-A114D level 2

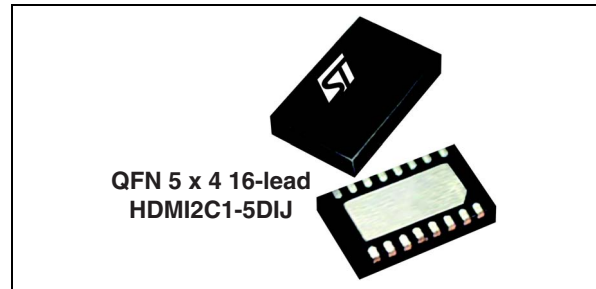
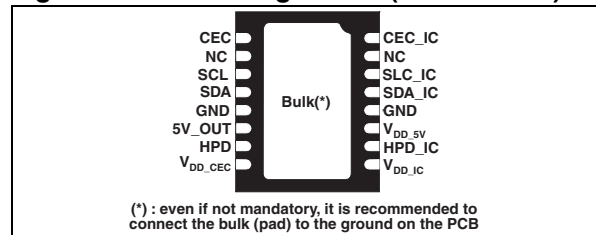


Figure 1. Pin configuration (bottom view)



Applications

- Consumer and computer electronics
- HD set-top boxes, DVD and flat television sets
- PC graphic cards

Description

The HDMI2C1-5DIJ is a fully integrated ESD protection, level-shifting device and signal booster for control links of HDMI 1.3 transmitters.

This device is a bi-directional isolation buffer, integrating hysteresis and signal boosters for maximum system robustness and signal integrity. All these features are provided in a single 16-lead QFN package featuring straightforward routing.

The HDMI2C1-5DIJ is a simple plug and play device that provides HDMI designers with an easy way to gain full compliance with the stringent HDMI 1.3 CTS on a wide temperature range.

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1 Application information

1.1 Power on reset

In order to activate the CEC and DDC lines, both following conditions must be respected:

- $V_{DD_5V} > V_{DD_ON}$ (see [Table 3](#))
- Both inputs of the bi-directional level shifters must be set to a high level at the same time

1.2 CEC input and output levels in high-level

When the CEC signal is set to a high level (idle-state), pin 1 and pin 16 voltages can be different as the HDMI2C1-5DIJ works as a level-shifter. The line is then considered in open circuit between these two pins. Low levels are identical on both sides.

1.3 Schematics

Figure 2. Application schematic

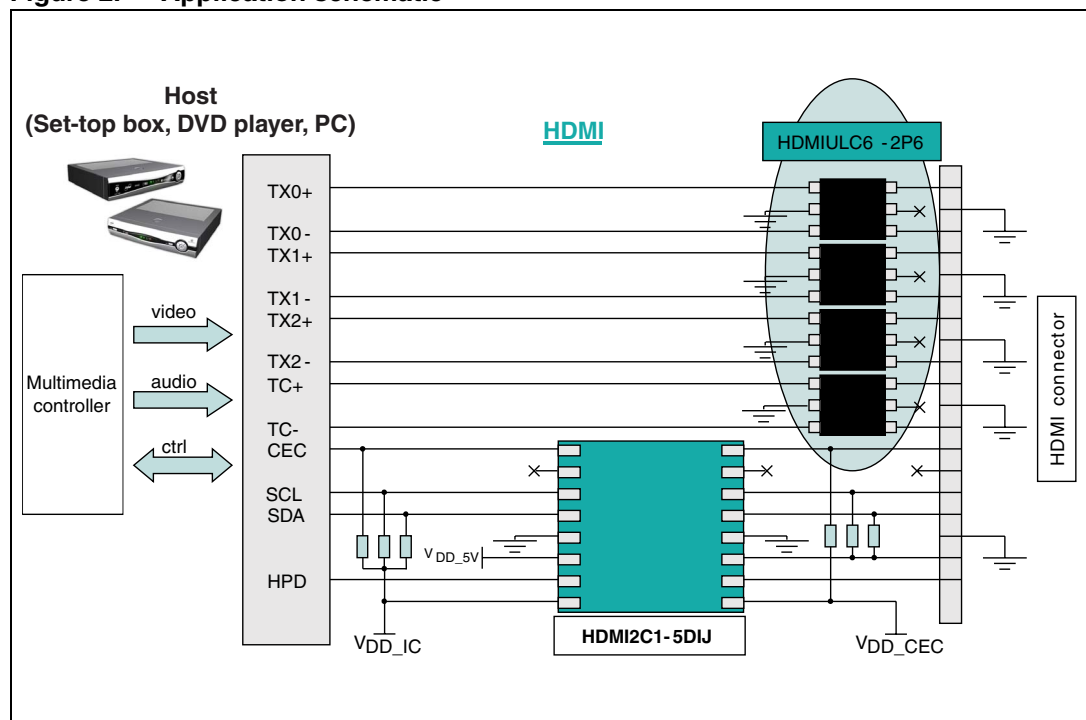


Figure 3. Electrical schematic

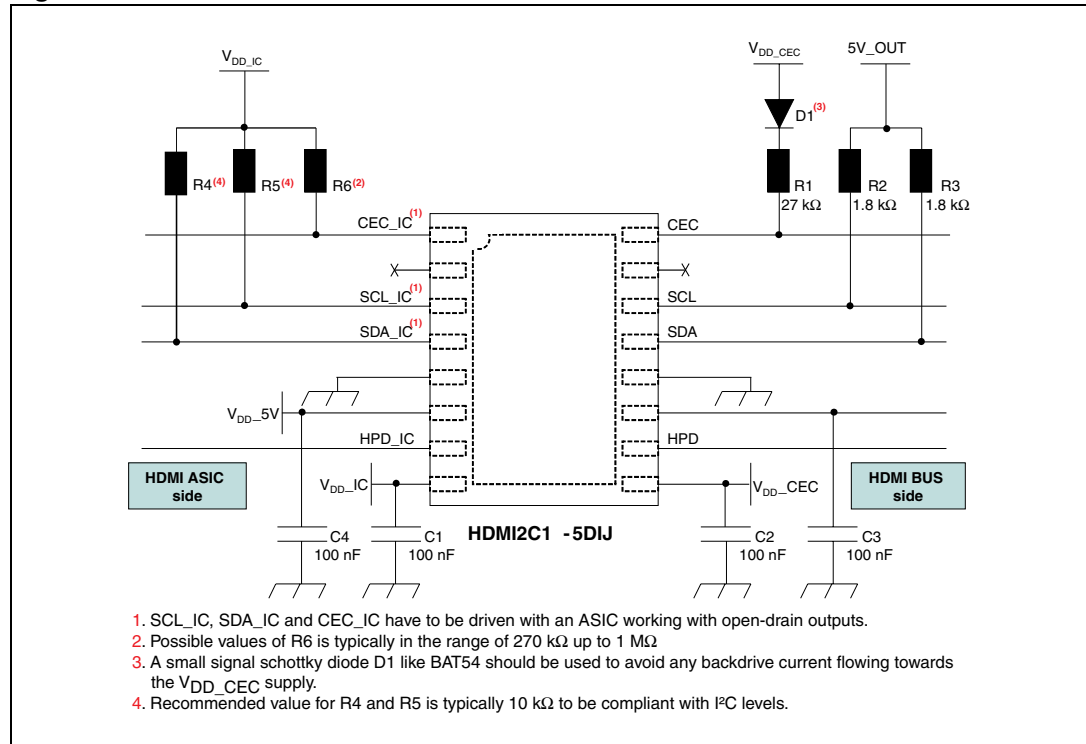


Table 1. Pin descriptions

Pin	Name	Description
1	CEC_IC	Consumer electronic control (HDMI ASIC side)
2	N.C.	----
3	SLC_IC	DDC I ² C clock line (HDMI ASIC side)
4	SDA_IC	DDC I ² C data line (HDMI ASIC side)
5	GND	Ground
6	V _{DD_5V}	5 V supply
7	HPD_IC	Hot plug detect signal (HDMI ASIC side)
8	V _{DD_IC}	ASIC logic level reference voltage
9	V _{DD_CEC}	CEC line logic level reference voltage
10	HPD	Hot plug detect signal (HDMI bus side)
11	5V_OUT	Current limiter output (HDMI bus side)
12	GND	Ground
13	SDA	DDC I ² C data line (HDMI Bus side)
14	SCL	DDC I ² C clock line (HDMI Bus side)
15	N.C.	----
16	CEC	Consumer electronic control (HDMI Bus side)

**QFN 5 X 4 16-lead
Top view**

Figure 4. CEC link functional schematic

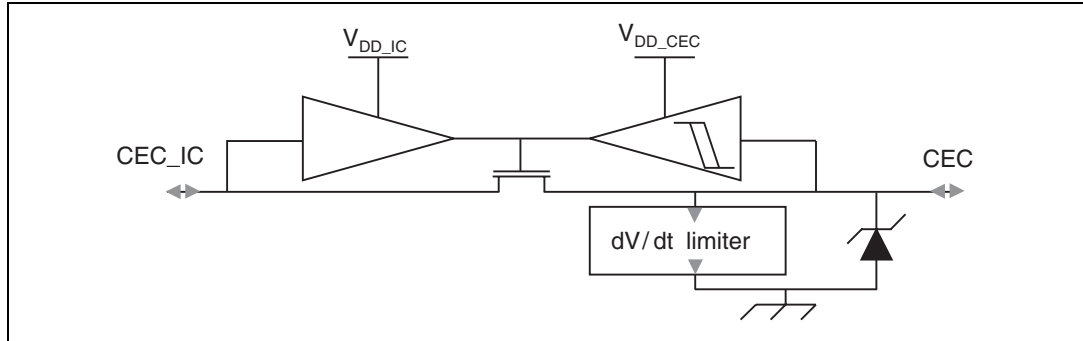


Figure 5. HPD link functional schematic

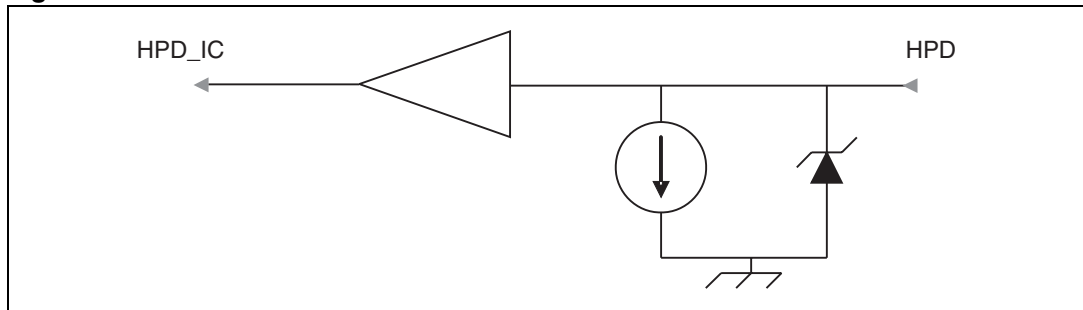


Figure 6. DDC link functional schematic

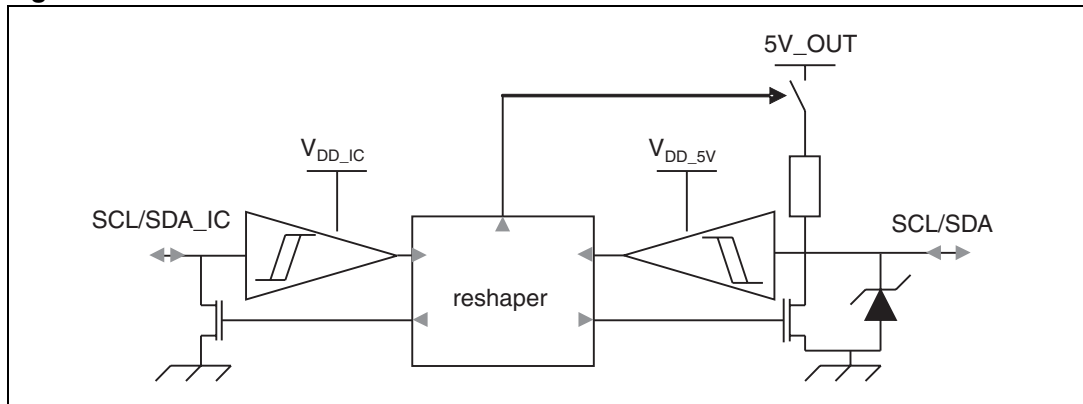
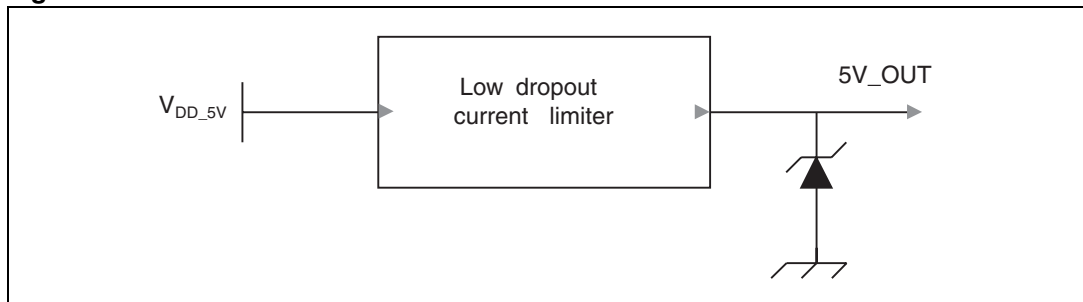


Figure 7. 5 V link functional schematic



2 Characteristics

Table 2. Absolute ratings

Symbol	Parameter	Test conditions	Value	Unit
V_{pp_BUS}	ESD discharge on HDMI BUS side (pin 10, 11, 13, 14,16), IEC 61000-4-2 level 4	Contact discharge	$\pm 8^{(1)}$	kV
V_{pp_IC}	ESD discharge (all pins), HBM JESD22-A114D level 2	Contact discharge	± 2	kV
T_{stg}	Storage temperature range		-55 to +150	°C
T_{op}	Operating temperature range		-40 to +85	°C
T_L	Maximum lead temperature for soldering during 10 s		260	°C
V_{DD_5V} V_{DD_IC} V_{DD_CEC}	Supply voltages		6	V
I_{DDC_IC}	Maximum allowed current sunk by SDA_IC or SCL_IC		1.5	mA

1. With a 100 nF capacitor connected to the 5 V output pin.

Table 3. Power supply characteristics

Symbol	Parameter	Test conditions	Value			Unit
			Min.	Typ.	Max.	
V_{DD_CEC}	CEC supply voltage		2.97	3.3	3.63	V
V_{DD_IC}	Low-voltage supply		1.62		3.63	V
V_{DD_5V}	5 V input supply voltage range		4.9		5.3	V
$V_{DD_ON}^{(1)}$	Power on reset				4.1	V
I_{QS_5V}	Quiescent currents on V_{DD_5V} , V_{DD_IC} , V_{DD_CEC} Idle-state on CEC and DDC links, HPD and 5V_OUT links open	$V_{DD_5V} = 5\text{ V}$, $V_{DD_IC} = 1.8\text{ V}$, $V_{DD_CEC} = 3.3\text{ V}$			1000	μA
I_{QS_IC}					75	
I_{QS_CEC}					150	

1. In order to activate the CEC and DDC lines, both the following conditions must be respected:
 - $V_{DD_5V} > V_{DD_ON}$
 - Both inputs of the bi-directional level shifters must be set to a high level at the same time.

Table 4. CEC electrical characteristics⁽¹⁾

Symbol	Parameter	Test conditions	Value			Unit
			Min.	Typ.	Max.	
V _{Tup_CEC}	Upward input voltage threshold on bus side				2.0	V
V _{Tdown_CEC}	Downward input voltage threshold on bus side		0.8			V
V _{HYST_CEC}	Input hysteresis on bus side			0.4		V
T _{RISE_CEC}	Output rise-time	R _{UP} = 27 kΩ ± 5%	25 ⁽²⁾		250	μs
T _{FALL_CEC}	Output fall-time	R _{UP} = 27 kΩ ± 5%			50	μs
I _{OFF_CEC}	Leakage current in powered-off state	V _{DD_5V} = 0 V, V _{DD_IC} = 0 V, V _{DD_CEC} = 3.3 V			1.8	μA
V _{IL_CEC_IC}	Input low level on IC side		30			%V _{DD_IC}
V _{IH_CEC_IC}	Input high level on IC side				70	%V _{DD_IC}
R _{ON_CEC}	On resistance across CEC and CEC_IC pins	CEC pin to 0 V		115	160	Ω
C _{in_CEC}	Input capacitance on CEC link	V _{DD_5V} = 0 V, V _{DD_CEC} = 0 V, V _{DD_IC} = 0 V, V _{BIAS} = 0 V, F = 100 kHz		17	25 ⁽³⁾	pF

1. T_{amb} = 25 °C, V_{DD_CEC} = 3.3 V, V_{DD_5V} = 5 V, unless otherwise specified.
2. The dV/dt limiter is used to ensure a minimum rise-time when a minimum load is connected to the link.
3. Maximum capacitance allowed at connector output is 200 pF in HDMI 1.3 specification.

Table 5. HDMI 5V_out current limiter electrical characteristics (T_{amb} = 25 °C, V_{DD_5V} = 5 V)

Symbol	Parameter	Test conditions	Value			Unit
			Min.	Typ.	Max.	
V _{DROP}	Drop-out voltage	I _{5V_OUT} = 55 mA	20	50	95 ⁽¹⁾	mV
I _{5V_OUT}	Output current	V _{5V_OUT} = 0 V	55		115 ⁽²⁾	mA

1. HDMI 1.3 specification requires a maximum of 100 mV voltage-drop.
2. Maximum allowed output current is 500 mA when the sink is powered off in HDMI 1.3 specification.

Table 6. Hot-plug detect electrical characteristics (T_{amb} = 25 °C, V_{DD_5V} = 5 V)

Symbol	Parameter	Test conditions	Value			Unit
			Min.	Typ.	Max.	
I _{PULL_DOWN}	Pull-down current			13	25	μA
V _{IL_HPD}	Input low-level		1			V
V _{IH_HPD}	Input high-level				1.7	V

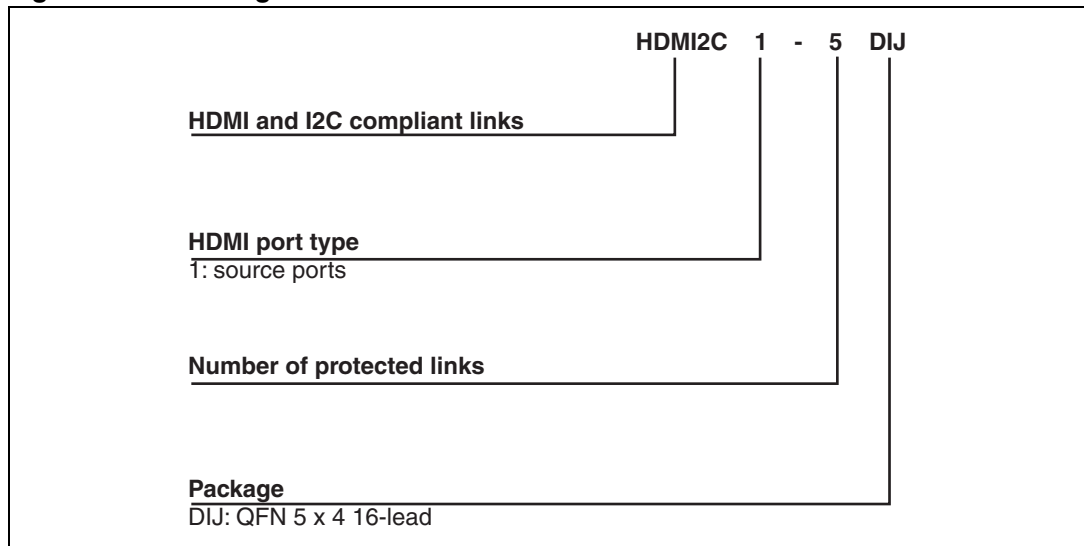
Table 7. DDC SDA/SCL electrical characteristics⁽¹⁾

Symbol	Parameter	Test conditions	Value			Unit
			Min.	Typ.	Max.	
V_{Tup_BUS}	Upward input voltage threshold on bus side				3.5	V
V_{Tdown_BUS}	Downward input voltage threshold on bus side		1.5			V
V_{HYST_BUS}	Input hysteresis on bus side		1		1.3	V
V_{OL_BUS}	Output low-level	Current sunk by SDA or SCL pin is 3 mA			350	mV
T_{RISE_BUS}	Output rise-time (30%-70%)	$C_{BUS} = 750 \text{ pF}^{(2)}$, $R_{UP} = 2 \text{ k}\Omega // 47 \text{ k}\Omega + 10 \%^{(3)}$			900	ns
T_{FALL_BUS}	Output fall-time (30%-70%)				250	ns
V_{Tup_IC}	Upward input voltage threshold on IC side		55		65	$\%V_{DD_IC}$
V_{Tdown_IC}	Downward input voltage threshold on IC side		35		45	$\%V_{DD_IC}$
V_{OL_IC}	Output low-level on IC side	Current sunk by SDA_IC or SCL_IC pins is 500 μ A			324 ⁽⁴⁾	mV
C_{IN_DDC}	Input capacitance on DDC link	$V_{DD_5V} = 0 \text{ V}$, $V_{DD_IC} = 0 \text{ V}$, $V_{DD_CEC} = 0 \text{ V}$, $V_{BIAS} = 0 \text{ V}$, $F = 100 \text{ kHz}$		11	17 ⁽⁵⁾	pF

1. $T_{amb} = 25 \text{ }^\circ\text{C}$, $V_{DD_5V} = 5 \text{ V}$, unless otherwise specified.
2. Maximum load capacitance allowed on I2C entire link (cable plus connectors) is 750 pF in HDMI spec. 1.3.
3. Two pull-up resistors in parallel (sink + source). Typical value is 47 k Ω and maximum value is 47 k Ω + 10% in HDMI 1.3 specification.
4. $V_{OL_IC} = 0.2 * V_{DD_IC}$ (min).
5. Maximum capacitance allowed at connector output is 50 pF in HDMI spec. 1.3.

3 Ordering information scheme

Figure 8. Ordering information scheme



4 Package information

- Epoxy meets UL94, V0
- Lead-free packages

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Table 8. QFN 5 x 4 16 leads dimensions

Ref.	Dimensions					
	Millimetres			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.80	0.90	1.00	0.031	0.035	0.039
A1	0.00	0.02	0.05	0.000	0.001	0.002
b	0.18	0.25	0.30	0.007	0.010	0.012
D	4.90	5.00	5.10	0.193	0.197	0.201
D2	4.20	4.35	4.45	0.165	0.171	0.175
E	3.90	4.00	4.10	0.154	0.157	0.161
E2	2.30	2.45	2.55	0.091	0.097	0.100
e		0.50			0.020	
k	0.20			0.008		
L	0.30	0.40	0.50	0.012	0.016	0.020

Figure 9. QFN 5 x 4 16-lead footprint (dimensions in mm)

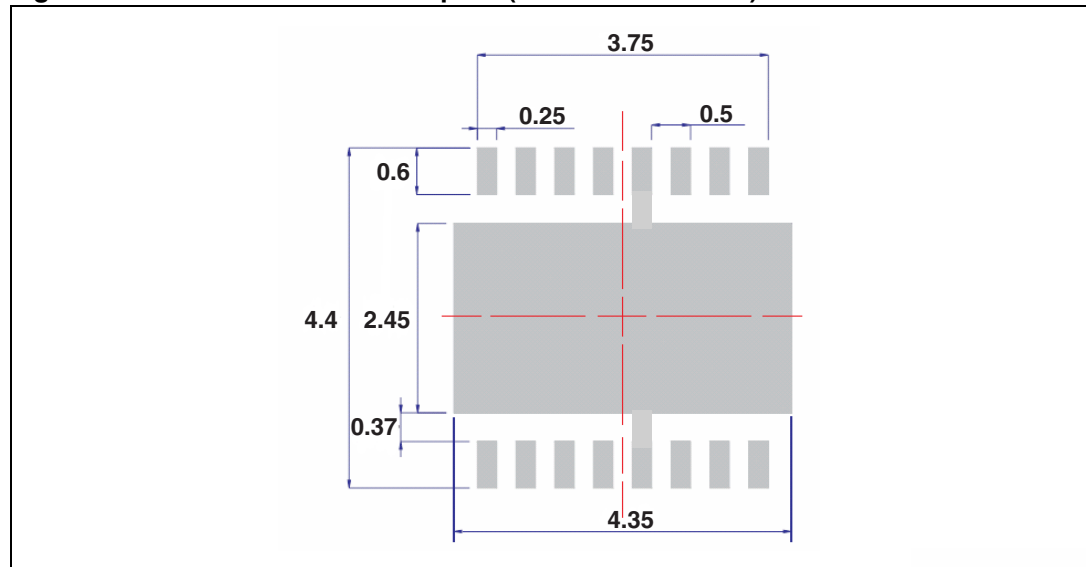
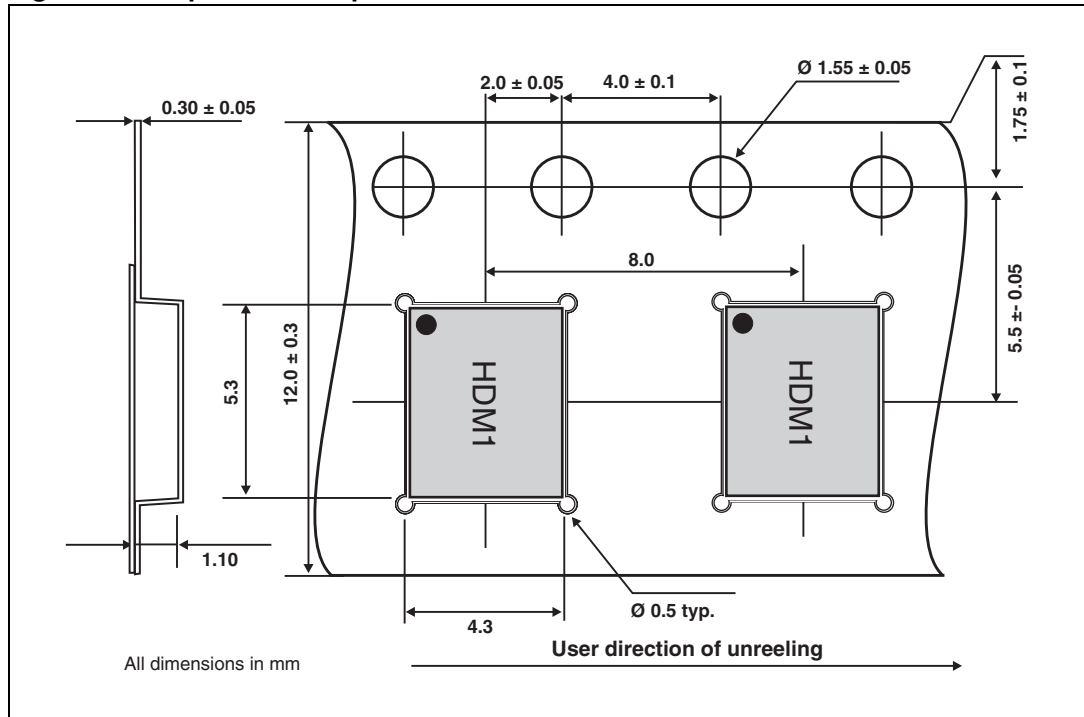


Figure 10. Tape and reel specification



5 Ordering information

Table 9. Ordering information

Order code	Marking	Package	Weight	Base qty	Delivery mode
HDMI2C1-5DIJ	HDM1	QFN 5x4 16-lead	60 mg	3000	Tape and reel

6 Revision history

Table 10. Document revision history

Date	Revision	Changes
05-Feb-2009	1	Initial release.
18-Mar-2009	2	Added Table 1 Pin descriptions. Updated Figure 2 and Figure 3 for connection of resistor R4 to HPD.
19-May-2011	3	<p>Figure 1:</p> <ul style="list-style-type: none"> - add "NC" to not connected pins - change "GND" ref of the pad into "bulk" reference - add comment about the "bulk" on the bottom <p>Figure 9:</p> <ul style="list-style-type: none"> - connect "GND" pins to the heatsink copper surface. <p>Updated Figure 2 and Figure 3.</p> <p>Table 2:</p> <p>Updated V_{pp_Bus} parameter.</p>

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