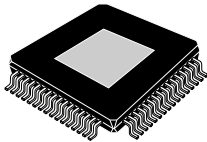



4 x 80W digital input class-D automotive audio amplifier with Hi-Fi audio quality, advanced diagnostics, 2 MHz switching frequency and High Resolution Bandwidth



**LQFP64 (exposed pad up)**

## Features

- AEC-Q100 qualification on going 
- Integrated 120 dB D/A conversion
- I<sup>2</sup>S and TDM digital input (up to 16 CH TDM)
- Selectable input sample rate frequency (44.1/48/96/192 kHz)
- Wide supply operating range: 4.5 V - 2518 V (5 V min at turn-on transition)
- PWM 2 MHz switching PWM:
  - Reduced size and cost of output LC
- High Resolution Bandwidth support:
  - Up to 40 kHz (I<sup>2</sup>S 96 kHz) with attenuation [0 dB, -2 dB]
  - Up to 80 kHz (I<sup>2</sup>S 192 kHz) with attenuation [0 dB, -2 dB]
- 4 I<sup>2</sup>C addresses
- 4 Ω, 2 Ω, 1 Ω driving with output channels parallelization
- MOSFET power outputs allowing high output power capability:
  - Typ 4 x 30 W /4 Ω @ 14.4 V, 1 kHz THD = 10%
  - Typ 4 x 25 W /4 Ω @ 14.4 V, 1 kHz THD = 1%
  - Typ 4 x 50 W /2 Ω @ 14.4 V 1 kHz THD =10 %
  - Typ 4 x 80 W /4 Ω @ 25V V, 1 kHz THD =10 %
- I<sup>2</sup>C full configurability and diagnostic:
  - 4 x Thermal warning and average junction temperature measurement on I<sup>2</sup>C (8 bits)
  - AC and DC diagnostic (independent of channel)
  - OCP protection scheme configurable (4 x OCP limit selectable)
  - Mute time configuration
  - DIM (digital impedance meter)
  - Feedback after filter configuration
- Capability to run complete diagnostic in play:
  - Short to GND/VCC
  - DC offset detector
- Extremely Low noise:
  - 13 μV A-weighted; 20 kHz (high gain) typ
- Very low THD:
  - 0.02% at 1 W 1 kHz on 4 and 2 Ω loads typ
  - 0.08% 20-20 kHz (full audio band) on 4 and 2 Ω loads (1 W)
- CD/Diag pin (3 selectable CD thresholds)
- Synchronization output pin (only with TDM input stream, on I<sup>2</sup>Sdata2)
- Channel independent Mute/Play/Gain selection/Diagnostic
- Real Time current monitor
- Open Load in play
- Battery load dump compatible (40 V)

| Product status link      |                         |           |
|--------------------------|-------------------------|-----------|
| <a href="#">HFDA801A</a> |                         |           |
| Product summary          |                         |           |
| Order code               | Package                 | Packing   |
| HFDA801A-VYY             | LQFP64<br>(exp. pad up) | Tray      |
| HFDA801A-VYT             |                         | Tape&Reel |

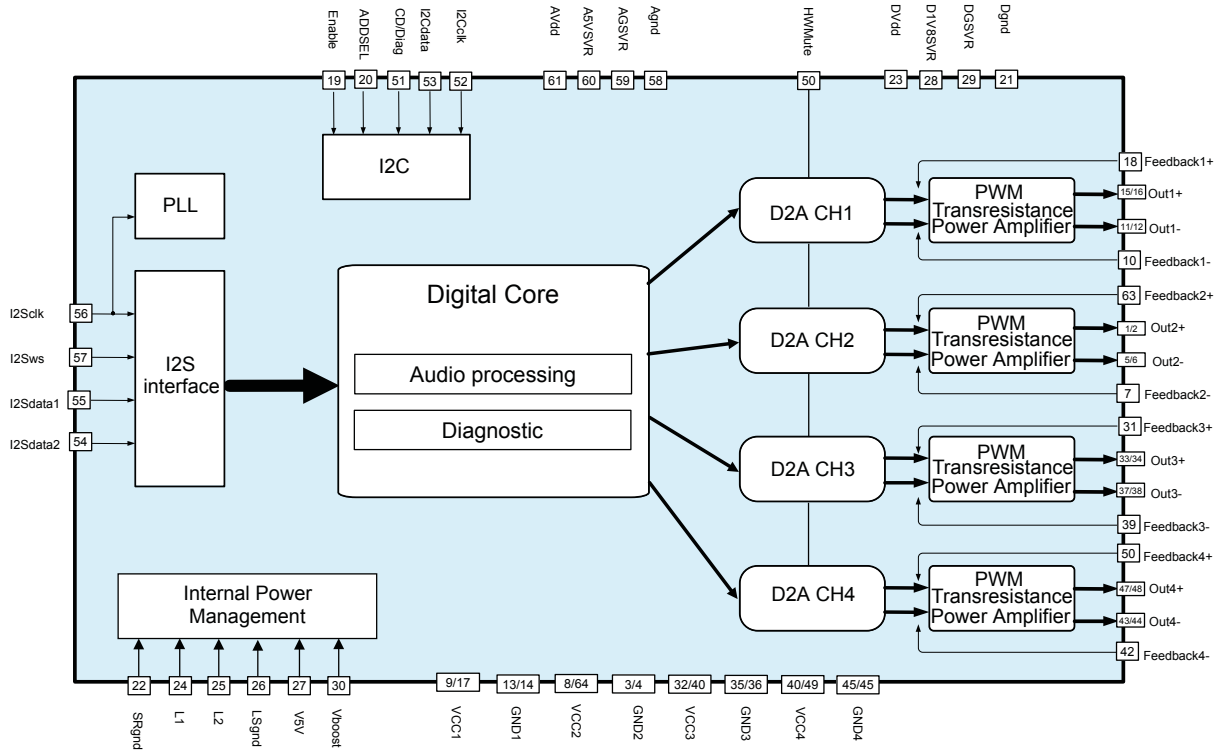
- Immune to pop/tick noise at turn on /off, battery variations (inside the operative range), during diagnostic
- EMI compliance evaluated according to CISPR25
- Legacy (no I<sup>2</sup>C mode)
- Integrated short circuit protections
- ESD integrated protections (2 kV HBM, 500 V / 750 V corner CDM)
- LQFP64 exposed pad up package

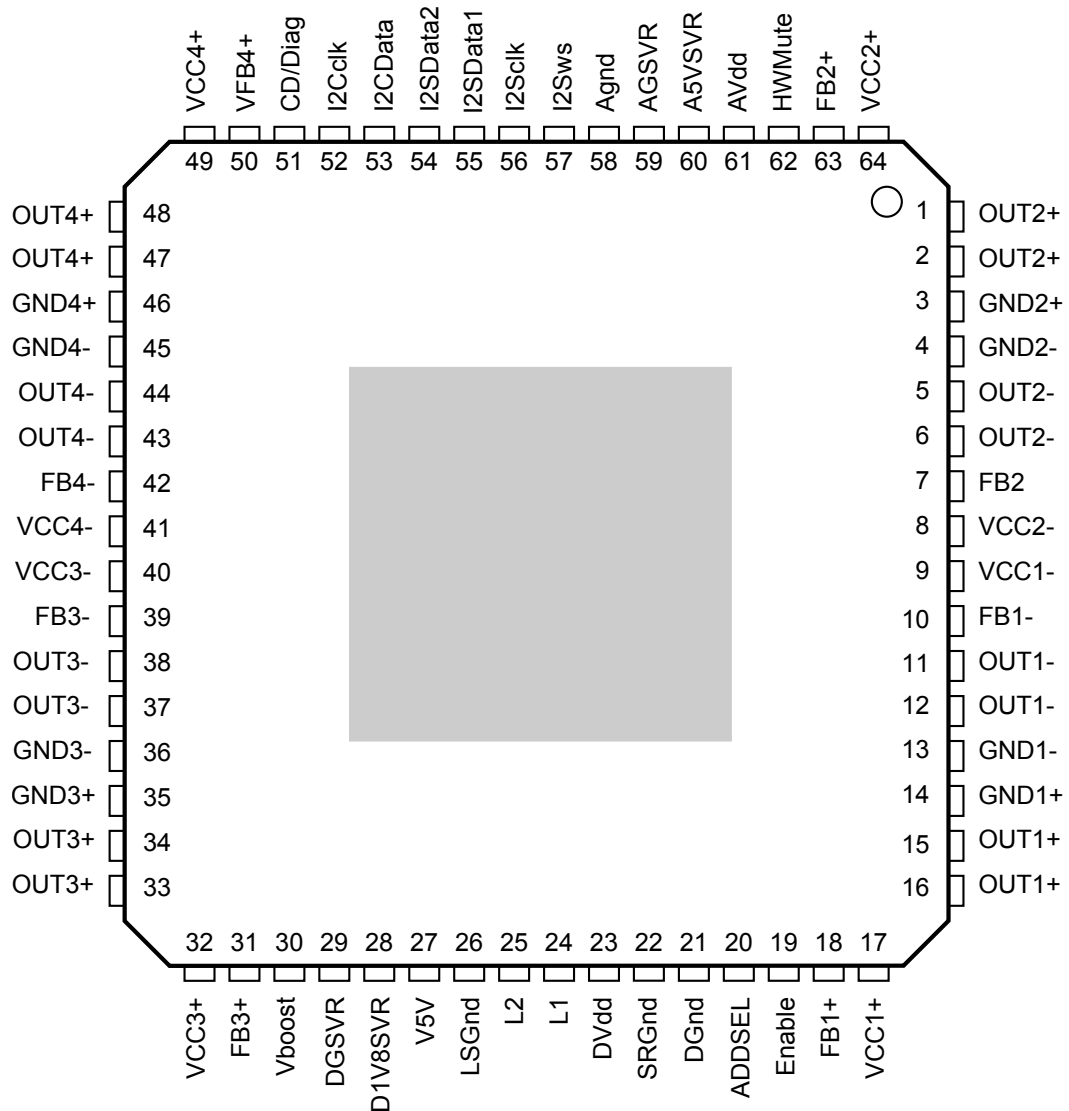
## Description

HFDA801A is the new ST class-D audio amplifier, specifically designed for automotive applications in the latest BCD technology. The HFDA801A integrates a 24-bits 120 dB DAC conversion, and features 2 MHz switching PWM class D output stage. This configuration enables the design of a compact and inexpensive application, reaching at the same time outstanding level of audio performances. HFDA801A supports wide band applications (80 kHz), with extremely low level of noise and low THD. Moreover it features the most complete diagnostic matrix, including full diagnostic in play to support the most demanding OEM requirements in terms of speaker control and system robustness/ reliability. HFDA801A supports start stop cranking down to 4.5 V (5 V at turn on) and it is housed in a very compact and thin LQFP 10x10 package. Thus the HFDA801A is suitable for any level of automotive application.

# 1 Block diagram and pins description

Figure 1. Block diagram



**Figure 2. Pin connection diagram (top view)**

**Table 1. Pins list description**

| #  | Pin   | Function                                   |
|----|-------|--|
| 1  | OUT2+ | Channel 2, half bridge plus, Output        |
| 2  | OUT2+ | Channel 2, half bridge plus, Output        |
| 3  | GND2+ | Channel 2, half bridge plus, Power Ground  |
| 4  | GND2- | Channel 2, half bridge minus, Power Ground |
| 5  | OUT2- | Channel 2, half bridge minus, Output       |
| 6  | OUT2- | Channel 2, half bridge minus, Output       |
| 7  | FB2-  | Channel 2, half bridge minus, Feedback     |
| 8  | VCC2- | Channel 2, half bridge minus, Power Supply |
| 9  | VCC1- | Channel 1, half bridge minus, Power Supply |
| 10 | FB1-  | Channel 1, half bridge minus, Feedback     |
| 11 | OUT1- | Channel 1, half bridge minus, Output       |

| #  | Pin     | Function  |
|----|---------|---|
| 12 | OUT1-   | Channel 1, half bridge minus, Output                        |
| 13 | GND1-   | Channel 1, half bridge minus, Power Ground                  |
| 14 | GND1+   | Channel 1, half bridge plus, Power Ground                   |
| 15 | OUT1+   | Channel 1, half bridge plus, Output                         |
| 16 | OUT1+   | Channel 1, half bridge plus, Output                         |
| 17 | VCC1+   | Channel 1, half bridge plus, Power Supply                   |
| 18 | FB1+    | Channel 1, half bridge plus, Feedback                       |
| 19 | Enable  | Enable pin  |
| 20 | ADDSEL  | Address selection pin, input                                |
| 21 | DGnd    | Digital ground  |
| 22 | SRGnd   | Power management ground 1                                   |
| 23 | DVdd    | Digital Power Supply  |
| 24 | L1      | Power management inductor side1                             |
| 25 | L2      | Power management inductor side2                             |
| 26 | LSGnd   | Power management ground 2                                   |
| 27 | V5V     | Internal 5V supply  |
| 28 | D1V8SVR | Positive digital supply V(SVR)+0.9 V (Internally generated) |
| 29 | DGSVR   | Negative digital supply V(SVR)-0.9 V (Internally generated) |
| 30 | Vboost  | Internal boost supply                                       |
| 31 | FB3+    | Channel 3, half bridge plus, Feedback                       |
| 32 | VCC3+   | Channel 1, half bridge plus, Power Supply                   |
| 33 | OUT3+   | Channel 3, half bridge plus, Output                         |
| 34 | OUT3+   | Channel 3, half bridge plus, Output                         |
| 35 | GND3+   | Channel 3, half bridge plus, Power Ground                   |
| 36 | GND3-   | Channel 3, half bridge minus, Power Ground                  |
| 37 | OUT3-   | Channel 3, half bridge minus, Output                        |
| 38 | OUT3-   | Channel 3, half bridge minus, Output                        |
| 39 | FB3-    | Channel 3, half bridge minus, Feedback                      |
| 40 | VCC3-   | Channel 3, half bridge minus, Power Supply                  |
| 41 | VCC4-   | Channel 4, half bridge minus, Power Supply                  |
| 42 | FB4-    | Channel 4, half bridge minus, Feedback                      |
| 43 | OUT4-   | Channel 4, half bridge minus, Output                        |
| 44 | OUT4-   | Channel 4, half bridge minus, Output                        |
| 45 | GND4-   | Channel 4, half bridge minus, Power Ground                  |
| 46 | GND4+   | Channel 4, half bridge plus, Power Ground                   |
| 47 | OUT4+   | Channel 4, half bridge plus, Output                         |
| 48 | OUT4+   | Channel 4, half bridge plus, Output                         |
| 49 | VCC4+   | Channel 4, half bridge plus, Power Supply                   |
| 50 | FB4+    | Channel 4, half bridge plus, Feedback                       |
| 51 | CD/Diag | Clipping detector and diagnostic output pin                 |
| 52 | I2CClk  | I2C Clock   |

| #  | Pin      | Function  |
|----|----------|---|
| 53 | I2CData  | I2C Data  |
| 54 | I2SData2 | I2S/TDM Data input 2  |
| 55 | I2SData1 | I2S/TDM Data input 1  |
| 56 | I2Sclk   | I2S/TDM Clock input   |
| 57 | I2Sws    | I2S/TDM Sync input  |
| 58 | Agnd     | Analog ground   |
| 59 | AGSVR    | Negative Analog Supply V(SVR)-2.5 V (Internally generated) <sup>(1)</sup> |
| 60 | A5VSVR   | Positive Analog Supply V(SVR)+2.5 V (Internally generated)                |
| 61 | AVdd     | Analog supply   |
| 62 | HWMute   | Hardware mute pin   |
| 63 | FB2+     | Channel 2, half bridge plus, Feedback                                     |
| 64 | VCC2+    | Channel 2, half bridge plus, Power Supply                                 |

1. Internal circuit output pin: not to be controlled externally. AMR not applicable.

## 2 Electrical specifications

### 2.1 Absolute maximum ratings

**Table 2. Absolute maximum ratings**

| Symbol   | Parameter  | Value       | Unit |
|--|--|-------------|------|
| VCC  | DC supply voltage                                      | -0.3 to 32  | V    |
| [V <sub>CC(x)+</sub> , V <sub>CC(x)-</sub> , A <sub>VDD</sub> , D <sub>VDD</sub> ]   | Transient supply voltage for t = 100 ms <sup>(1)</sup> | -0.3 to 40  | V    |
| GND <sub>max</sub>   | Ground pin voltage difference                          | -0.3 to 0.3 | V    |
| [GND <sub>(x)+</sub> , GND <sub>(x)-</sub> , A <sub>GND</sub> , D <sub>GND</sub> , SR <sub>GND</sub> , LS <sub>GND</sub> ]               |  |             |      |
| FB <sub>(x)+</sub> , FB <sub>(x)-</sub>  | Feedback pin   | -0.3 to 32  | V    |
| OUT <sub>(x)+</sub> , OUT <sub>(x)-</sub>  | Output pin   | -0.3 to 32  | V    |
| L1   | Internal Regulator pin                                 | -0.3 to 32  | V    |
| L2   | Internal Regulator pin                                 | -0.3 to 40  | V    |
| I <sup>2</sup> C <sub>data</sub> , I <sup>2</sup> C <sub>clk</sub>   | I <sup>2</sup> C bus pins voltage                      | -0.3 to 5.5 | V    |
| I <sup>2</sup> S <sub>data1</sub> , I <sup>2</sup> S <sub>data2</sub> , I <sup>2</sup> S <sub>clk</sub> , I <sup>2</sup> S <sub>WS</sub> | I <sup>2</sup> S bus pins voltage                      | -0.3 to 5.5 | V    |
| Enable   | Enable pin voltage                                     | -0.3 to 5.5 | V    |
| CD/Diag  | CD/DIAG pin  | -0.3 to 5.5 | V    |
| HWMute   | Hardware Mute  | -0.3 to 5.5 | V    |
| T <sub>amb</sub>   | Ambient operating temperature                          | -40 to 105  | °C   |
| T <sub>stg</sub> , T <sub>j</sub>  | Storage and junction temperature                       | -55 to 150  | °C   |
| ESD <sub>HBM</sub>   | ESD protection HBM <sup>(2)</sup>                      | 2000        | V    |
| ESD <sub>CDM</sub>   | ESD protection CDM <sup>(2)</sup>                      | 500         | V    |

- Ramp time  $T_r = 2$  ms
- Definition according to the international standard

### 2.2 Thermal data

**Table 3. Thermal data**

| Symbol            | Parameter                                       | Value | Unit |
|-------------------|---|-------|------|
| R <sub>thjc</sub> | R <sub>th</sub> junction to case <sup>(1)</sup> | 1.26  | °C/W |

- Top Cold Plate as per Jedec best practice guidelines (JESD51) in contact with package top side (e-pad). Ambient temperature set to 85°C.

### 3 General description

HFDA801A is a fully digital single chip class-D amplifier with high immunity to the demodulation filter effects. The high integration level and the on-board signal processing allow excellent audio performance to be achieved. Thanks to the digital input and to the feedback strategy in the power stage, HFDA801A makes the amplifier immune from the output filter components non-linearity. The number and size of the external components are minimized.

HFDA801A includes: digital I<sup>2</sup>C and I<sup>2</sup>S interfaces, internal 24 bits DAC conversion, digital signal processing for interpolation and noise shaping, innovative self-diagnostic functions and automatic detection of wrong load connections or variation of the load, internal PLL for a clock generation. Moreover HFDA801A provides a breakthrough innovative digital impedance-meter which can communicate via I<sup>2</sup>C the output load value.

#### 3.1 Feedback topology and switching frequency

HFDA801A adopts an innovative feedback topology, where the LC filter is included in the feedback loop making the amplifier highly insensitive to the characteristics of such demodulation circuit. This solution optimizes the system performance in terms of THD and frequency response in any load condition.

Regardless of the big phase shifting introduced by the output filter the device shows an adequate phase margin for any load condition. The system stability has been designed considering:

- PWM switching variation (from 2.1 MHz to 2.3 MHz)
- Silicon temperature variation (from -40 to 150 °C)
- Load variation (both inductive and capacitive considered)
- LC demodulator filter variation and tolerance
- Voltage supply variation (from 4.5 to 2518 V)
  - Minimum Supply Voltage level during Turn-On transition = 5 V

The system has been designed to guarantee a phase margin > 45 degrees for any working condition.

The new feedback topology assures a strong control of voltage and current across the load making the diagnostic load detection reliable. Moreover, this topology allows to reach exceptionally good values of output damping factor.

#### 3.2 PWM frequencies

HFDA801A PWM frequency is well above the AM band, avoiding by architecture the EMC interference of PWM switching first harmonic. Moreover, this choice permits to optimize the size and cost of the external LC demodulation filter.

The PWM frequency depends on the I<sup>2</sup>S WS frequency as reported in the table below:

**Table 4. PWM frequency relation with I<sup>2</sup>S WS frequency**

| WS Frequency [kHz] | Nominal PWM Frequency [MHz] |
|--------------------|-----------------------------|
| 44.1               | 2.1168                      |
| 48                 | 2.304                       |
| 96                 | 2.304                       |
| 192                | 2.304                       |

#### 3.3 Load possibilities

HFDA801A supports several load possibilities and configurations. The default configuration is suitable for a 4-channels application (front/rear – left/right): 4 x 4 Ω (up to 18 V).. By means of the I<sup>2</sup>C bus bit IB1-d7,d6 it is possible to choose a 2-channels solution with parallel outputs (left/right) or a 2.1 configuration for sub-woofer application.



Possible channel configurations:

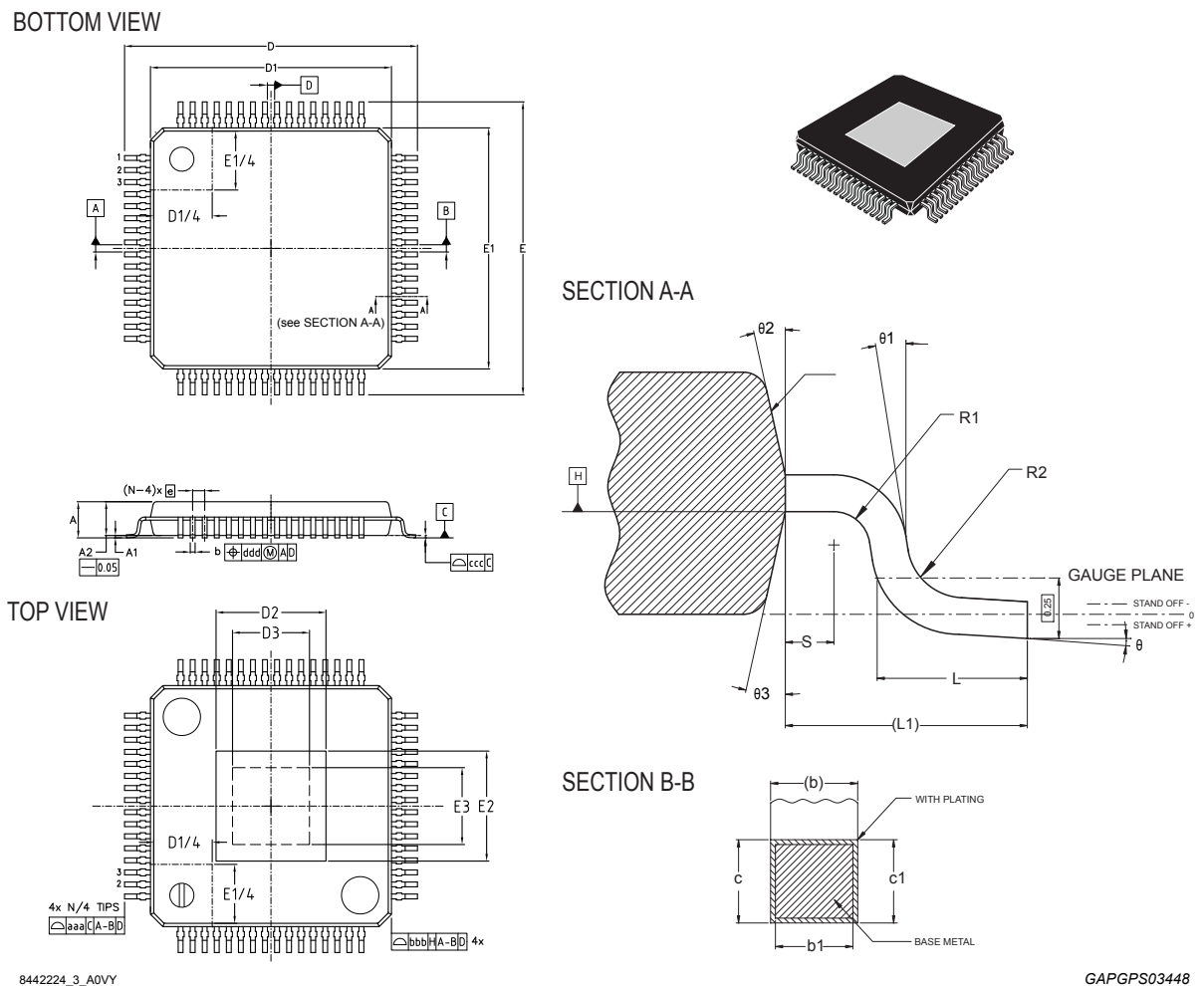
- 4 x 4  $\Omega$  (up to 25 V)
- 4 x 2  $\Omega$  (up to 18 V)
- 2 x 1  $\Omega$  (through channels connected in parallel; limited to 18 V)
- 2 x 4  $\Omega$  + 1 x 2  $\Omega$  (through parallelized channels)

## 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

### 4.1 LQFP64 (10x10x1.4 mm exp. pad up) package information

**Figure 3. LQFP64 (10x10x1.4 mm exp. pad up) package outline**

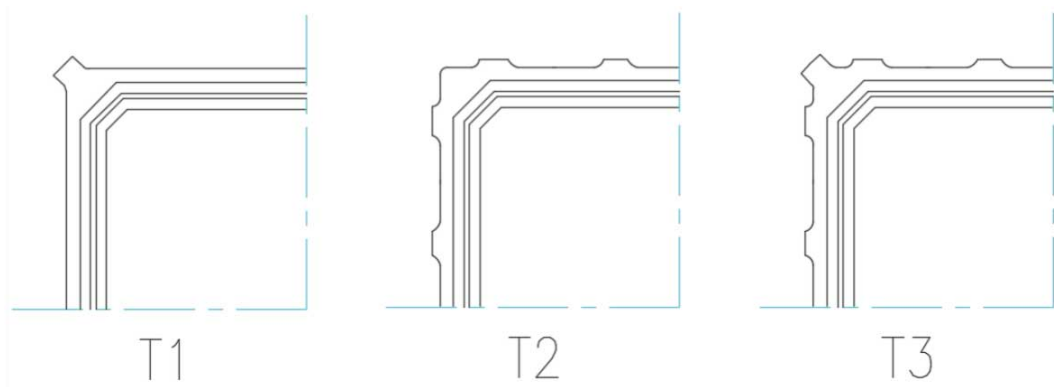


**Table 5. LQFP64 (10x10x1.4 mm exp. pad up) package mechanical data**

| Symbol     | Dimension in mm |      |      |
|------------|-----------------|------|------|
|            | Min.            | Typ. | Max. |
| $\theta$   | 0°              | 3.5° | 6°   |
| $\theta 1$ | 0°              | 9°   | 12°  |
| $\theta 2$ | 11°             | 12°  | 13°  |
| $\theta 3$ | 11°             | 12°  | 13°  |
| A          | -               | -    | 1.49 |

| Symbol  | Dimension in mm |       |      |
|---|-----------------|-------|------|
|   | Min.            | Typ.  | Max. |
| A1  | -0.04           | -     | 0.04 |
| A2  | 1.35            | 1.4   | 1.45 |
| b   | -               | -     | 0.27 |
| b1  | 0.17            | 0.2   | 0.23 |
| c   | 0.09            | -     | 0.2  |
| c1  | 0.09            | 0.127 | 0.16 |
| D   | 12.00 BSC       |       |      |
| D1 <sup>(1)(2)</sup>                            | 10.00 BSC       |       |      |
| D2  | See VARIATIONS  |       |      |
| D3  | See VARIATIONS  |       |      |
| e   | 0.50 BSC        |       |      |
| E   | 12.00 BSC       |       |      |
| E1 <sup>(1)(2)</sup>                            | 10.00 BSC       |       |      |
| E2  | See VARIATIONS  |       |      |
| E3  | See VARIATIONS  |       |      |
| L   | 0.45            | 0.6   | 0.75 |
| L1  | 1.00 REF        |       |      |
| N   | -               | 64    | -    |
| R1  | 0.08            | -     | -    |
| R2  | 0.08            | -     | 0.2  |
| S   | 0.2             | -     | -    |
| <b>Tolerance of form and position</b>           |                 |       |      |
| aaa   | -               | 0.2   | -    |
| bbb   | -               | 0.2   | -    |
| ccc   | -               | 0.08  | -    |
| ddd   | -               | 0.08  | -    |
| <b>VARIATIONS</b>                               |                 |       |      |
| <b>Pad option 6.0x6.0 (T1-T3)<sup>(3)</sup></b> |                 |       |      |
| D2  | -               | -     | 6.61 |
| E2  | -               | -     | 6.61 |
| D3  | 4.8             | -     | -    |
| E3  | 4.8             | -     | -    |

1. Dimensions D1 and E1 do not include mold flash or protrusions. Allowable mold flash or protrusion is "0.25 mm" per side.
2. The Top package body size may be smaller than the bottom package size by as much as 0.15 mm.
3. Number, dimension and position of groves shown in [Figure 4](#) are for reference only.

**Figure 4. Exposed-pad groove's shapes**

## Revision history

**Table 6. Document revision history**

| Date        | Version | Changes          |
|-------------|---------|------------------|
| 15-Gen-2021 | 1       | Initial release. |

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[500](#) [FDA4100LV](#) [MAX98306ETD+T](#) [TS4994EIJT](#) [NCP2820FCT1G](#) [NCP2823AFCT2G](#) [NCS2211MNTXG](#) [CPA2233CQ16-A1](#)  
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