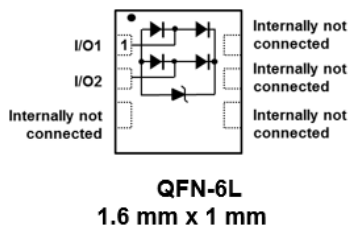


Very low clamping Ethernet 10 Gbps single line ESD protection



Features

- High ESD protection level exceeding IEC 61000-4-2 level 4:
 - $\pm 30\text{kV}$ (contact discharge)
 - $\pm 30\text{kV}$ (air discharge)
- High IEC 61000-4-5 surge capability: 10 A
- Very low dynamic resistance: 0.25 Ohm
- Low capacitance: 0.7 pF

Application

- 1G/2.5G/5G/10G Ethernet

Description

The HSP031-1BM6 is a single channel ESD array with a rail to rail architecture designed to protect 2 differential lines from over voltages event caused by ESD, surge (8/20 μs).

Packaged in a QFN-6L, the device is designed specifically for the protection of high-speed differential lines such as Ethernet 10 Gbps.

Product status link

[HSP031-1BM6](#)

Product summary

Order code	HSP031-1BM6
Package	QFN-6L
Packing	Tape and reel

1 Characteristics

Table 1. Absolute maximum ratings $T_{amb} = 25\text{ }^{\circ}\text{C}$

Symbol	Parameter		Value	Unit
V_{PP}	Peak pulse voltage	IEC 61000-4-2 contact discharge	30	kV
		IEC 61000-4-2 air discharge	30	
I_{PP}	Peak pulse current	8/20 μs	10	A
T_j	Operating junction temperature range		-55 to +150	$^{\circ}\text{C}$
T_{stg}	Storage temperature range		-55 to +150	$^{\circ}\text{C}$
T_L	Maximum lead temperature for soldering during 10 s		260	$^{\circ}\text{C}$

Figure 1. Electrical characteristics (definition)

- V_{RM} Maximum stand-off voltage
- I_{RM} Maximum leakage current @ V_{RM}
- V_{TRIG} Triggering voltage
- I_{HOLD} Holding current
- V_H Turn-off voltage

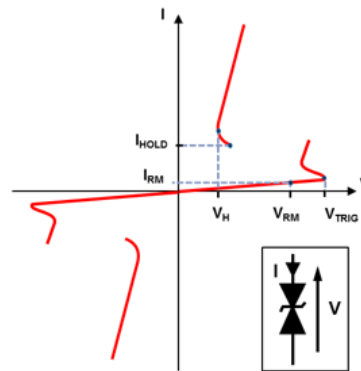


Table 2. Electrical characteristics $T_{amb} = 25\text{ }^{\circ}\text{C}$

Symbol	Parameter	Test conditions	Value			Unit
			Min.	Typ.	Max.	
V_{RM}	Reverse working voltage				3.3	V
I_{RM}	Leakage current	$V_{RM} = 3.3\text{ V}$			50	nA
V_{TRIG}	Maximum off-state voltage			9	10.5	V
I_{HOLD}	Minimum on-state current			38		mA
V_H	Minimum on-state voltage		1	1.3		V
V_{CL}	Clamping voltage	$I_{pp} = 10\text{ A} - 8/20\text{ }\mu\text{s}$			7	V
		IEC 61000-4-2, +/- 8 kV contact discharge at 30 ns		8		V
		TLP measurement (pulse duration 100 ns), $I_{pp} = 16\text{ A}$		5.9		V
R_d	TLP, pulse duration = 100 ns			0.25		Ω
C_{LINE}	Line capacitance	V I/O = 0 V, f = 3 GHz, $V_{OSC} = 30\text{ mV}$		0.7	0.9	pF
S21	Attenuation measurement	f < 600 MHz		0.1		dB
fc		-3 db		5		GHz

1.1 Characteristics (curves)

Typical curves unless otherwise specified.

Figure 2. Peak pulse current versus initial junction temperature (maximum value)

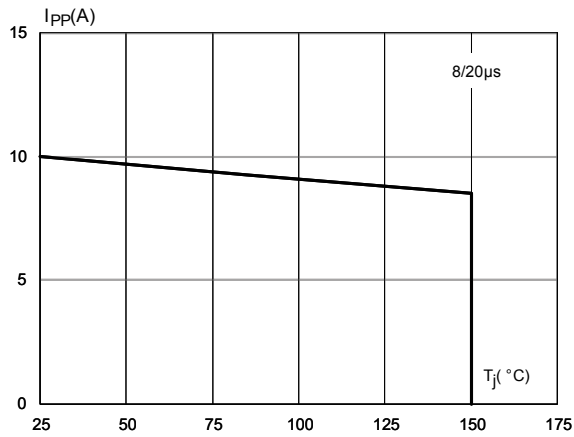


Figure 3. Peak pulse current versus clamping voltage (maximum value)

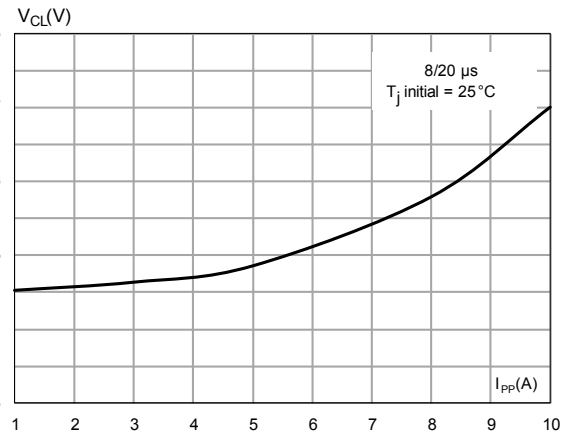


Figure 4. Leakage current versus junction temperature

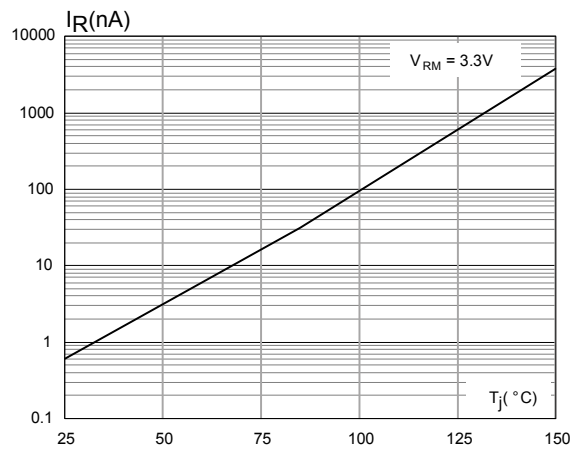


Figure 5. Leakage current versus reverse voltage

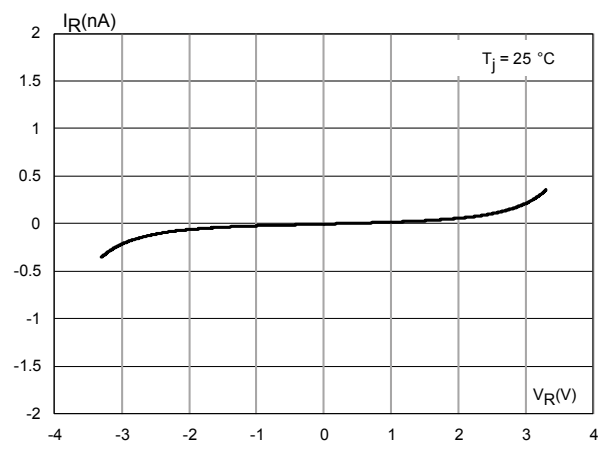


Figure 6. ESD response to IEC 61000-4-2 (+8 kV contact discharge)

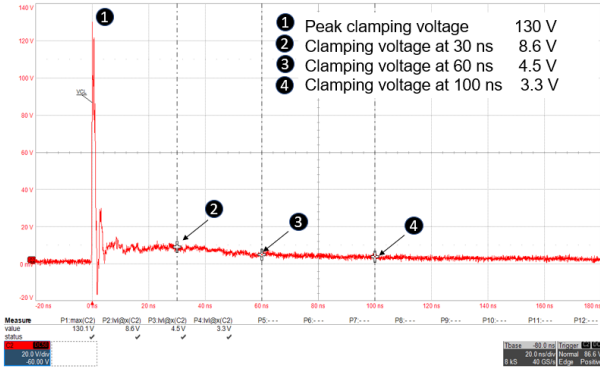


Figure 7. ESD response to IEC 61000-4-2 (-8 kV contact discharge)

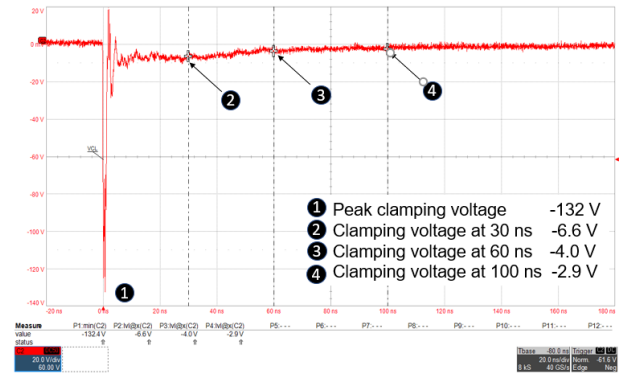


Figure 8. Positive TLP measurement

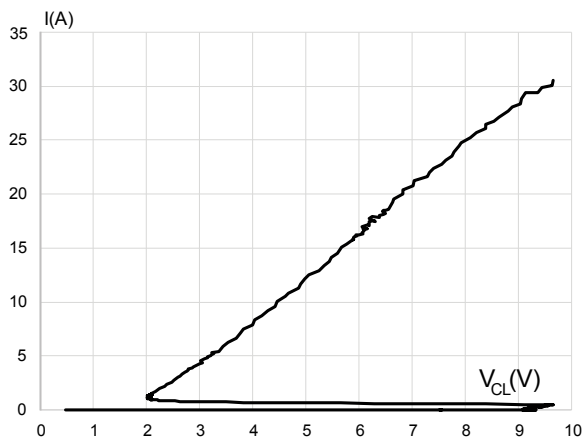


Figure 9. Negative TLP measurement

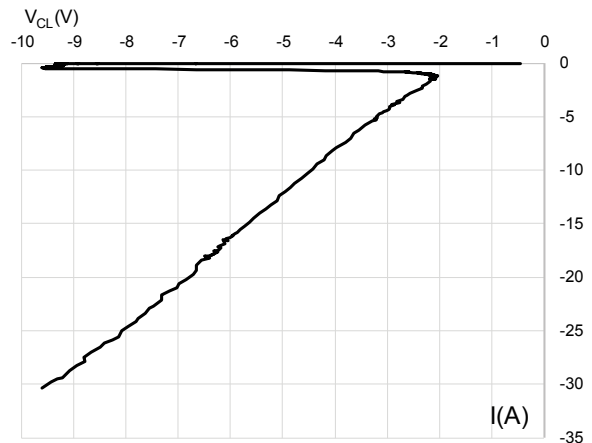


Figure 10. Line capacitance versus frequency

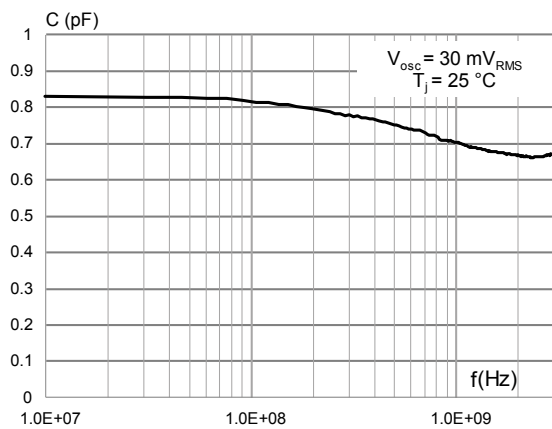


Figure 11. Line capacitance versus junction temperature

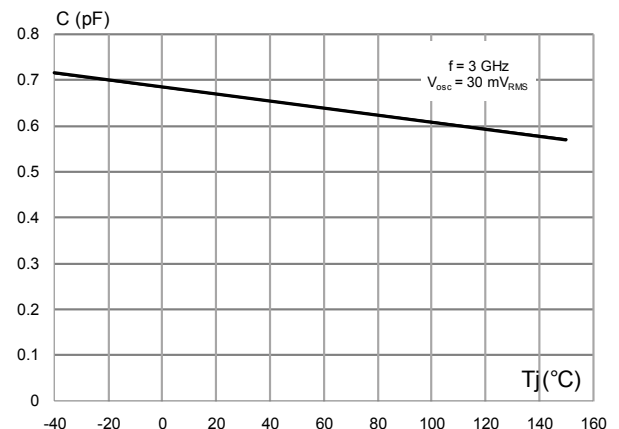


Figure 12. Line capacitance at a frequency of 3 GHz versus reverse voltage

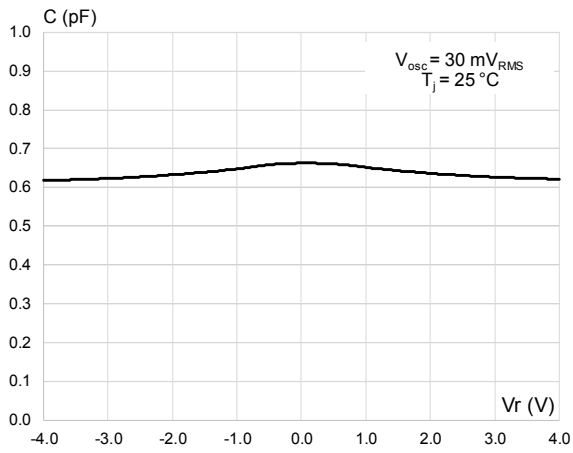
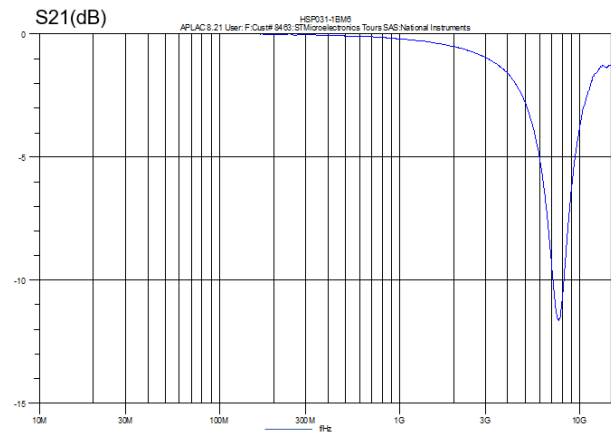


Figure 13. S21



2 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

2.1 QFN-6L package information

Figure 14. QFN-6L package outline

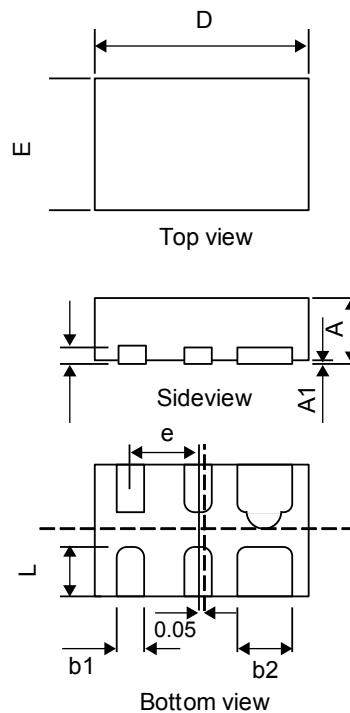
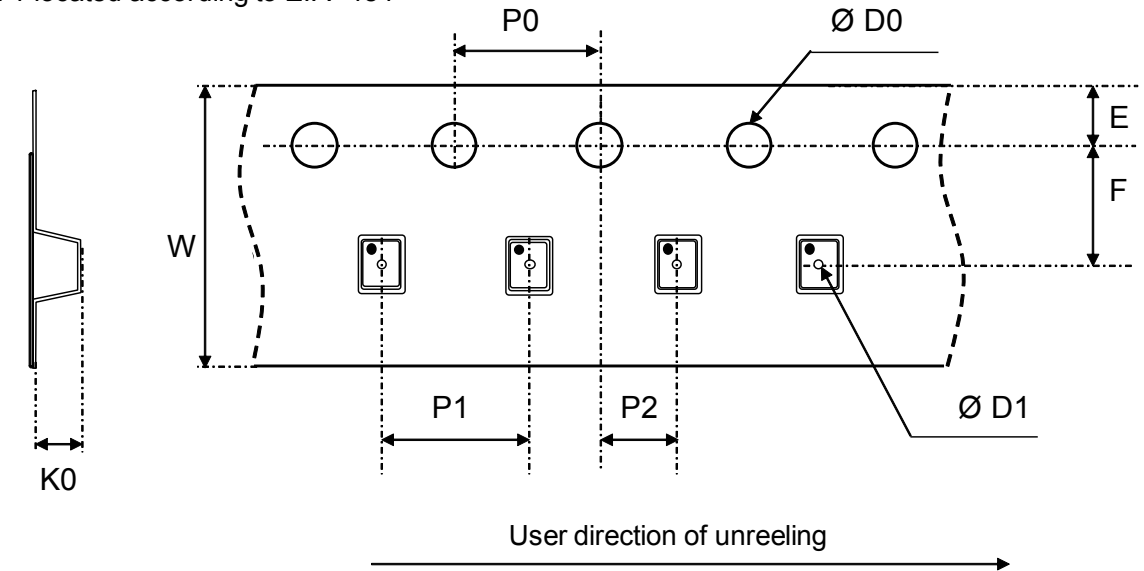


Table 3. QFN-6L mechanical data

Symbol	Dimensions (millimeters)		
	Min.	Typ.	Max.
A	0.45	0.50	0.55
A1	0.00		0.05
A3		0.127	
b1	0.15	0.20	0.25
b2	0.35	0.40	0.45
D	1.55	1.60	1.65
E	0.95	1.00	1.05
e		0.50	
L	0.28	0.38	0.48

Figure 15. Tape outline

Pin 1 located according to EIA-481



Note: Pocket dimensions are not on scale
Pocket shape may vary depending on package

Table 4. Tape dimensions values

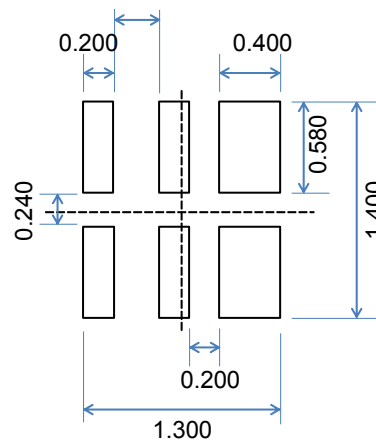
Ref.	Dimensions Millimeters		
	Min.	Typ.	Max.
D0	1.45	1.55	1.65
D1	0.50	0.60	0.70
F	3.45	3.50	3.55
E	1.65	1.75	1.85
K0	0.67	0.72	0.77
P0	3.9	4	4.1
P1	3.9	4	4.1
P2	1.95	2.00	2.05
W	7.9	8.0	8.2

3 Recommendation on PCB assembly

3.1 Footprint

SMD footprint design is recommended.

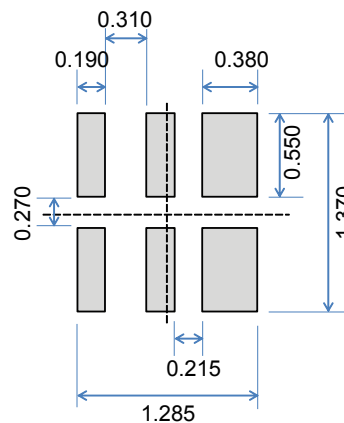
Figure 16. Footprint in mm



3.2 Stencil opening design

1. Reference design
 - a. Stencil opening thickness: 75 μm / 3 mils
 - b. Stencil aperture ratio: 90%

Figure 17. Recommended stencil window position in mm



3.3 Solder paste

1. Halide-free flux qualification ROL0 according to ANSI/J-STD-004.
2. "No clean" solder paste is recommended.
3. Offers a high tack force to resist component movement during high speed.
4. Solder paste with fine particles: powder particle size is 20-38 μm .

3.4 Placement

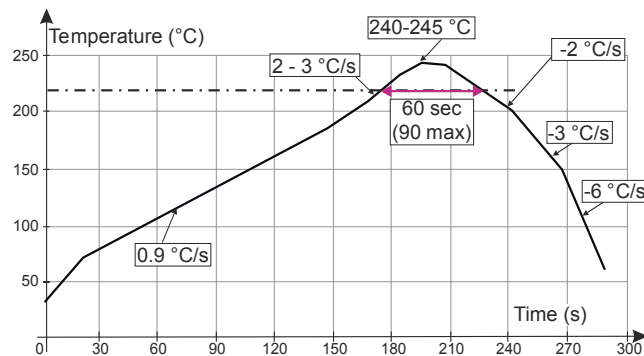
1. Manual positioning is not recommended.
2. It is recommended to use the lead recognition capabilities of the placement system, not the outline centering
3. Standard tolerance of ± 0.05 mm is recommended.
4. 3.5 N placement force is recommended. Too much placement force can lead to squeezed out solder paste and cause solder joints to short. Too low placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or badly centered packages.
5. To improve the package placement accuracy, a bottom side optical control should be performed with a high resolution tool.
6. For assembly, a perfect supporting of the PCB (all the more on flexible PCB) is recommended during solder paste printing, pick and place and reflow soldering by using optimized tools.

3.5 PCB design preference

1. To control the solder paste amount, the closed via is recommended instead of open vias.
2. The position of tracks and open vias in the solder area should be well balanced. A symmetrical layout is recommended, to avoid any tilt phenomena caused by asymmetrical solder paste due to solder flow away.

3.6 Reflow profile

Figure 18. ST ECOPACK[®] recommended soldering reflow profile for PCB mounting



Note: Minimize air convection currents in the reflow oven to avoid component movement.

Note: Maximum soldering profile corresponds to the latest IPC/JEDEC J-STD-020.

4 Ordering information

Figure 19. Ordering information scheme

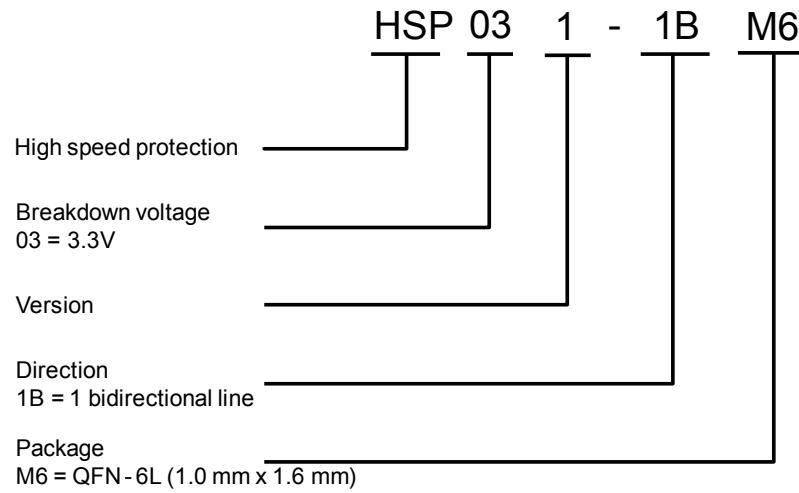


Table 5. Ordering information

Order code	Marking	Package	Weight	Base qty.	Delivery mode
HSP031-1BM6	HE ⁽¹⁾	QFN-6L	2.27 mg	3000	Tape and reel

1. The marking can be rotated by 90° to differentiate assembly location

Revision history

Table 6. Document revision history

Date	Version	Changes
25-May-2020	1	Initial release.

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