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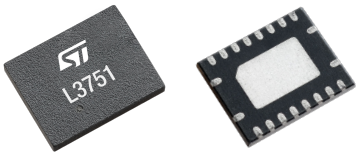
L3751

Datasheet

Wide 6 V to 75 V input voltage synchronous buck controller



Maturity status link
L3751

Features

- Wide 6 V to 75 V input voltage range
- Adjustable output voltage from 0.8 V to 60 V
- 100 kHz - 1 MHz switching frequency range
- 40 ns minimum on-time for extreme duty ratio
- Low dropout operation during line transient
- Adjustable soft-start or input voltage tracking
- Pulse skipping or forced PWM operation at light load
- Synchronization
- Adjustable precision enable
- Power Good open collector output validates V_{OUT}
- 7.5 V gate drivers for standard V_{TH} MOSFETs
- Constant current protection with hiccup mode
- Precision or lossless programmable current sensing
- Improved line transient response
- Input voltage undervoltage lockout
- Internal voltage monitoring
- Thermal protection
- Operating junction temperature range: -40 °C to 150 °C

Applications

- Telecom, networking and industrial applications
- Failsafe systems
- Unregulated 24 V and 48 V input voltage bus
- Conversion from high voltage battery to 12 V and 5 V rail

Description

The 6 V to 75 V wide input voltage range L3751 synchronous buck controller features extreme voltage conversion ratio over switching frequency range (100 kHz - 1 MHz) thanks to 40 ns minimum conduction time.

The diode emulation (DEM) implements pulse skipping mode that maximizes the efficiency at light-load giving controlled output voltage ripple. The forced PWM (FPWM) over the load range makes the switching frequency constant and minimizes the output voltage ripple.

The Power Good open collector output validates the regulated output voltage for monitoring and it is useful to implement output voltage sequencing for digital ICs during the power-up phase.

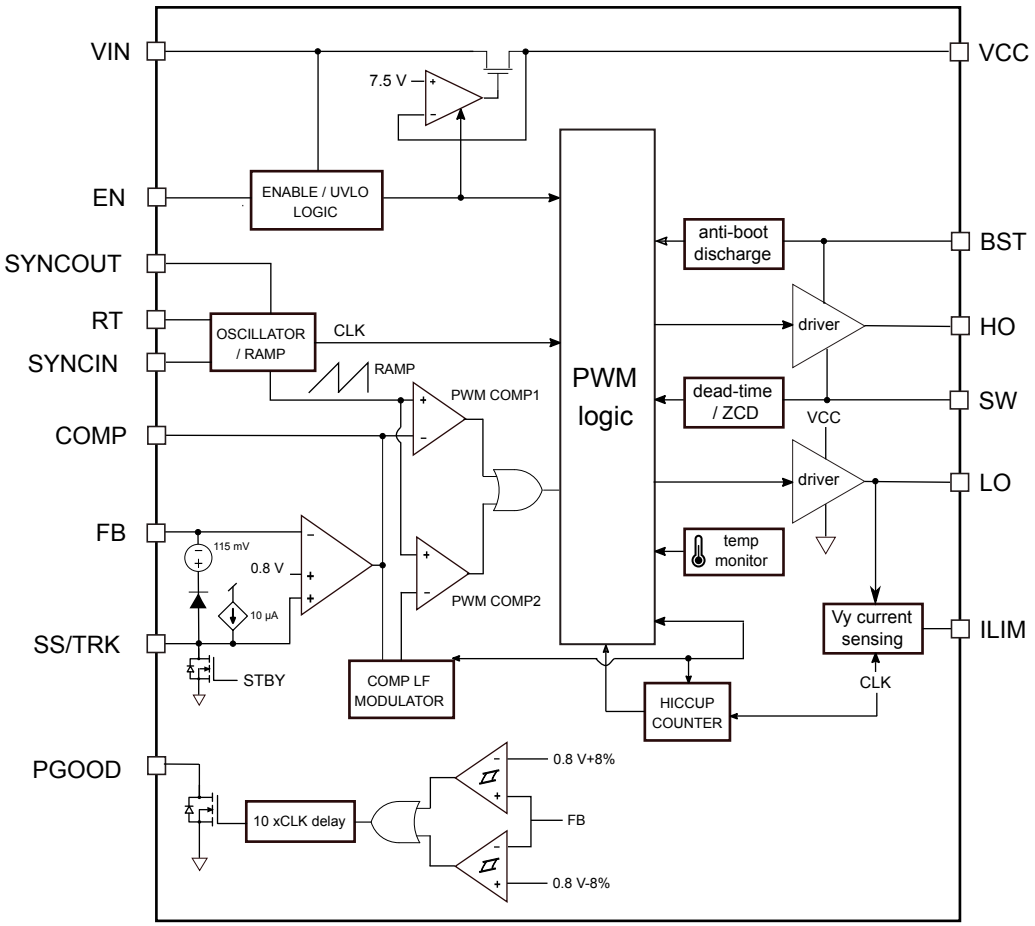
An embedded gate driver minimizes the number of external components and it is designed for standard V_{TH} MOSFET.

Embedded protections–output overcurrent, input voltage UVLO, internal voltage monitoring, thermal shutdown - feature controlled and safe operation for critical environments in telecom, networking and industrial applications.

The device is available in a QFN 20 leads 3.5 x 4.5 mm package with wettable flanks.

1 Diagram

Figure 1. **Simplified block diagram**



2 Pin configuration

Figure 2. **QFN pin connection (top view)**

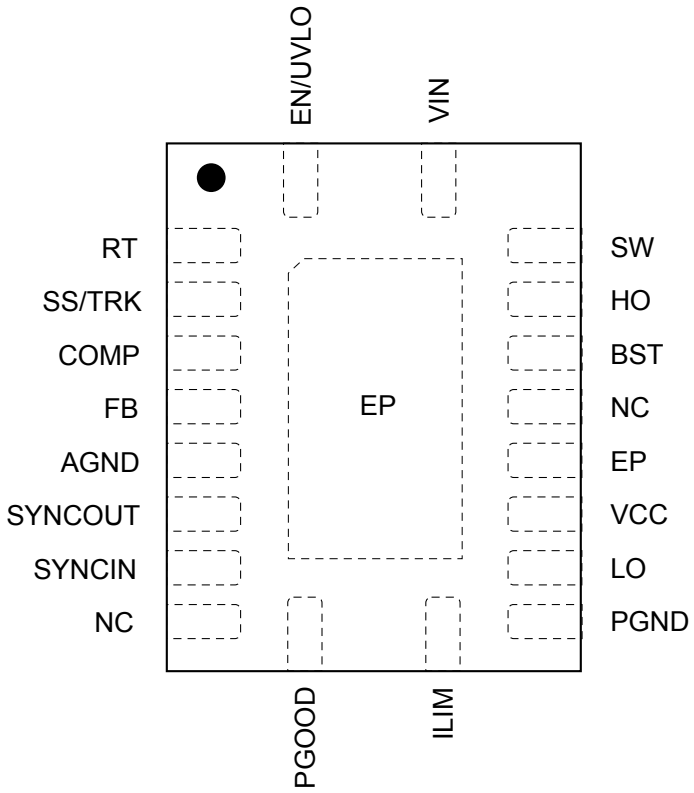


Table 1. **Pin description**

QFN pin	Name	Function
1	EN/UVLO	The central tap of a resistor divider connected to this pin helps to design the enable and undervoltage lockout thresholds referred to the input voltage. • $V_{EN/UVLO}$ < 0.4 typ.: the device is in shutdown mode • 0.4 V typ. < $V_{EN/UVLO}$ < 1.2 V typ.: device in standby - VCC regulator active - SS/TRK pin in low impedance • $V_{EN/UVLO}$ > 1.2 V typ.: SS/TRK pin released and the device ready to start - 10 µA current flows to the external resistor divider to design the enable hysteresis.
2	RT	A pull-down resistor to AGND programs the oscillator frequency (100 kHz – 1 MHz) and adjust the internal ramp for constant PWM gain.
3	SS/TRK	The pin circuitry features a current generator (10 µA typ.) to charge an external capacitor and so program the soft-start time, otherwise it implements voltage tracking if connected to an auxiliary voltage source. In soft-start phase, the SS/TRK voltage is the error amplifier reference and then the internal reference becomes active after the startup phase has ended. The pin is clamped 115 mV above the FB voltage for controlled recovery from an overcurrent event or clamped to ground during stand-by operation or internal fault.
4	COMP	Output of the internal error amplifier. Connect the compensation network between COMP and the FB.
5	FB	Inverting input of the internal error amplifier. Connect the compensation network between COMP and the FB.
6	AGND	Analog ground
7	SYNCOUT	Synchronization output implements 180° phase shifted referred to HO driving signal if the regulator is master. If synchronized to an external clock the signal is in phase with SYNCIN.

QFN pin	Name	Function
8	SYNCIN	Synchronization input and DEM (Diode Emulation) / FPWM (Forced PWM) selection. The device always implements DEM during soft-start to support pre-charged output capacitor at device startup. Low logic level selects DEM, high logic level or synchronization clock input enables the forced PWM. The device features a smooth transition DEM to FPWM thanks to embedded dedicated circuitry.
9	NC	Not internally connected
10	PGOOD	Power Good output collector is driven in low impedance when the FB voltage is out of the regulation window.
11	ILIM	Valley current limit adjust and current sense comparator input. A series resistor programs valley current threshold for accurate sensing across external sensing resistor or lossless sensing directly on the drain of the low-side MOSFET.
12	PGND	Power ground
13	LO	Low-side MOSFET gate drive output. Optional series resistor may be connected to adjust switching times for EMI compatibility.
14	VCC	Output of the internal 7.5 V linear regulator that powers the embedded voltage gate driver. Connect high quality mlcc capacitor (470 nF≤ CVCC ≤ 2 µF) to power ground. An external voltage source higher than internal regulator output can be connected (VEN/UVLO > 0.4 V) to increase MOSFET driving capability in terms of gate driver VTH overdriving or output current capability required at high switching frequency.
15	EP	Pin internally connected to exposed pad and electrically isolated. Connect to PGND plane.
16	NC	Not internally connected
17	BST	Bootstrap supply for the high-side gate driver. Connect an external diode between VCC and BOOT and capacitor (100 nF typ.) between BOOT and SW pins.
18	HO	High-side MOSFET gate drive output. Optional series resistor may be connected to adjust switching times for EMI compatibility.
19	SW	Switching node to be connected to the source of the HS MOSFET, drain of the LS MOSFET and bootstrap capacitor terminal.
20	VIN	Voltage input for the internal circuitry and VCC linear regulator.
E.P.	EP	Exposed Pad. Connect to PGND plane.

3 Typical application circuit

Figure 3. **Typical application**

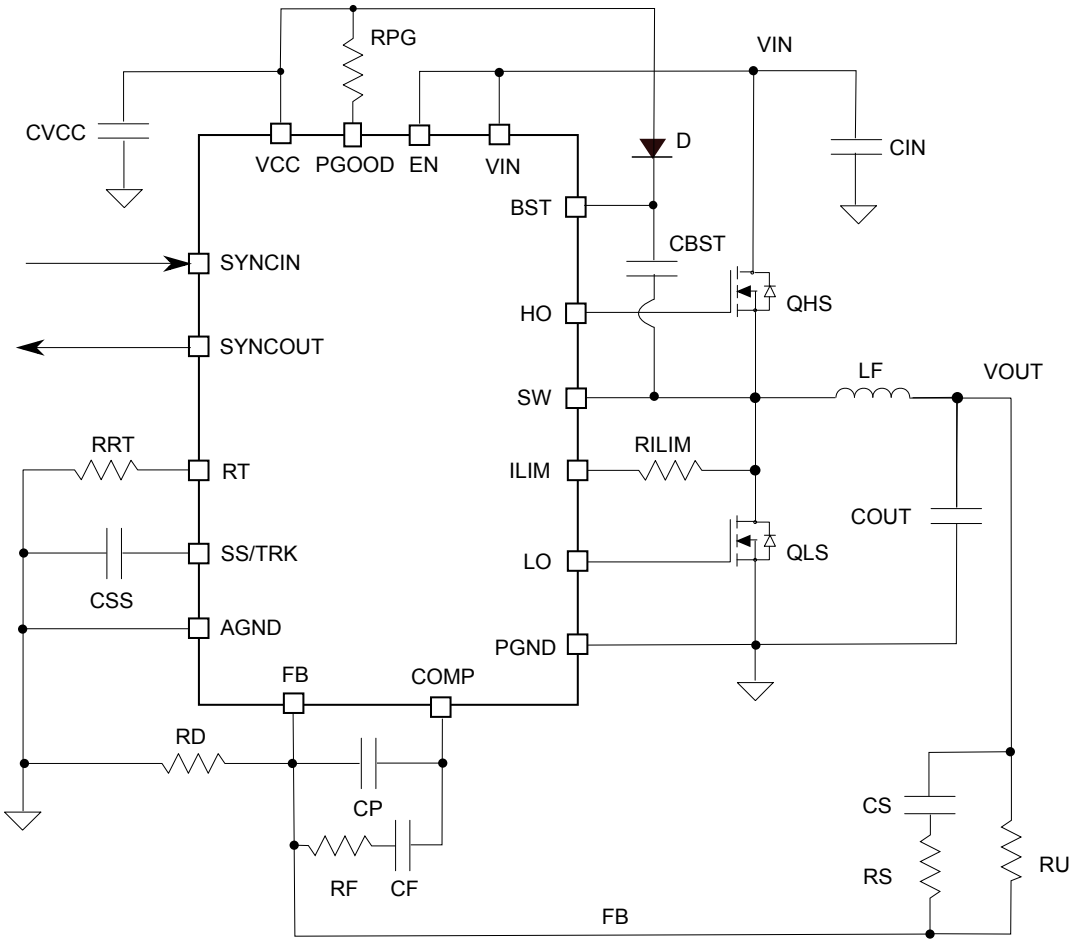


Table 2. Schematic application components description

Symbol	Description
C_{IN}	Input capacitor
C_{BST}	Bootstrap capacitor
C_{OUT}	Output capacitor
C_C	Compensation capacitor
C_P	Compensation capacitor
R_F	Compensation resistor
C_S	Feedforward capacitor
R_S	Feedforward resistor
R_U	High-side feedback resistor
R_D	Low-side feedback resistor
C_{SS}	Soft-start capacitor
R_{RT}	Frequency adjust resistor
R_{LIM}	Current limit resistor
L_F	Buck inductor
Q_1	High-side MOSFET
Q_2	Low-side MOSFET
D	Bootstrap Diode

4 Maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Min.	Max.	Unit
V_{IN}	Input voltage	-0.3	100	V
SW	Switching node	-1	100	V
	Switching node (20 ns transient)	-5	100	V
ILIM	Current limit pin	-1	100	V
EN/UVLO	Enable pin and undervoltage lockout	-0.3	100	V
VCC	VCC pin	-0.3	13	V
FB, COMP, SS/TRK, RT	Analog pins	-0.3	4.6	V
SYNCIN	Synchronization input	-0.3	8	V
BST	Bootstrap pin	-0.3	100	V
BST to SW	Bootstrap to SW voltage difference	-0.3	13	V
LO	20 ns transient	-3		V
PGOOD	Power Good	-0.3	14	V
T_J	Operating junction temperature	-40	150	°C
T_{STG}	Storage temperature range	-40	150	°C

Note: Stressing the device above the absolute maximum rating may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 4. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Thermal resistance junction-ambient	30	°C/W

1. *FR4 board with using 1 sq−in pad, 1 oz Cu.*

Table 5. ESD performance

Symbol	Parameter	Test conditions	Value	Unit
ESD	ESD protection voltage	HBM	2	kV
		CDM	500	V

Table 6. Recommended operating conditions

Symbol	Parameter	Value	Unit
V_{IN}	Input voltage	6 to 75	V
EN/UVLO	Analog pins	0 to V_{IN}	V
PGOOD	Power Good	0 to 13	V
$I_{SYNCOUT}$	SYNCOUT pin sink and source currents	-1 to 1	mA
I_{PGOOD}	PGOOD sink current	2	mA
T_{OP}	Operating junction temperature range	- 40 to 125	°C

5 Electrical characteristics

$V_{EN/UVLO}$ = 1.5 V, V_{IN} = 48 V; R_{RT} = 24.9 kΩ; typical values are at T_J = 25 °C; minimum and maximum values are at -40 °C ≤ T_J ≤ 125 °C, unless otherwise specified.

Table 7. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Input Supply						
V_{IN}	Operating input voltage		6		75	V
I_Q	Quiescent current	Not switching, $V_{SS/TRK}$ = 0 V		1.8	2.3	mA
		$V_{EN/UVLO}$ = 1 V		1.75	2.25	mA
I_{Q-SDN}	Shutdown input current	$V_{EN/UVLO}$ = 0 V, V_{VCC} < 1 V		8.5	21	µA
VCC regulator						
V_{VCC}	Internal regulator voltage	$V_{SS/TRK}$ = 0 V, 9 V ≤ V_{VIN} ≤ 75 V, I_{VCC} = 10 mA	7.3	7.5	7.7	V
$V_{VCC-LDO}$	VIN to VCC dropout voltage	V_{VIN} = 6 V, $V_{SS/TRK}$ = 0 V, I_{VCC} = 20 mA; T_J = 25 °C		0.25	0.63	V
I_{SC-LDO}	VCC short-circuit current	$V_{SS/TRK}$ = 0 V, V_{VCC} = 0 V; T_J = 25 °C	40	50	70	mA
V_{VCC-UV}	VCC undervoltage threshold	V_{VCC} rising	4.8	4.93	5.2	V
$V_{VCC-UVH}$	VCC undervoltage hysteresis	V_{VCC} falling		0.26		V
$V_{VCC-EXT}$ (1)	Minimun external bias supply voltage	Voltage required to disable V_{CC} regulator	8			V
I_{VCC}	External V_{CC} input current, Not switching	$V_{SS/TRK}$ = 0, V_{VCC} = 13 V			2.5	mA
Enable and Input UVLO						
V_{SDN}	Shutdown to stand-by threshold	$V_{EN/UVLO}$ rising		0.42		V
$V_{SDN-HYS}$	Shutdown threshold hysteresis	EN/UVLO falling		50		mV
V_{EN}	Standby to operating threshold	$V_{EN/UVLO}$ rising	1.16	1.2	1.25	V
I_{EN-HYS}	Standby to operating hysteresis current	$V_{EN/UVLO}$ = 1.5 V	8	10	11	µA
Error Amplifier						
V_{REF}	FB reference voltage	FB connected to COMP	792	800	808	mV
$I_{FB-BIAS}$	FB input bias current	V_{FB} = 0.8 V; T_J = 25 °C	-0.1		0.1	µA
$V_{COMP-OH}$	COMP output high voltage	V_{FB} = 0 V, COMP sourcing 1 mA		3.3		V
$V_{COMP-OL}$	COMP output low voltage	COMP sinking 1 mA; T_J = 25 °C			0.3	V
AVOL (1)	DC gain			94		dB
GBW (1)	Unity gain bandwidth			6.5		MHz
Soft-Start and Voltage Tracking						
I_{SS}	SS/TRK capacitor charging current	$V_{SS/TRK}$ = 0 V	7.5	10	12	µA
R_{SS}	SS/TRK discharge FET resistance	$V_{EN/UVLO}$ = 1 V, $V_{SS/TRK}$ = 0.1 V		12		Ω
V_{SS-FB}	SS/TRK to FB offset	T_J = 25 °C	-15		15	mV
$V_{SS-CLAMP}$	SS/TRK clamp voltage	$V_{SS/TRK}$ – V_{FB}, V_{FB} = 0.8 V		115		mV

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
		Power Good				
PG_{UTH}	FB upper threshold for PGOOD high to low	% of V_{REF}, V_{FB} rising	106	108	110	%
PG_{LTH}	FB lower threshold for PGOOD high to low	% of V_{REF}, V_{FB} falling	90	92	94	%
PG_{HYS_U}	PGOOD upper threshold hysteresis	% of V_{REF}		3		%
PG_{HYS_L}	PGOOD lower threshold hysteresis	% of V_{REF}		2		%
$T_{PG-RISE}$ (1)	PGOOD rising filter	FB to PGOOD rising edge		$10/F_{SW}$		µs
$T_{PG-FALL}$ (1)	PGOOD falling filter	FB to PGOOD falling edge		$10/F_{SW}$		µs
V_{PG-OL}	PGOOD low state output voltage	V_{FB} = 0.9 V, I_{PGOOD} = 2 mA			150	mV
I_{PG-OH}	PGOOD high state leakage current	V_{FB} = 0.8 V, V_{PGOOD} = 13 V; T_J = 25 °C			100	nA
		Oscillator				
F_{SW}	Oscillator frequency	R_{RT} = 100 kΩ		115		kHz
		R_{RT} = 25 kΩ	380	400	420	
		R_{RT} = 11 kΩ		800		
		Synchronization input / output				
F_{SYNC}	SYNCIN external clock frequency (> 100 kHz < 1 MHz)	% of nominal frequency set by R_{RT}	-20		+50	%
$V_{SYNC-IH}$	Minimum SYNCIN input logic high		2			V
$V_{SYNC-IL}$	Maximum SYNCIN input logic low				0.8	V
R_{SYNCIN}	SYNCIN input resistance	V_{SYNCIN} = 3 V		20		kΩ
$T_{SYNCI-PW}$	SYNCIN input minimum pulse-width	Minimum high state or low state duration; T_J = 25 °C	50			ns
$V_{SYNCO-OH}$	SYNCOUT high state output voltage	$I_{SYNCOUT}$ = –1 mA (sourcing)	3			V
$V_{SYNCO-OL}$	SYNCOUT low state output voltage	$I_{SYNCOUT}$ = 1 mA (sinking)			0.4	V
$T_{SYNCOUT}$	Delay from HO rising to SYNCOUT leading edge	V_{SYNCIN} = 0 V, $T_S = 1/F_{SW}$, F_{SW} set by R_{RT}		$T_S/2$-140		ns
T_{SYNCIN}	Delay from SYNCIN leading edge to HO rising	50% to 50%, R_T = 11 kΩ, V_{IN} = 75 V		190		ns
		Bootstrap and BST UVLO				
I_{Q-BST}	BST to SW quiescent current, not switching	$V_{SS/TRK}$ = 0 V, V_{SW} = 48 V, V_{BST} = 54 V		300	500	µA
V_{BST-UV}	BST to SW undervoltage detection	$V_{BST} – V_{SW}$ falling		3.4		V
$V_{BST-HYS}$	BST to SW undervoltage hysteresis	$V_{BST} – V_{SW}$ rising		0.42		V
		PWM Control				
$T_{ON(MIN)}$	Minimum controllable on-time	$V_{BST} – V_{SW}$ = 7 V, HO 50% to 50%		40	60	ns
$T_{OFF(MIN)}$	Minimum off-time	$V_{BST} – V_{SW}$ = 7 V, HO 50% to 50%		180	250	ns
DC_{MAX}	Maximum duty cycle	F_{SW} = 100 kHz, 6 V ≤ V_{VIN} ≤ 60 V	98	99		%
		F_{SW} = 400 kHz, 6 V ≤ V_{VIN} ≤ 60 V	90	94		%
$V_{RAMP(min)}$	Ramp valley voltage (COMP at 0% duty cycle)			300		mV
k_{FF}	PWM feedforward gain (V_{IN} / V_{RAMP})	6 V ≤ V_{VIN} ≤ 75 V		30		V/V

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
		PWM Control				
I_{RS}	ILIM source current, R_{SENSE}	25 °C	90	100	110	µA
		-40 °C to 125 °C	80	100	110	
I_{RDSON}	I_{LIM} source current, $R_{DS(on)}$ mode	SW voltage detected at I_{LIM}, T_J = 25 °C	180	200	220	µA
I_{RSTC} (1)	I_{LIM} current temperature compensation	R_{DS-ON} mode		4500		ppm/°C
		R_{SENSE} mode		0		
$V_{ILIM-TH}$	ILIM comparator threshold at ILIM		-9	-2	4.5	mV
		Short-circuit protection (SCP)				
$V_{CLAMP-OS}$	Clamp offset voltage – no current limiting	CLAMP to COMP steady-state offset voltage; -40 ≤ T_J ≤ +125 °C		0.2 + V_{VIN}/150		V
$V_{CLAMP-MIN}$	Minimum clamp voltage	CLAMP voltage with continuous current limiting; -40 ≤ T_J ≤ +125 °C		0.3 + V_{VIN}/300		V
		Short-circuit protection (SCP)				
$C_{HICC-DEL}$	Hiccup mode activation delay	Clock cycles with current limiting before hiccup off-time activated		128		cycles
C_{HICCUP}	Hiccup mode off-time after activation	Clock cycles with no switching followed by SS/TRK release		8192		cycles
		Diode Emulation				
V_{ZCD-SS}	Zero-cross detect (ZCD) soft-start ramp	ZCD threshold measured at SW pin 50 clock cycles after first HO pulse		0		mV
$V_{ZCD-DIS}$	Zero-cross detect disable threshold (CCM)	ZCD threshold measured at SW pin 1000 clock cycles after first HO pulse		200		mV
V_{DEM-TH}	Diode emulation zero-cross threshold	Measured at SW with V_{SW} rising	-7	-2	4	mV
		Gate Drivers				
R_{HO-UP}	HO high-state resistance, HO to BST	V_{BST} – V_{SW} = 7 V, I_{HO} = –100 mA		1.5		Ω
$R_{HO-DOWN}$	$R_{HO-DOWN}$ HO low-state resistance, HO to SW	V_{BST} – V_{SW} = 7 V, I_{HO} = 100 mA		0.9		Ω
R_{LO-UP}	LO high-state resistance, LO to VCC	V_{BST} – V_{SW} = 7 V, I_{LO} = –100 mA		1.5		Ω
$R_{LO-DOWN}$	LO low-state resistance, LO to PGND	V_{BST} – V_{SW} = 7 V, I_{LO} = 100 mA		0.9		Ω
I_{HOH}, I_{LOH} (1)	HO, LO source current	V_{BST} – V_{SW} = 7 V, HO = SW, LO = AGND		2.3		A
I_{HOL}, I_{LOL} (1)	HO, LO sink current	V_{BST} – V_{SW} = 7 V, HO = BST, LO = VCC		3.5		A
T_{HO-TR}, T_{LO-TR}	HO, LO rise times	V_{BST} – V_{SW} = 7 V, C_{LOAD} = 1 nF, 20% to 80%		7		ns
T_{HO-TF} T_{LO-TF}	HO, LO fall times	V_{BST} – V_{SW} = 7 V, C_{LOAD} = 1 nF, 80% to 20%		4		ns
T_{HO-DT} (1)	HO turn-on deadtime	V_{BST} – V_{SW} = 7 V, LO off to HO on, 50% to 50%		14		ns
T_{LO-DT} (1)	LO turn-on deadtime	V_{BST} – V_{SW} = 7 V, HO off to LO on, 50% to 50%		14		ns
		Thermal protection				
T_{SD}	Thermal shutdown threshold	T_J rising		175		°C

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
T_{SD-HYS}	Thermal shutdown hysteresis			20		°C

1. *Specified by design – not tested in production.*

Note: All minimum and maximum limits are specified by correlating the electrical characteristics to process and temperature variations and applying statistical process control.

6 Functional description

The L3751 device is a native buck controller based on constant frequency voltage mode architecture.

The output voltage VOUT, sensed by the feedback pin (FB), is compared to an internal reference (0.8 V) providing an error signal on the COMP pin. The comparison between the COMP voltage level and the internal programmable frequency sawtooth ramp, controls the activation time of the external power switches.

The main internal blocks are shown in the block diagram in Figure 1 and can be summarized as follows:

- The voltage regulator to supply the internal circuitry and provide a fixed internal reference. This block also implements a voltage monitor circuitry (UVLO) that checks the input and internal voltages
- The embedded external N-channel MOSFET drivers and the bootstrap capacitor circuitry to supply the high-side driver
- The embedded circuitry that generates the sawtooth ramp to modulate the duty cycle based on the internal programmable oscillator or the input synchronization signal. The input voltage feedforward is implemented for improved line transient response
- The voltage mode error amplifier
- The PWM comparators and the relative analog and digital circuitry necessary to drive the internal MOSFET drivers
- The soft-start circuitry to limit inrush current during the start-up phase and the reference clamper
- The adjustable senseless or precise valley current limit sensing block and hiccup circuitry to handle overload and short-circuit conditions
- The thermal shutdown circuitry to prevent thermal runaway
- The output voltage monitor circuitry which releases the PGOOD signal if the sensed output voltage is above 87% of the target value.

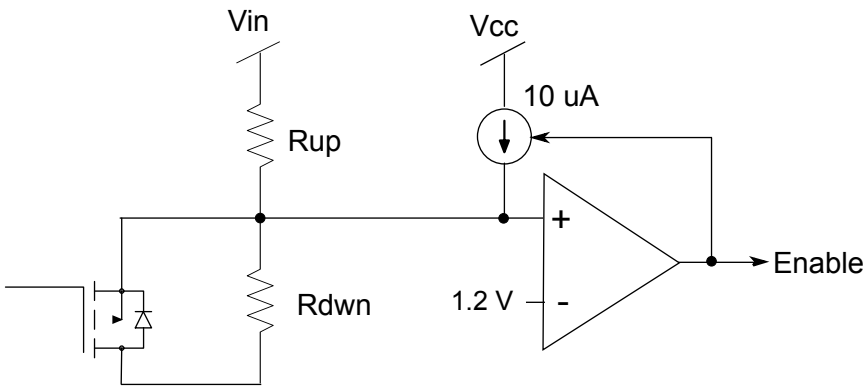
6.1 Precision enable

The EN/UVLO pin multiplexes the inherent functions as described below:

- VEN / UVLO < 0.4 typ.: the device is in shutdown mode
- 0.4 V typ. < VEN / UVLO < 1.2 V typ.: device in standby having the VCC regulator active but the device operation inhibited and SS / TRK pin in low impedance
- VEN / UVLO > 1.2 V typ.: SS / TRK pin released and the device starts operating. An internal 10 µA current flows to the external resistor divider to design the enable to UVLO hysteresis.

The central tap of a resistor divider connected to the EN/UVLO pin from VIN designs the enable and undervoltage lockout thresholds referred to the input voltage as shown in the figure below.

Figure 4. EN / UVLO resistor divider



The value of the resistors composing the divider can be calculated as follows:

$$R_{UP} = \frac{VIN_{ON} - VIN_{OFF}}{10\mu A} \qquad R_{DWN} = R_{UP} \cdot \frac{1.2}{VIN_{ON} - 1.2} \tag{1}$$

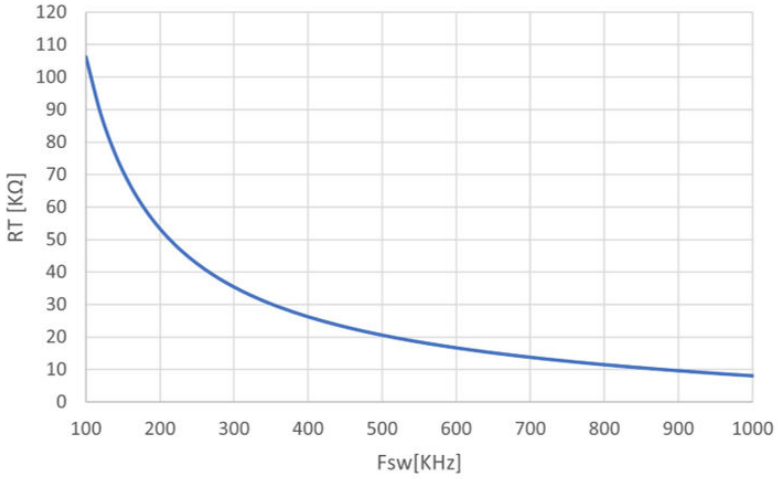
Where VIN_{ON} and VIN_{OFF} represent the desired turn-on and turn-off thresholds.

6.2 Oscillator and synchronization

The programmable internal oscillator frequency depends on the external resistor connected between the RRT pin and ground according to the following formula:

$$R_{RT}[k\Omega] = \frac{10500}{f_{SW}[kH]} + 0.004 \times (400 - fSW[kHz]) \tag{2}$$

Figure 5. R_{RT} resistor value for f_{SW} programming



The switching frequency can be alternatively adjusted, synchronizing the device to the external clock signal fed to the SYNCIN pin that satisfies the following requirements:

- Clock frequency range: 100 kHz to 1 MHz
- Clock frequency: -20% to +50% of the oscillator frequency programmed by R_{RT}
- Clock maximum amplitude: 13 V
- Clock minimum pulse: 50 ns

The device works in phase with the synchronization signal.

The L3751 features the internal sawtooth ramp feedforward for constant PWM gain over input voltage and programmable switching frequency range:

$$G_{PWM} = \frac{V_{OUT}}{V_{COMP}} = \frac{V_{IN}}{\Delta V_{RAMP}} = \frac{V_{IN}}{K \cdot V_{IN}} = \frac{1}{K} \tag{3}$$

Where K = 30.

Figure 6. **Internal sawtooth ramp feedforward - voltage feed forward**

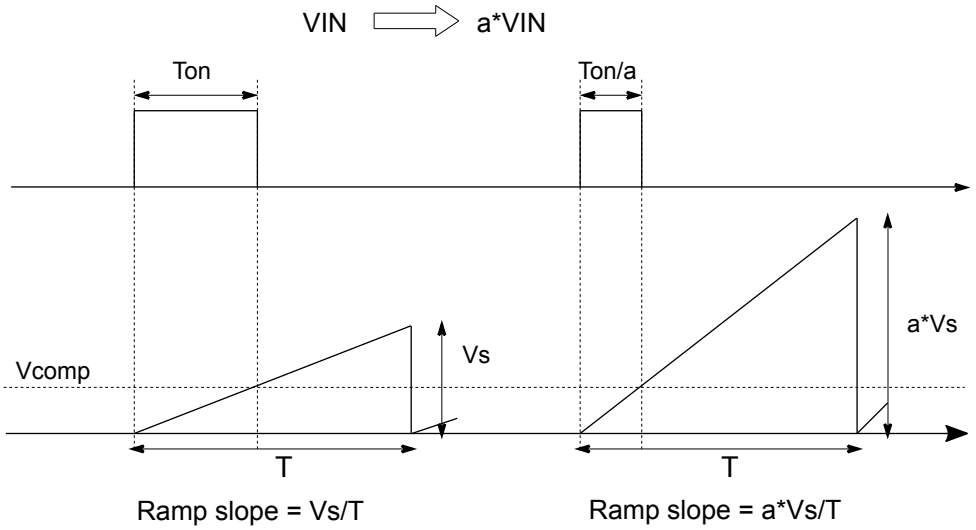
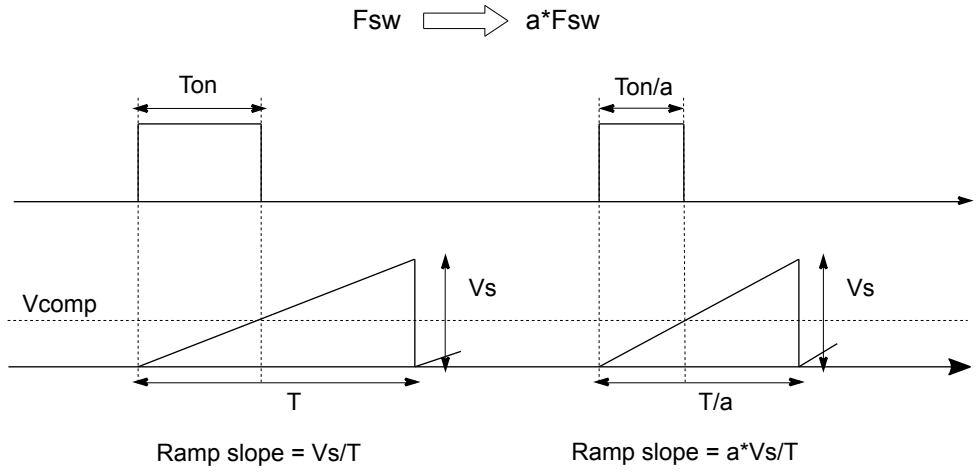


Figure 7. **Internal sawtooth ramp feedforward - Fsw adjusted by external resistor**



The device generates a synchronization signal available at the SYNCOUT pin that has 180° phase shift referred to the rising edge of the internal oscillator. Synchronized operation is easily accomplished connecting the SYNCOUT of the master to the SINCIN of the slave device to reduce the RMS current of the input filter and increase the EMI performance.

6.3 Soft-start

The soft-start (SS) feature minimizes the inrush current surge, decreases the stress of the power components during the power-up phase and makes the output voltage increase monotonically.

The device is inhibited as long as the EN/UVLO pin voltage is lower than the 0.4 V typ.

As soon as the EN/UVLO pin voltage exceeds the 1.2 V typ. rising threshold the soft-start phase takes place; an internal 10 µA typ. current source charges the external soft-start capacitor to ramp the SS/TRK pin voltage, clamping the internal error amplifier reference voltage. When the SS/TRK voltage exceeds the 0.8 V threshold the internal EA reference drives the non-inverting input so the SS is ended.

Figure 8. **Soft-start block diagram**

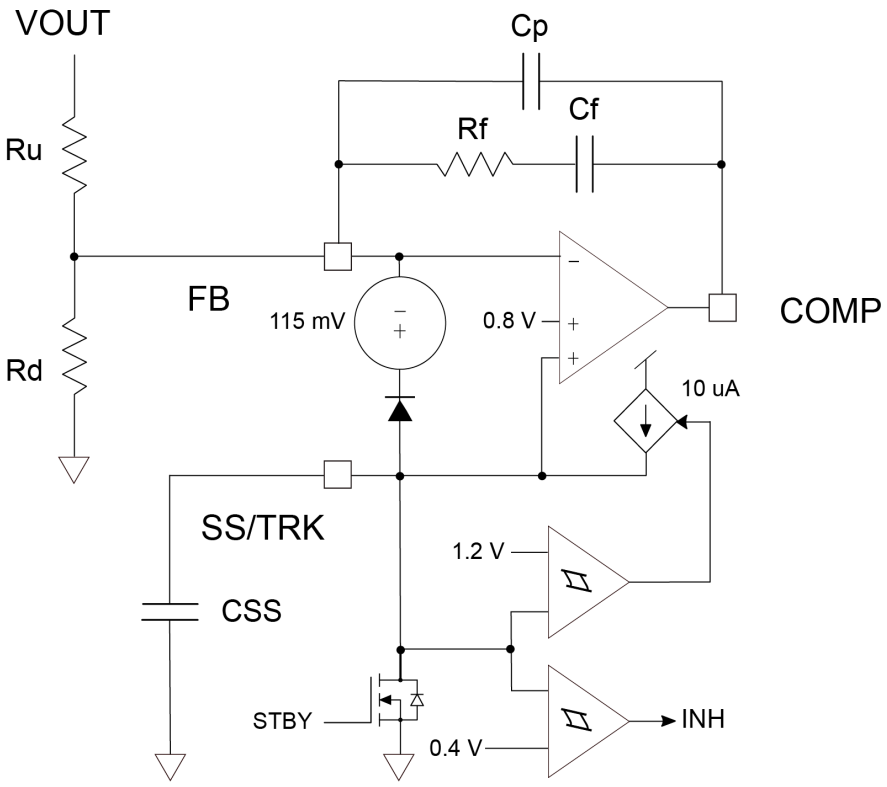


Figure 9. **Soft-start phase**

In the same way the device is able to track an external voltage source driving the SS/TRK pin in excess of the internal 10 µA typ current capability, like a simple voltage divider, to implement radiometric startup for multiple power rails suitable for digital ICs.

Figure 10. **Schematic to implement input voltage tracking**

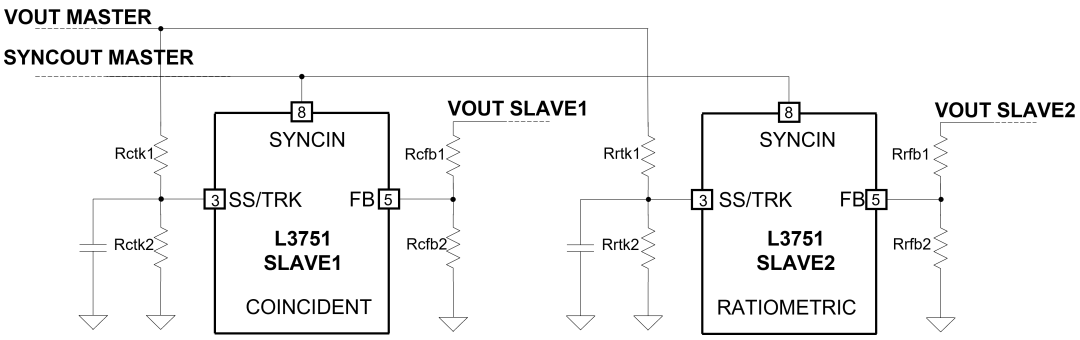
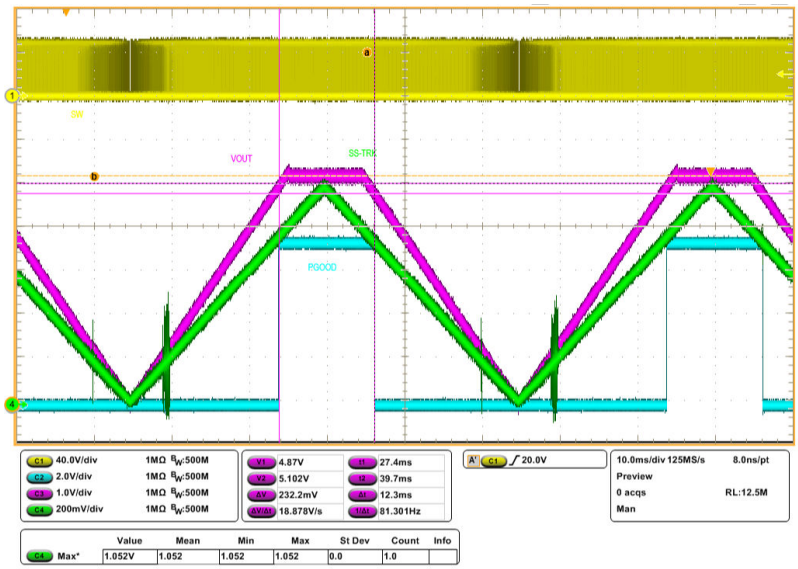
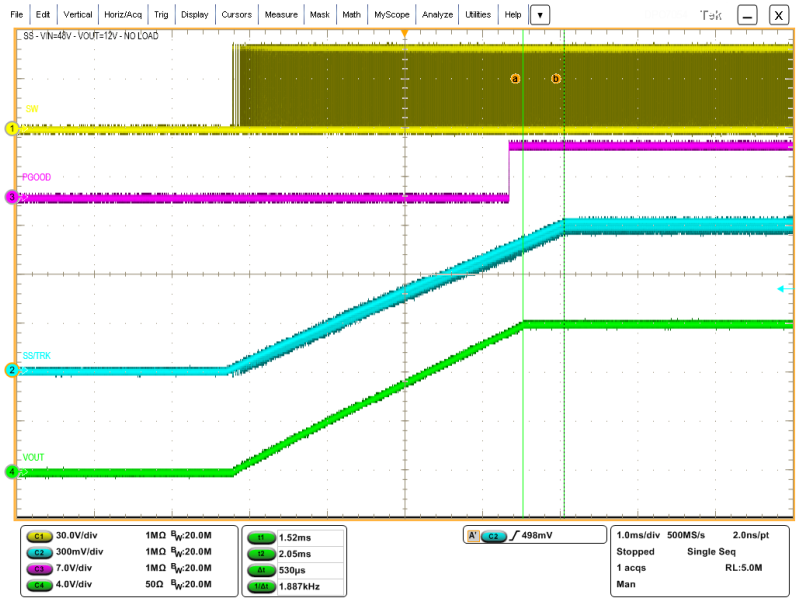


Figure 11. **Input voltage tracking**



After startup, the SS/TRK voltage is dynamically clamped 115 mV above the FB pin voltage in order to implement a partial soft-start, depending on the actual FB voltage, to recover from an abrupt load removal in overcurrent event.

Figure 12. **SS/TRK clampler operation**



6.4 Error amplifier

The error amplifier (EA) provides the error signal to be compared with the sawtooth to perform the pulse width modulation. Its non-inverting input is internally connected to a 0.8 V voltage reference, while its inverting input (FB) and output (COMP) are externally available for feedback and frequency compensation. In this device, the error amplifier is a voltage mode operational amplifier so with high DC gain and low output impedance.

The uncompensated error amplifier characteristics are the following:

Table 8. **Error amplifier characteristic**

Characteristic	Value
Non-inverting input voltage reference voltage	800 mV
Low frequency gain (A0)	95 dB
GBWP	6.5 MHz
Output voltage swing	0.3 to 3.3 V
Source / sink current capability	20 / 45 mA

In continuous conduction working mode (CCM), the transfer function of the power section has two poles due to the LC filter and one zero due to the ESR of the output capacitor. Different topologies of compensation networks can be used depending on the ESR value of the output capacitor.

If the zero introduced by the output capacitor helps to compensate the double pole of the LC filter, a type II compensation network can be used. Otherwise, a type III compensation network must be used (see Section 7 Closing the loop for details on the compensation network design).

Anyway, the methodology to compensate the loop is to introduce zeros to obtain a safe phase margin.

6.5 Embedded gate driver supply

The embedded gate driver power supply is the 7.5 V typ. LDO regulator output available on the VCC pin for the external compensation. Connect an mlcc capacitor value between 470 nF and 2.2 µF for proper operation.

The typical regulator dropout voltage is 250 mV @ V_{IN} = 6 V, I_{VCC} = 20 mA so the VCC voltage may drop at input voltage lower than 7.75 V. Be aware that the VCC drop at low input voltage may increase “not logic level MOSFET” R_{DSON}, affecting nominal programmed OCP threshold and increasing switching, conduction losses. For operation compatible with low input voltage, select “logic level MOSFET” with guaranteed maximum V_{TH} = 4.5 V.

The VCC regulator provides the gate current for direct low-side and floating high-side driving, through the bootstrap capacitor charge refresh. Make sure to select external MOSFETs in order that the total driving current consumption is smaller than VCC regulator minimum output current capability at the programmed switching frequency:

$$I_{DRV} = (Q_{G\ HS} + Q_{G\ LS}) \cdot fsw \leq I_{VCC\ MIN} = 40mA \quad (4)$$

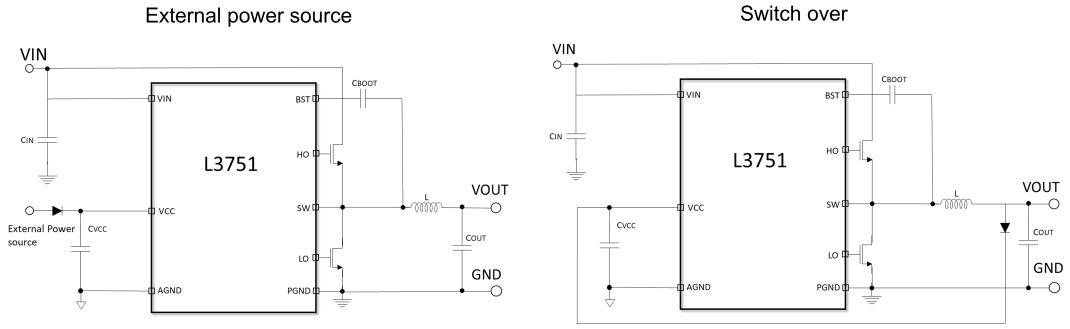
The internal LDO is turned off if an external voltage source drives the VCC higher than regulated LDO.

This function is useful to decrease the power dissipation of internal LDO and increase light load efficiency of the conversion. A higher VCC voltage also means a higher driving voltage for better Rdson and efficiency gain at high load.

Typically, the VCC can be upgrade by connecting, with an external diode, to an External Power Supply or directly to Vout if it is between 8 V and 13 V.

The external power supply at VCC pin must be provided/removed when Vin is present on L3751 pin.

Figure 13. VCC power circuite

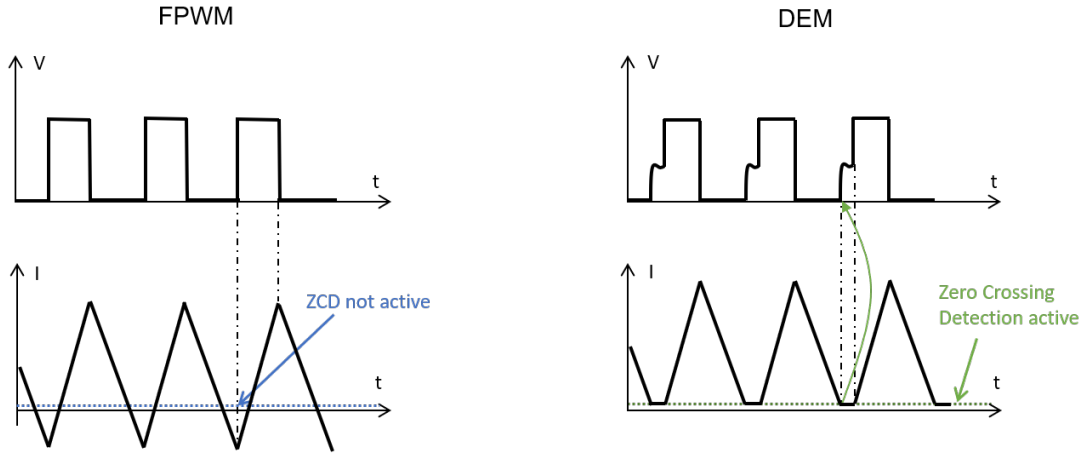


6.6 Light load operation

The device always implements diode emulation, so-called “DEM”, during soft-start to support pre-charged output capacitor at device startup.

The state of the SYNCIN pin at power-up determines the light load operation: low logic level selects DEM, high logic level or detected synchronization clock signal enables the forced PWM mode, so-called “FPWM”. In detail, the DEM to FPWM transition is implemented smoothly ramping the zero current detecting threshold (ZCD) from 0 V to 200 mV in 1000 clock cycles starting from the first PWM pulse from the loop.

Figure 14. DEM vs. FPWM management in light load condition



The DEM mode operates in DCM and pulse skipping at light load, maximizing the efficiency in these application conditions minimizing the conversion losses with controlled output voltage ripple.

The forced PWM (FPWM) over the load range makes the switching frequency constant and minimizes the output voltage ripple, suggested for low noise application like sensors or analog circuitry supply.

Figure 15. **DEM to FPWM smooth transition in 1000 clks at powerup**

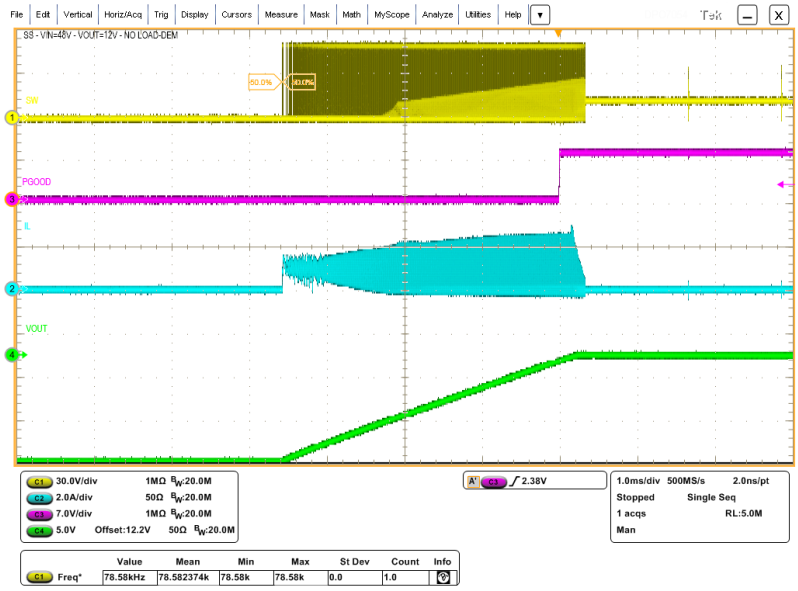


Figure 16. **Efficiency typ. @ 240 KHz, V_{OUT} = 5 V**

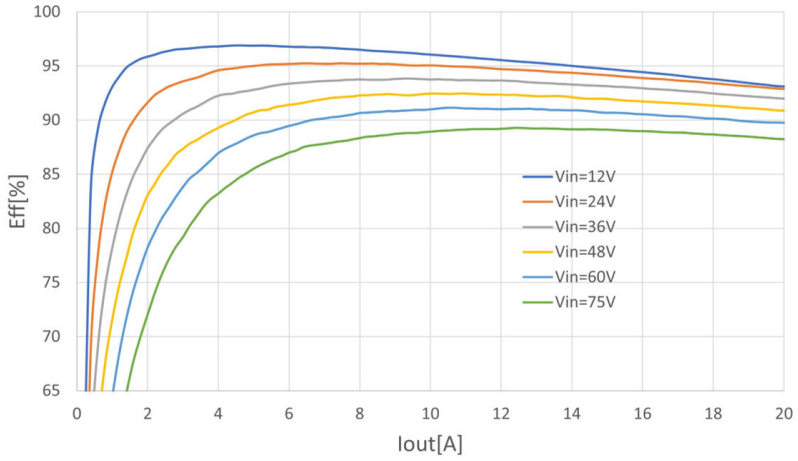


Figure 17. **Efficiency typ. @ 240 KHz, V_{OUT} = 12 V**

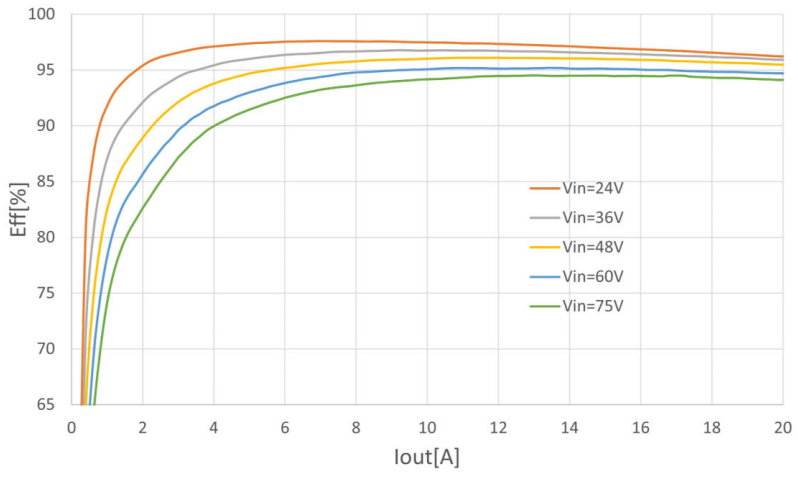


Figure 18. **Efficiency typ. @ 240 KHz DEM vs. FPWM**

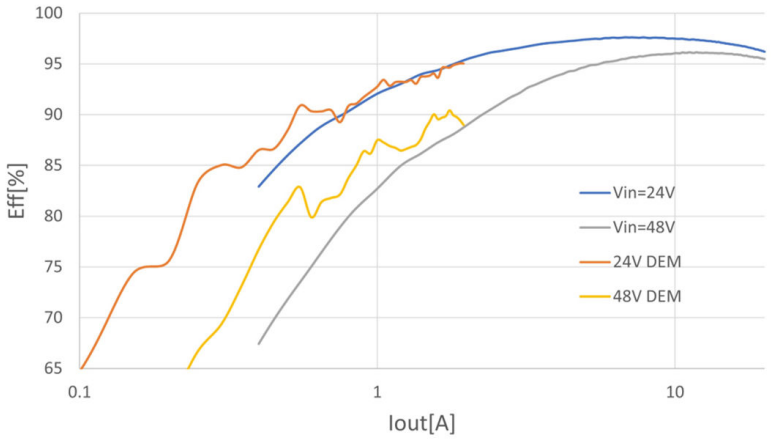
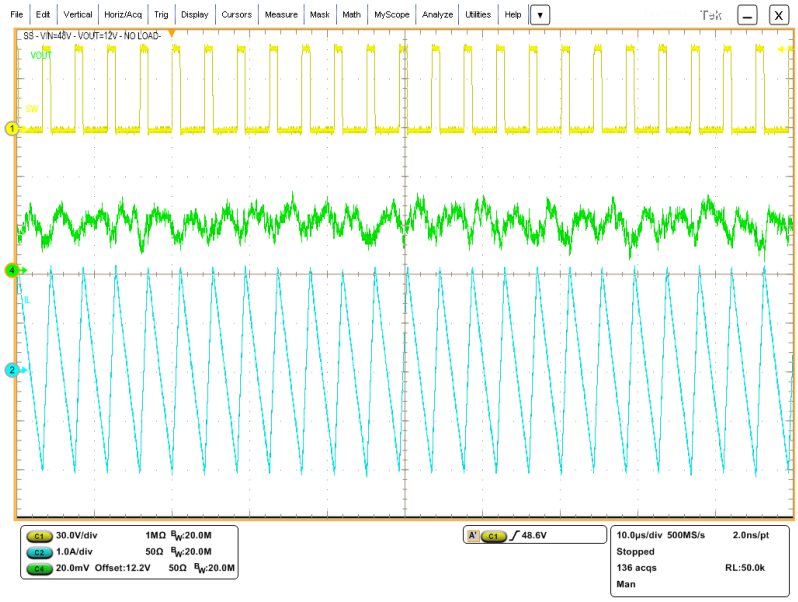


Figure 19. **DEM output voltage ripple at zero load**

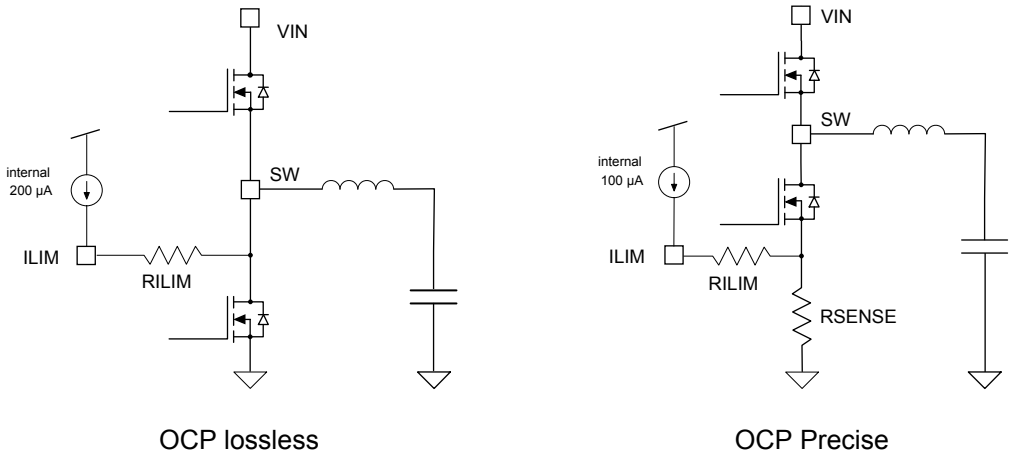
Figure 20. **FPWM output voltage ripple at zero load**



6.7 Overcurrent protection

The current protection circuitry features a constant current protection to handle an exceptional dynamic load request that can persist continuously for maximum 128 clock cycles. Within this time window, the device limits the DC output current accordingly with valley current threshold programmed value with R_{ILIM} resistor, as shown in the figure below.

Figure 21. **R_{ILIM} resistor connection to define lossless and precise OCP setting**



In case the overcurrent event is detected longer, the hiccup protection is triggered to limit the stress of the external power components in case of continuous short-circuit event: the switching activity is prevented for 8192 clock cycles and the SS capacitor is discharged for a new soft-start cycle.

Figure 22. **Constant current in persistent short-circuit**

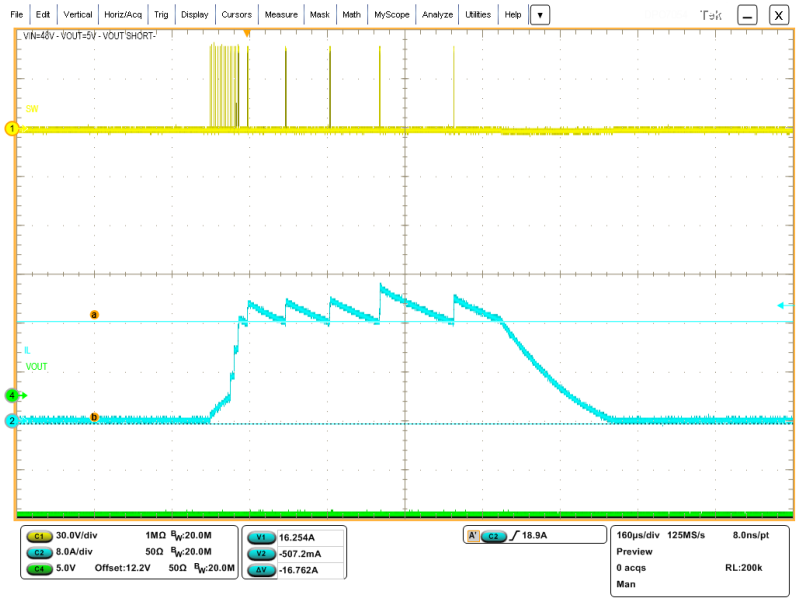
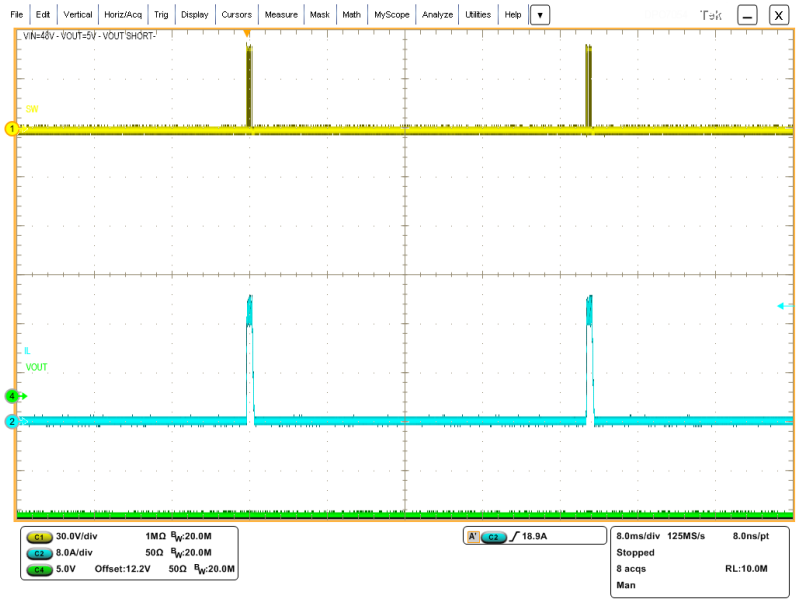


Figure 23. **Hiccup in persistent short-circuit**



The L3751 implements an improved pulse-by-pulse valley current sensing thanks to dedicated control logic for an effective current protection over the duty cycle range. The device supports programmable valley current monitoring across an optional sensing resistor for the best reading accuracy or across the on-state R_{SDON} of the low-side MOSFET to minimize the conduction losses, as shown in Figure 17.

The valley current threshold is easily programmed with series R_{ILIM} resistor connected from I_{LIM} pin to the selected sensing element (see Figure 17). As soon as the LO gate signal is driven high an internal generator sources a constant current out of the I_{LIM} pin so the pin voltage is:

$$V_{ILIM}(t) = (R_{ILIM}+R_x)\cdot I_{ILIM} - R_x \cdot I_{VY}(t) \approx R_{ILIM}\cdot I_{ILIM} - R_x \cdot I_{VY}(t) \quad (5)$$

where R_X can be the low-side R_{DSON} or the shunt resistor. An internal comparator monitors the pin voltage and keeps the low LO signal high until it drops to $V_{ILIM\ TH}$ threshold (- 2 mV typ.)

$$I_{ILIM} = \begin{cases} 200\mu A \ \ at\ T_J = 27°C \ \ in\ case\ of\ RDSON\ lossles\ sensing \\ 100\mu A \ \ at\ T_J = 27°C \ \ in\ case\ of\ precise\ sensing\ on\ shunt\ resistor \end{cases} \quad (6)$$

Both levels compensated with the 4500 ppm/°C thermal coefficient.
As a consequence, assuming $V_{ILIM} \approx 0$, the R_{ILIM} value can be calculated as:

$$R_{ILIM} \approx \frac{R_X \cdot I_{VY\_MAX}}{I_{ILIM}} = \frac{R_X}{I_{ILIM}} \cdot \left(I_{O\_MAX} - \frac{\Delta I_L}{2} \right) \quad (7)$$

where the sensed inductor current I_{VY_MAX} can be expressed in terms of $I_{O\_MAX\ DC}$ output current and the inductor current ripple ΔI_L for simplicity.

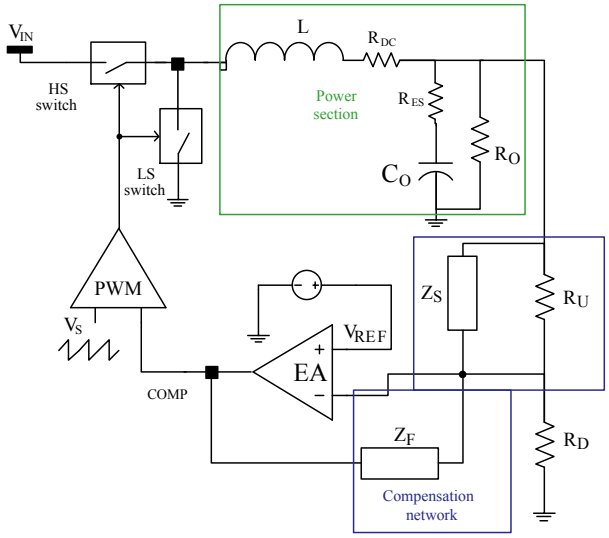
7 Closing the loop

7.1 Total transfer function

The compensation network assures stability and good dynamic performance over the application conditions.

The loop of the L3751 is based on the voltage mode control. The embedded wide bandwidth operational amplifier can be considered ideal in the calculation of the compensator since its frequency response is much larger than designed system bandwidth.

Figure 24. Voltage mode control loop



The transfer function of the PWM modulator, from the error amplifier output (COMP pin) to the LX pin results in an almost constant gain, due to the voltage feedforward which generates a sawtooth with amplitude VS directly proportional to the input voltage.

$$G_{PWM0} = \frac{V_{IN}}{V_S} = \frac{1}{K_{FF}} = 1/30 \tag{8}$$

The transfer function of the power section (i.e. the L-C filters and the output load) is:

$$G_{LC}(s) = \frac{R_O \parallel \left(R_{ES} + {}^{1}\!/\!_{s \cdot C_O}\right)}{R_O \parallel \left(R_{ES} + {}^{1}\!/\!_{s \cdot C_O}\right) + s \cdot L + R_{DC}} \tag{9}$$

given L, R_{DC}, C_0, R_{ES} and R_0 as defined in Figure 23.

For convenience, the G_{LC} can be written as:

$$G_{LC}(s) = G_{LC0} \cdot \frac{1 + \frac{s}{2\pi \cdot f_{ZESR}}}{1 + \frac{s}{2\pi \cdot Q \cdot f_{LC}} + \left(\frac{s}{2\pi \cdot f_{LC}}\right)^2} \quad where \; G_{LC0} = \frac{R_O}{R_O + R_{DC}} \approx 1 \tag{10}$$

$$f_{ZESR} = \frac{1}{2\pi \cdot C_O \cdot R_{ES}} \qquad f_{LC} = \frac{1}{2\pi \cdot \sqrt{L \cdot C_O} \cdot \sqrt{\frac{R_O + R_{ES}}{R_O + R_{DC}}}} \approx \frac{1}{2\pi \cdot \sqrt{L \cdot C_O}} \tag{11}$$

$$Q = \frac{\sqrt{L \cdot C_O} \cdot \sqrt{R_O + R_{DC}}\sqrt{R_O + R_{ES}}}{L + C_O \cdot (R_O \cdot R_{DC} + R_O \cdot R_{ES} + R_{ES} \cdot R_{DC})} \approx \frac{\sqrt{L \cdot C_O} \cdot R_O}{L} = \sqrt{\frac{C_O}{L}} \cdot R_O \tag{12}$$

assuming the inductor and output capacitor parasitic resistance, R_{DC} and R_{ES}, are negligible compared to R_O.

The total closed loop gain is:

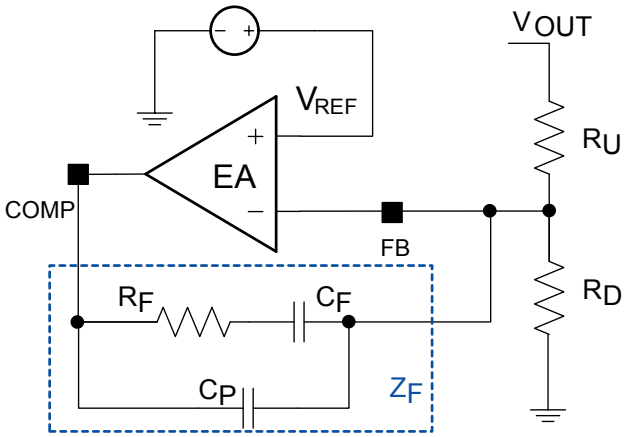
$$G_{LOOP}(s) = G_{PWM0} \cdot G_{LC}(s) \cdot G_{COMP}(s) \quad (13)$$

The implemented compensation network represented with $G_{COMP}(s)$ term depends on the characteristics of the selected output capacitor, as explained in the following chapters.

7.2 Type II compensation network

If the equivalent series resistance (RES) of the output capacitor introduces a zero with a frequency inside the desired bandwidth (that is: $2\pi * R_{ES} * CO > 1 / BW$), this zero help to stabilize the loop. Electrolytic capacitors show non-negligible ESR (> 30 mΩ typically), so with this kind of output capacitor the type II network combined with the zero of the ESR allows the loop to be stabilized.

Figure 25. Type II compensation network



The type II compensation network transfer function, from V_{OUT} to COMP, is computed in the equation below:

$$G_{COMP_{II}}(s) = -\frac{Z_F(s)}{R_U} = -\frac{1 + \frac{s}{2\pi \cdot f_{Z1}}}{\frac{s}{2\pi \cdot f_{P0}} \cdot \left(1 + \frac{s}{2\pi \cdot f_{P1HF}}\right)} \quad (14)$$

$$f_{Z1} = \frac{1}{2\pi \cdot R_F \cdot C_F};\ f_{P0} = \frac{1}{2\pi \cdot (C_F + C_P) \cdot R_U};\ f_{P1HF} = \frac{1}{2\pi \cdot R_F \cdot C_F \parallel C_P} \quad (15)$$

The following suggestions can be followed for a quite common compensation strategy, assuming that $C_P << C_F$. $G_{LOOP}(s)$ in case of type II compensation network and electrolytic output capacitors can be written as follows at $s = 2\pi * f_{BW}$ to derive the R_F / R_U ratio as fixed:

$$G_{LOOPII}(s = 2\pi \cdot f_{BW}) \cong \frac{1}{K_{FF}} \cdot \frac{{f_{LC}}^2}{f_{ZESR}} \cdot \frac{R_F}{R_U} \cdot \frac{1}{f_{BW}} = 1 \quad (16)$$

After choosing the regulator bandwidth (typically $f_{BW} < 0.2 * f_{SW}$) and a value for R_U, usually between 10 kΩ and 100 kΩ in order to achieve C_F and C_P values not comparable with parasitic capacitance of the board, the R_F required value is calculated as follows from the previous equation:

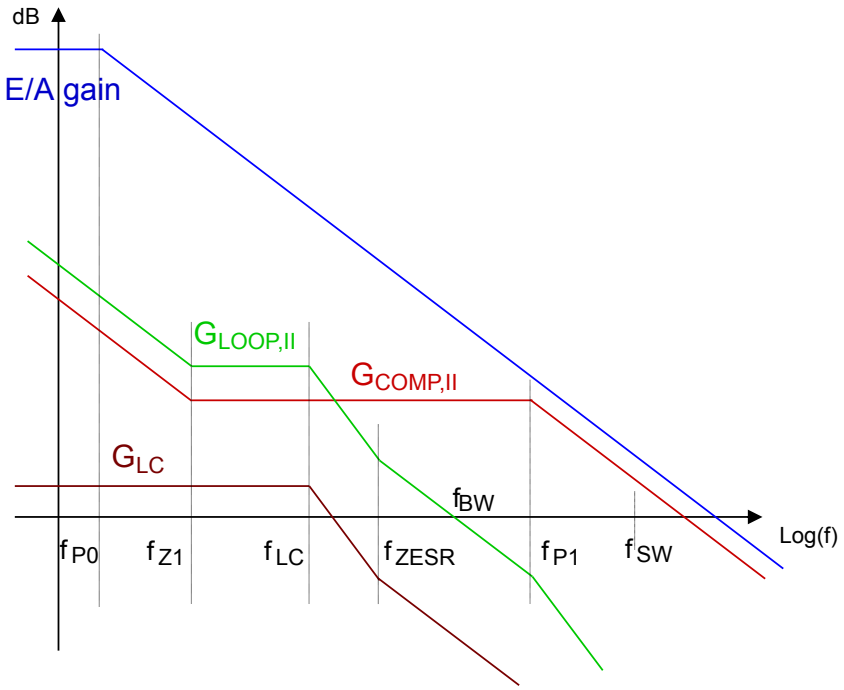
$$R_F = \frac{K_{FF} \cdot f_{ZESR} \cdot f_{BW}}{{f_{LC}}^2} \cdot R_U \quad (17)$$

Select C_F in order to place f_{Z1} below f_{LC} (typically $0.1 * F_{LC}$) and C_P to place f_{P1HF} at $0.5 * f_{SW}$

$$C_F = \frac{1}{2\pi \cdot R_F \cdot 0.1 \cdot f_{LC}} \qquad C_P = \frac{1}{2\pi \cdot R_F \cdot 0.5 \cdot f_{SW}} \quad (18)$$

The resultant control loop and other transfer function gains are shown in the figure below.

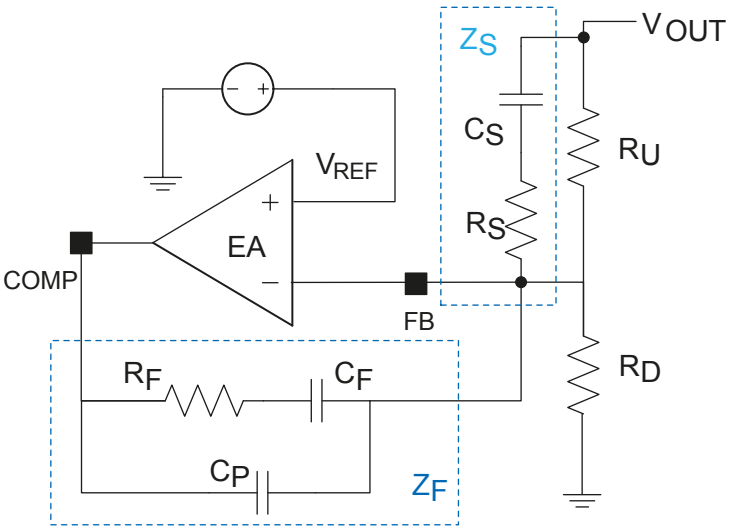
Figure 26. Type II compensation - Bode plot



7.3 Type III compensation network

If f_{ZESR} is higher than the target loop bandwidth, as usually happens if the output filter is based on MLCC ceramic capacitors, a type III compensation network is adviced to increase the bandwidth and system performance.

Figure 27. Type III compensation network



The type III compensation network transfer function, from V_{OUT} to COMP, is computed in the equation below:

$$G_{COMP_{III}}(s) = -\frac{Z_F(s)}{R_U \parallel Z_S(s)} = -\frac{\left(1+\frac{s}{2\pi \cdot f_{Z1}}\right)\cdot\left(1+\frac{s}{2\pi \cdot f_{Z2}}\right)}{\frac{s}{2\pi \cdot f_{P0}}\cdot\left(1+\frac{s}{2\pi \cdot f_{P1HF}}\right)\cdot\left(1+\frac{s}{2\pi \cdot f_{P2HF}}\right)} \quad (19)$$

In addition to the singularities of $G_{COMPII}(s)$, shown in the previous section, one more zero and HF pole are present:

$$f_{Z2} = \frac{1}{2\pi \cdot (R_U + R_S)\cdot C_S} \qquad f_{P2HF} = \frac{1}{2\pi \cdot R_S \cdot C_S} \quad (20)$$

The following suggestions can be followed for a quite common compensation strategy, assuming that $C_P << C_F$ and $R_S << R_U$.

$G_{LOOP}(s)$ in case of type III compensation network and electrolytic output capacitors can be written as follows at the at $s = 2\pi * f_{BW}$ to derive the R_F / R_U ratio as fixed:

$$G_{LOOPIII}(s = 2\pi \cdot f_{BW}) \cong \frac{1}{K_{FF}} \cdot \frac{f_{LC}}{f_{BW}} \cdot \frac{R_F}{R_U} = 1 \quad (21)$$

After choosing the regulator bandwidth (typically $f_{BW} < 0.2 * f_{SW}$) and a value for R_U, usually between 10 kΩ and 100 kΩ in order to achieve C_F and C_P not comparable with parasitic capacitance of the board, the RF required value is calculated as follows from the previous equation:

$$R_F = \frac{K_{FF} \cdot f_{BW}}{f_{LC}} \cdot R_U \quad (22)$$

Select C_F in order to place f_{Z1} below f_{LC} (typically $0.8 * f_{LC}$) and C_P to place f_{P1HF} at $0.5 * F_{SW}$.

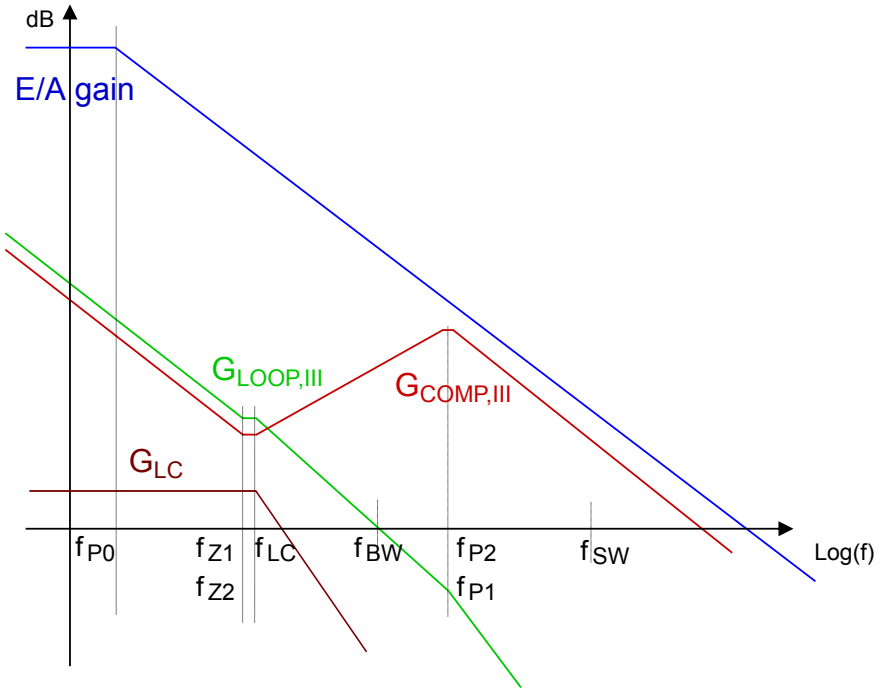
$$C_F = \frac{1}{2\pi \cdot R_F \cdot 0.8 \cdot f_{LC}} \qquad C_P = \frac{1}{2\pi \cdot R_F \cdot 0.5 \cdot f_{SW}} \quad (23)$$

Select C_S in order to place f_{Z2} at $0.8 * f_{LC}$ and R_S to place F_{P2HF} at $0.5 * f_{SW}$.

$$C_S = \frac{1}{2\pi \cdot R_U \cdot 0.8 \cdot f_{LC}} \qquad R_S = \frac{1}{2\pi \cdot C_S \cdot 0.5 \cdot f_{SW}} \quad (24)$$

The resultant control loop and other transfer function gains are shown in figure below.

Figure 28. Type III compensation - Bode plot



8 Application notes

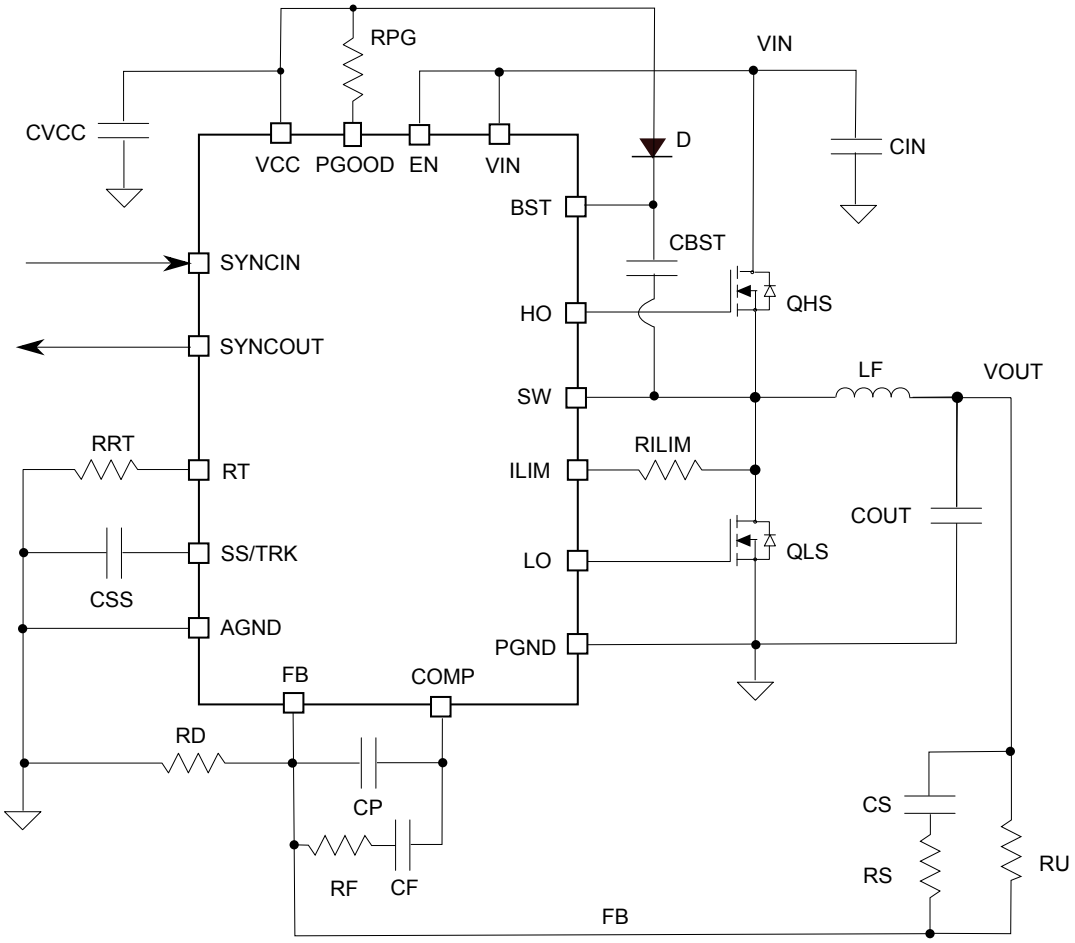
8.1 Output voltage divider

The error amplifier reference voltage is 0.85 V typical.

Referring to Figure 24 for Type II compensator and Figure 26 for type III, the output voltage is adjusted as follows:

$$V_{OUT} = 0.8 \cdot \left(1 + \frac{R_U}{R_D}\right) \quad (25)$$

Figure 29. L3751 application schematic



8.2 Synchronization (forced PWM)

Beating frequency noise is an issue when multiple switching regulators populate the same application board. The L3751 synchronization circuitry features the same switching frequency for a set of regulators simply connecting the SYNCOUT of the master to the SYNCIN pin of the slaves together, so preventing beating noise. The master device provides the synchronization signal to the others.

For proper synchronization of multiple regulators, all of them have to be configured with the same switching frequency, so the same resistor value connected at the RT pin. Alternatively, the SYNCIN can be driven by an external clock signal in accordance with electrical parameters defined in Table 7. The external clock frequency range at SYNCIN pin is -20% to +50% of the programmed oscillator frequency with the RT resistor.

In order to minimize the RMS current flowing through the input filter and improve overall EMC performance, the L3751 device provides a phase shift of 180° between the master and the slaves. If more than two devices are synchronized, the phase shift is fixed and all slaves have a common 180° phase shift with respect to the master.

Considering two L3751 operating synchronized which regulate the same output voltage (i.e.: operating with the same duty cycle), the input filter RMS current is minimized and is calculated as:

$$I_{RMS} = \begin{cases} \frac{I_{OUT}}{2} \cdot \sqrt{2D \cdot (1-2D)} & if\ D < 0.5 \\ \frac{I_{OUT}}{2} \cdot \sqrt{(2D-1) \cdot (2-2D)} & if\ D > 0.5 \end{cases} \quad (26)$$

The graphical representation of the input RMS current of the input filter in the case of two devices with 0° phase shift (synchronized to an external signal) or 180° phase shift (synchronized connecting their SYNCH pins) regulating the same output voltage.

8.3 PCB layout

The PCB design is a crucial factor for the final application EMC and for the proper device operation in buck converter topology, which is critical for inherent high dv/dt pulsed current paths. The scenario gets even more complex for a controller with external MOSFETs because of additional gate-driving paths that are usually internally optimized in a monolithic device.

Figure 30. Pulsed current paths in buck topology

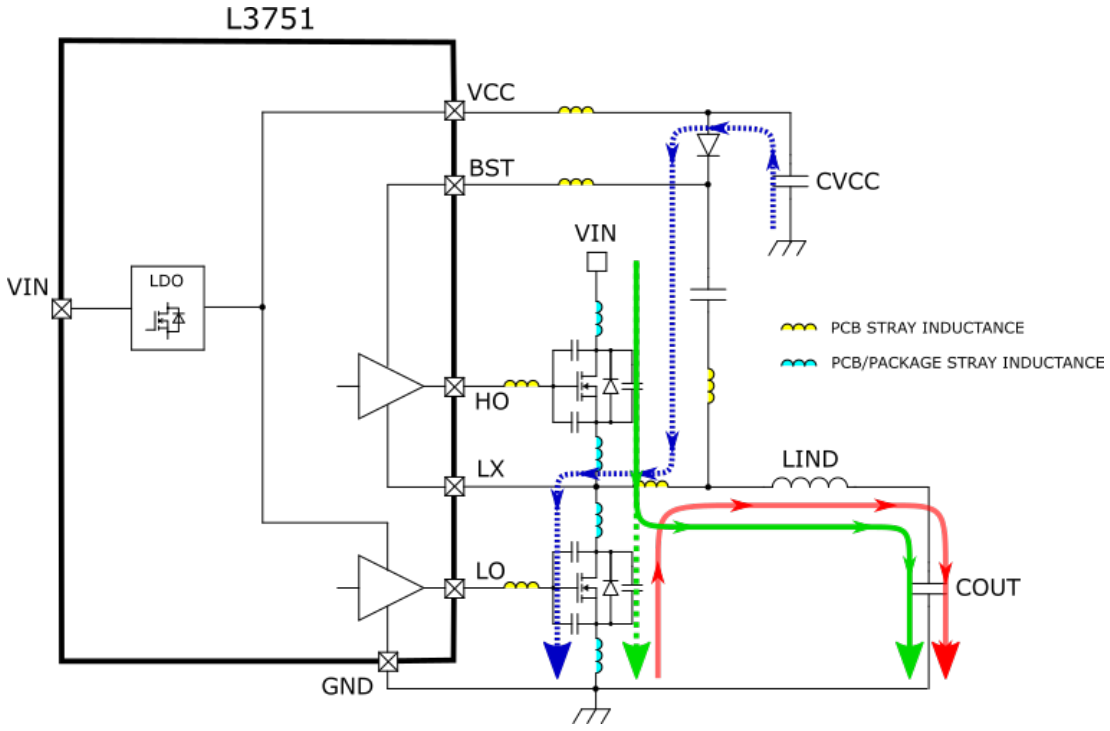


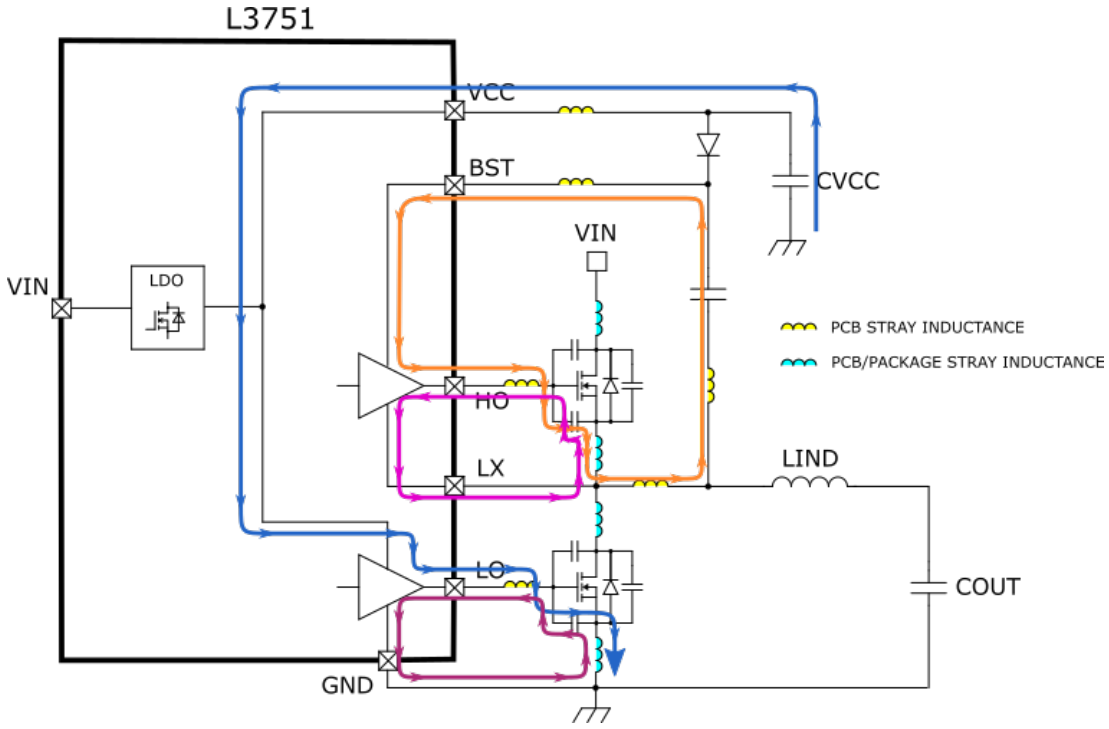
Figure 30 shows the current paths in buck topology: at TON time when HS ("high-side Switch") is closed, an impulsive current, green-dotted trace, flows from VIN to the LS (“low-side switch”) diode to recover the majority gate charge in spatial zone; that is the Qrr for the diode reverse recovery operation from forward biasing. This pulsed current level can be much higher than load current: the gate charge amount depends on the diode p-n junction and the peak current is limited only by parasitic. When the diode is reverse biased, the LX node rises and the HS current becomes the inductor current, so the output current ripple included, which is the green trace.

Contrarly to the HS turn-off (red trace), the inductor current starts to flow through the LS body-diode during the deadtime and then through the LS, when enabled by the anti-cross conduction circuitry. At the same time, the blue-dotted trace current, flowing from VCC to the LX node grounded, restores the HS gate charge spent during TON on the bootstrap capacitor and compensates for the HS driver current consumption.

The quoted switched currents may generate voltage spikes caused by inductive parasitic components related to the PCB board traces and package bonding wires of the external power components.

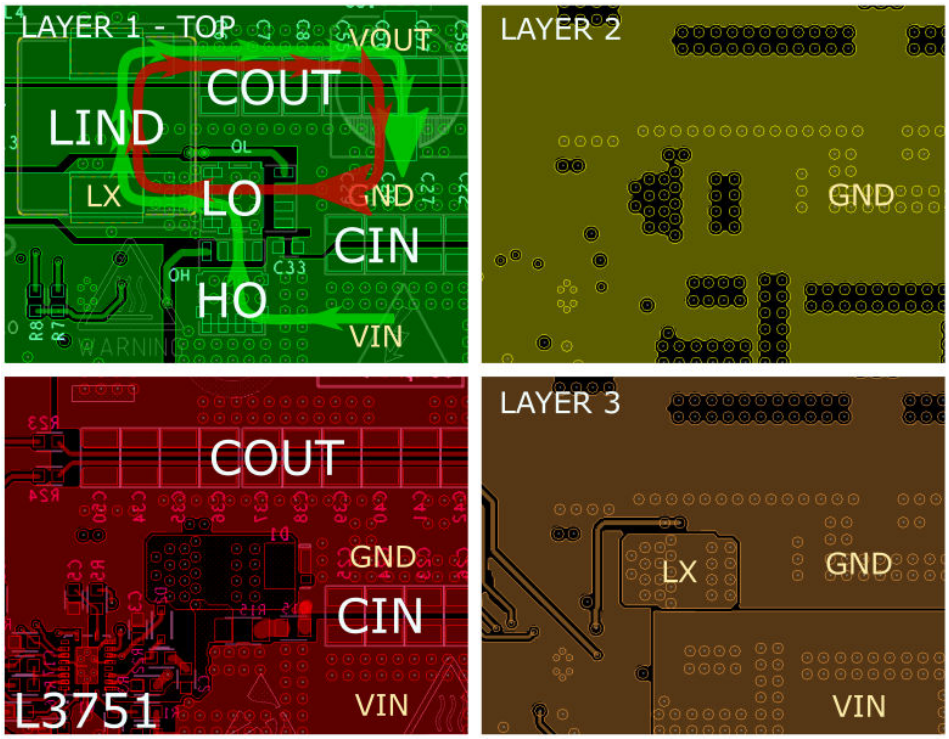
In addition to that described above, which applies to a monolithic device with power elements embedded, a controller with external MOSFETs like the L3751 has additional gate-driving loops for the external MOSFETs, as shown in Figure 31.

Figure 31. **High frequency gate-driving loops**



The orange and blue traces represent the turning-on paths for HS and LS respectively, while purple and dark red traces the external MOSFETs turning-off paths. All these loops operate at the switching frequency, high dv/dt with current capability limited by the internal MOSFETs of the drivers (few ohms).

Figure 32. **Board layout example**



Consequently, as anticipated at the beginning of the section, the external power component placing (Cin, Cboot, Cvcc, diode and both power elements) and wire connection to minimize inductive parasitic components is critical for the device operation and EMC reduction. Figure 32 shows an example of optimized board layout in terms of component placing and wire trace design that keep the mentioned critical loops on the layer 1, preventing PCB via insertion in critical high frequency loops.

9 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

9.1 QFN20 (3.5 x 4.5 mm) package information

Figure 33. **QFN20 (3.5 x 4.5 mm) package outline**

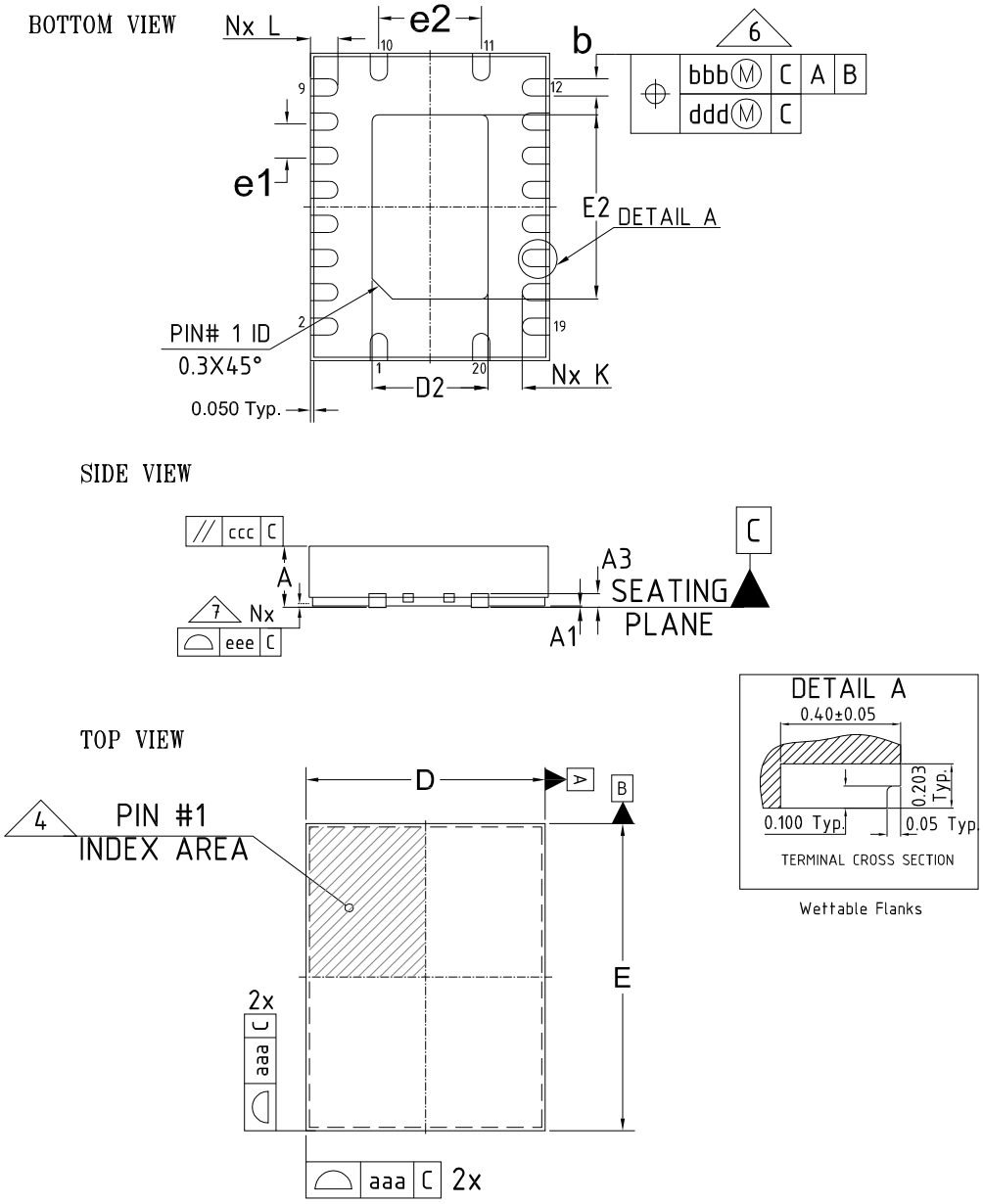
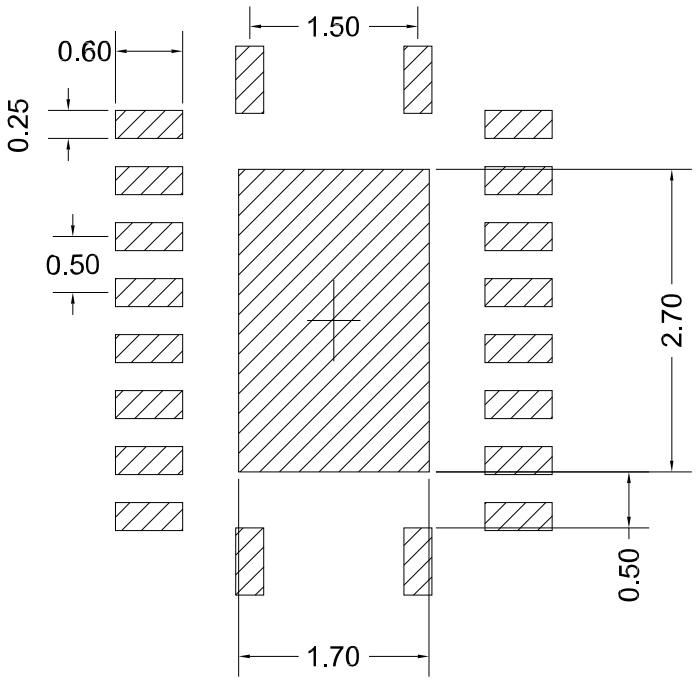


Table 9. **QFN20 (3.5 x 4.5 mm) mechanical data**

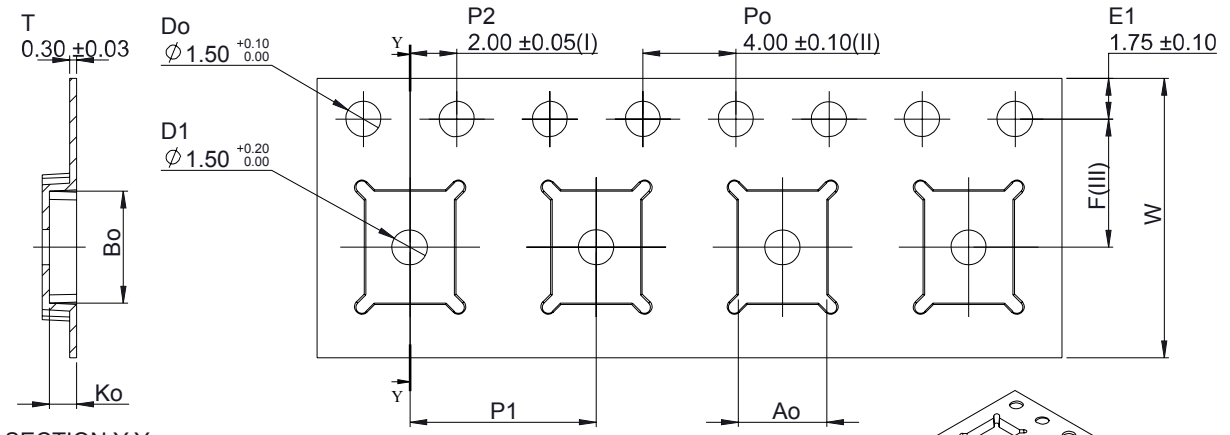
Dim.	mm		
	Min.	Typ.	Max.
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A3		0.203 Ref.	
b	0.20	0.25	0.30
D		3.50 BSC	
E		4.50 BSC	
e1		0.50 BSC	
e2		1.50 BSC	
D2	1.60	1.70	1.80
E2	2.60	2.70	2.80
K	0.20	-	-
L	0.30	0.40	0.50
N		20	
ND		2	
NE		8	
aaa		0.05	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	

Figure 34. **QFN20 (3.5 x 4.5 mm) recommended footprint**



9.2 QFN20 (3.5 x 4.5 mm) packing information

Figure 35. **QFN20 (3.5 x 4.5 mm) tape drawing**



Ao	3.80	+/- 0.10
Bo	4.80	+/- 0.10
Ko	1.18	+/- 0.10
F	5.50	+/- 0.05
P1	8.00	+/- 0.10
W	12.00	+0.30/-0.10

(I) Measured from centreline of sprocket hole to centreline of pocket.
(II) Cumulative tolerance of 10 sprocket holes is ± 0.20 .
(III) Measured from centreline of sprocket hole to centreline of pocket.
(IV) Other material available.
(V) Typical SR of Formed tape to be $1.0X10^{4}$ Ω≤ SR≤$1.0X10^{10}$Ω.
ALL DIMENSIONS IN MILLIMETRES UNLESS OTHERWISE STATED.

Figure 36. **QFN20 (3.5 x 4.5 mm) tape oriented**

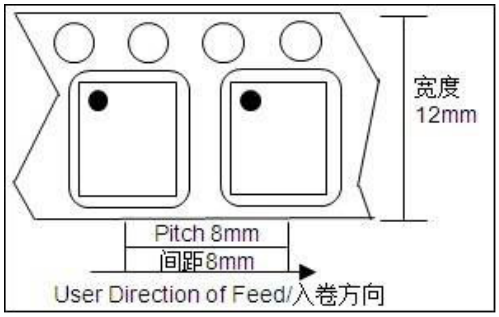
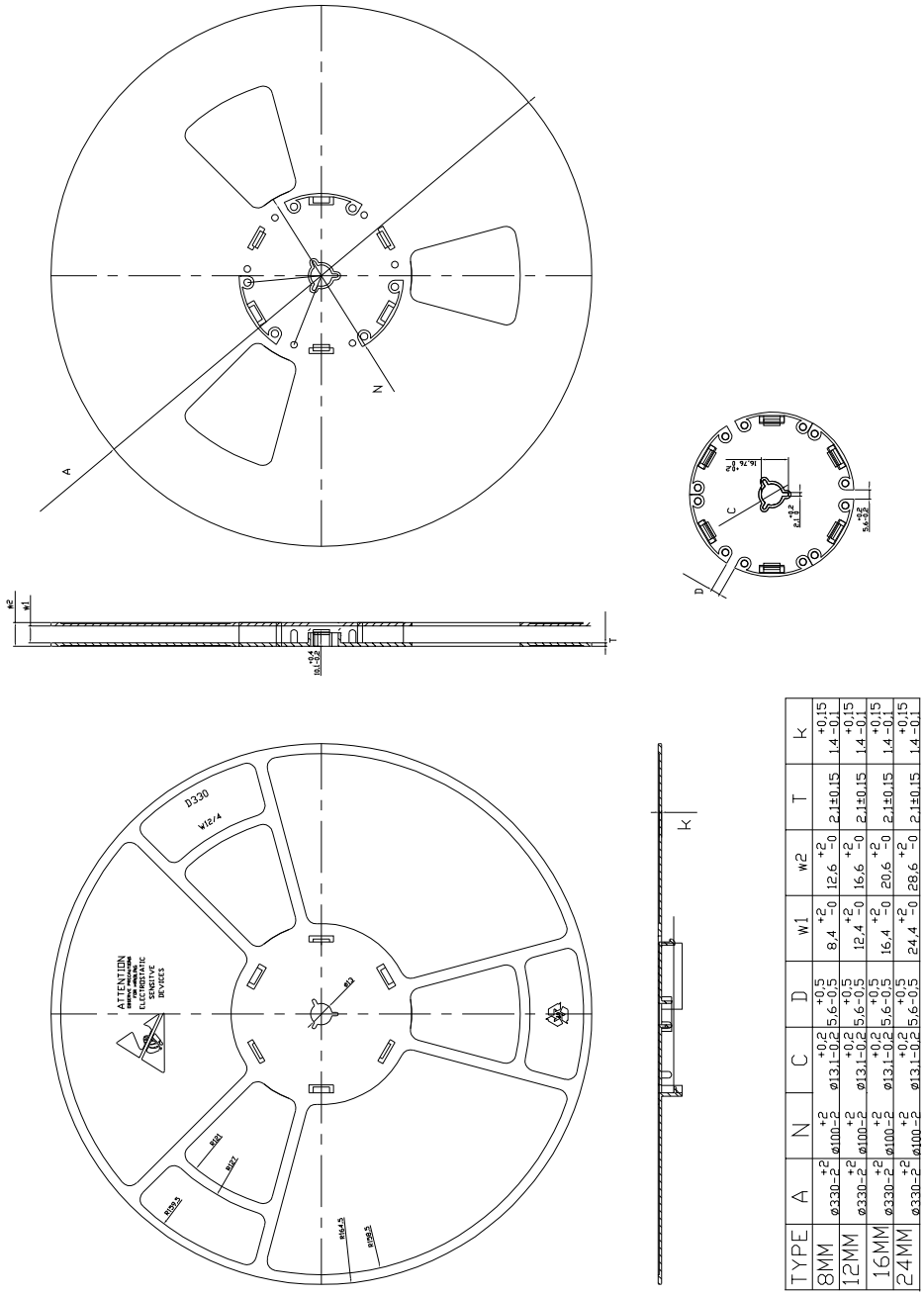


Figure 37. **QFN20 (3.5 x 4.5 mm) reel dimensions**



TYPE	A	N	C	D	W1	W2	T	K
8MM	ø330-2 +2	ø100-2 +2	ø13.1-0.2 +0.2	5.6-0.5 +0.5	8.4 +2 -0	12.6 +2 -0	2.1±0.15	1.4-0.1 +0.15
12MM	ø330-2 +2	ø100-2 +2	ø13.1-0.2 +0.2	5.6-0.5 +0.5	12.4 +2 -0	16.6 +2 -0	2.1±0.15	1.4-0.1 +0.15
16MM	ø330-2 +2	ø100-2 +2	ø13.1-0.2 +0.2	5.6-0.5 +0.5	16.4 +2 -0	20.6 +2 -0	2.1±0.15	1.4-0.1 +0.15
24MM	ø330-2 +2	ø100-2 +2	ø13.1-0.2 +0.2	5.6-0.5 +0.5	24.4 +2 -0	28.6 +2 -0	2.1±0.15	1.4-0.1 +0.15

Revision history

Table 10. **Document revision history**

Date	Revision	Changes
08-Apr-2022	1	Initial release.
06-Dec-2022	2	Updated Table 1. Pin description Updated Section 6.5 Embedded gate driver supply Added Figure 13. VCC power circuite
13-Feb-2023	3	Updated Table 1, Figure 3, Figure 25, Figure 27 and Figure 29. Minor text changes.

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