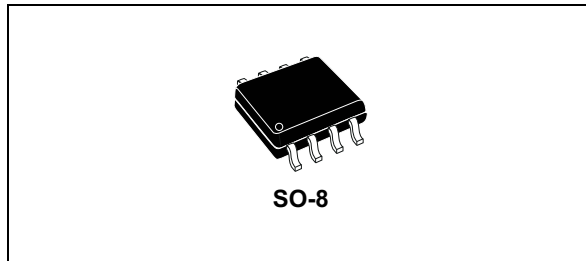


## 5 V low drop linear voltage regulator for automotive application

Datasheet - production data



- Enable input for enabling/disabling the voltage regulator
- Thermal shutdown and short circuit protection
- Wide temperature range ( $T_j = -40^{\circ}\text{C}$  to  $150^{\circ}\text{C}$ )

### Description

The L5050S is a 5 V low dropout linear voltage regulator suitable for automotive applications, available in a SO-8 package. The LDO delivers up to 50 mA of load current, and consumes as low as 5  $\mu\text{A}$  of quiescent current with device disabled. High output voltage accuracy ( $\pm 2\%$ ) is kept over wide temperature range, line and load variation. Enable feature allows output enabling or disabling. The maximum input voltage is 40 V. The regulator output current is internally limited and the device is protected against short circuit, overload and over temperature conditions. In addition, only low value ceramic capacitor on output is required for stability.

### Features

Max DC supply voltage	$V_S$	40 V
Max output voltage tolerance	$\Delta V_o$	$\pm 2\%$
Max dropout voltage	$V_{dp}$	500 mV
Output current	$I_o$	50 mA
Quiescent current	$I_{qn}$	5 $\mu\text{A}$ <sup>(1)</sup>

1. Typical value valid with  $E_n = \text{LOW}$ .


- AEC-Q100 qualified 
- Operating DC supply voltage range 5.6 V to 40 V
- Low dropout voltage
- Low quiescent current consumption
- Precision output voltage 5 V  $\pm 2\%$

Table 1. Device summary

Package	Order codes
	Tape & reel
SO-8	L5050STR

L5050S

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# 1 Block diagram and pins description

Figure 1. Functional block diagram – L5050S

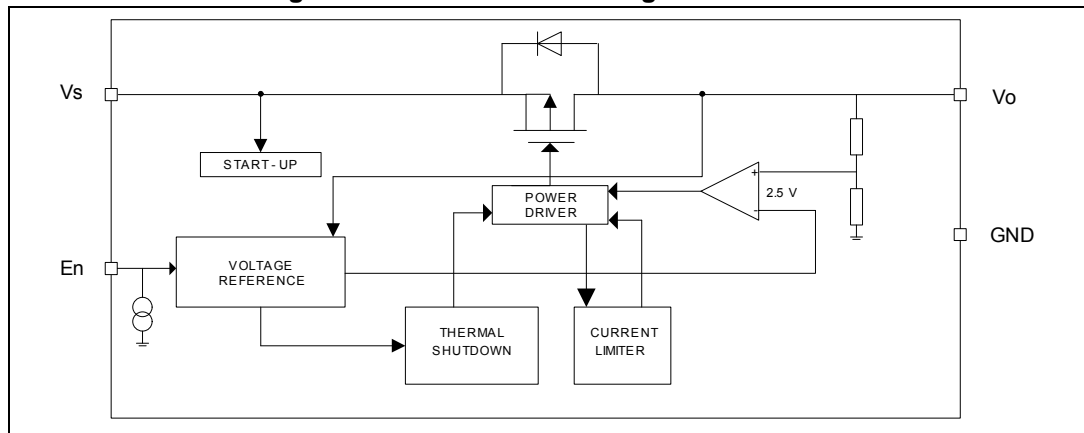


Figure 2. Pins configuration

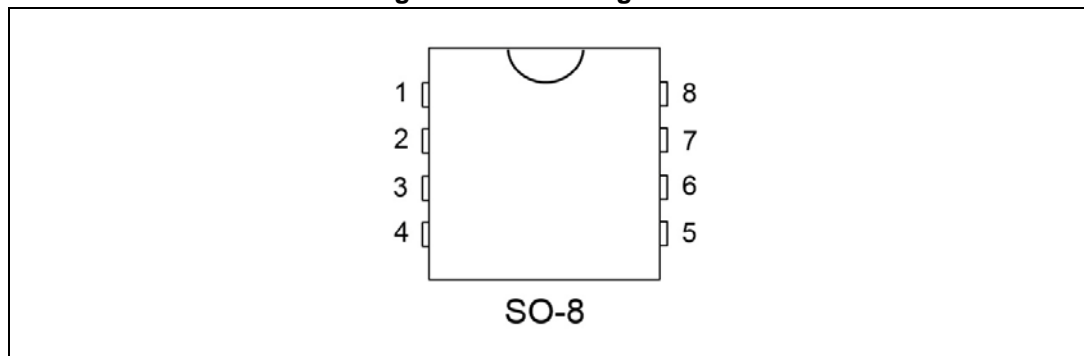


Table 2. Pins description

Pin name	L5050S Pin number	Function
N.C.	1	—
GND	2	Ground reference for regulator.
Vo	3	5 V regulated output. Block to GND with a ceramic capacitor ( $\geq 220$ nF for regulator stability).
N.C.	4	—
N.C.	5	—
Vs	6	Supply voltage, block directly to GND on the IC with a capacitor.
En	7	Enable pin: high signal to switch the regulator on.
N.C.	8	—

## 2 Electrical specifications

### 2.1 Absolute maximum ratings

Stressing the device above the rating listed in the [Table 3: Absolute maximum ratings](#) may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE program and other relevant quality documents.

**Table 3. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_S$	DC supply voltage	-0.3 to 40	V
$I_S$	Input current	Internally limited	
$V_O$	DC output voltage	-0.3 to 6	V
$I_O$	DC output current	Internally limited	
$V_{En}$	Enable input	-0.3 to 40	
$T_j$	Junction operating temperature	-40 to 150	°C
$V_{ESD\ HBM}$	ESD HBM voltage level (HBM-MIL STD 883C)	±2	kV
$V_{ESD\ CDM}$	ESD CDM voltage level (CDM)	±750	V

**Table 4. Thermal data**

Item	Symbol	Parameter	Value <sup>(1)</sup>	Unit
A.001	$R_{th-jamb}$	Thermal resistance junction to ambient	110	°C/W

1. PCB: double layer; FR4 area = 77 mm x 86 mm; PCB thickness = 1.6 mm; Cu thickness = 70 µm (front and back side).

### 2.2 Electrical characteristics

Values specified in this section are for  $V_S = 5.6\text{ V to }31\text{ V}$ ,  $T_j = -40\text{ °C to }+150\text{ °C}$ , unless otherwise stated.

**Table 5. General**

Item	Pin	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
A.002	$V_O$	$V_O$	Output voltage	$V_S = 5.6\text{ to }31\text{ V}$ ; $I_O = 5\text{ to }50\text{ mA}$	4.9	5	5.1	V
A.003	$V_O$	$I_{short}$	Short circuit current	$V_S = 5.6\text{ to }31\text{ V}$	200	380	550	mA
				$V_S = 10.5\text{ V}$	200	370	450	
A.004	$V_O$	$I_{lim}^{(1)}$	Output current limitation	$V_S = 10.5\text{ V}$	100	225	450	mA
A.005	$V_S, V_O$	$V_{line}$	Line regulation voltage	$V_S = 5.6\text{ to }18\text{ V}$ ; $I_O = 5\text{ to }50\text{ mA}$			50	mV

Table 5. General (continued)

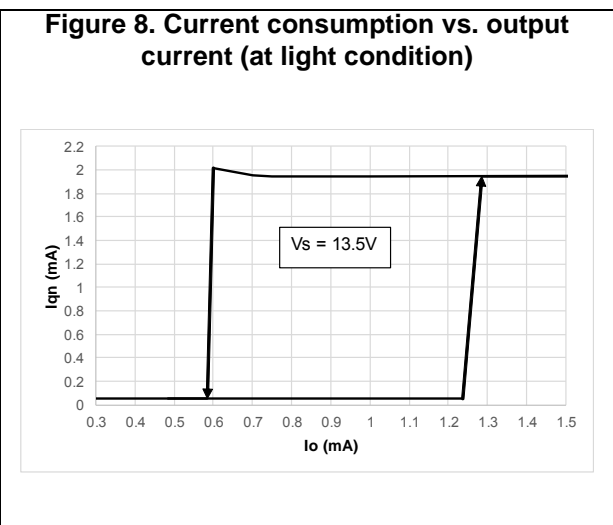
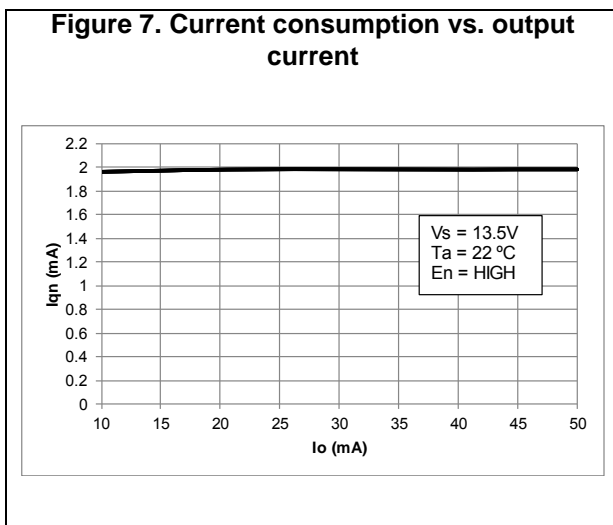
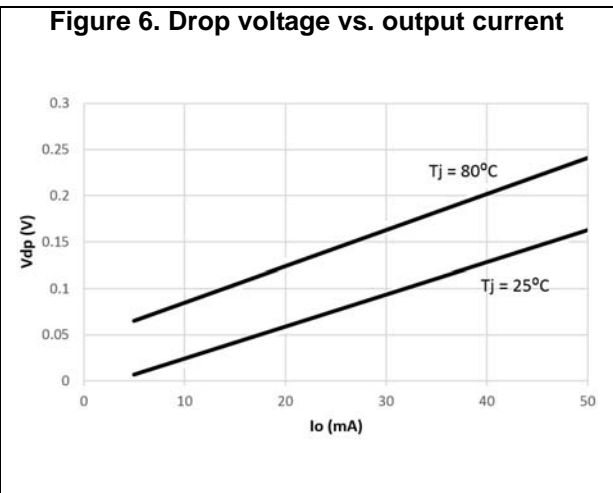
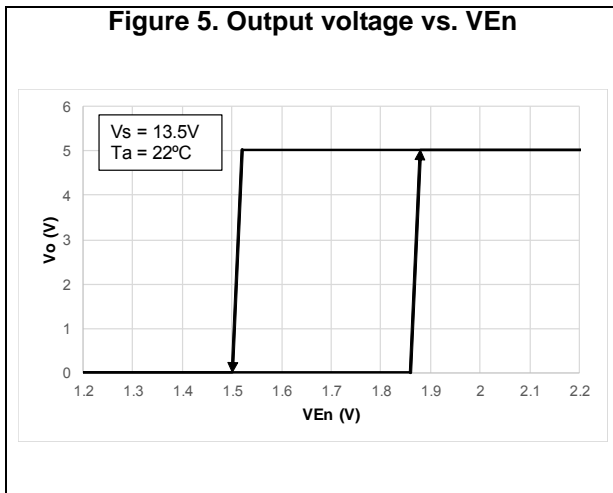
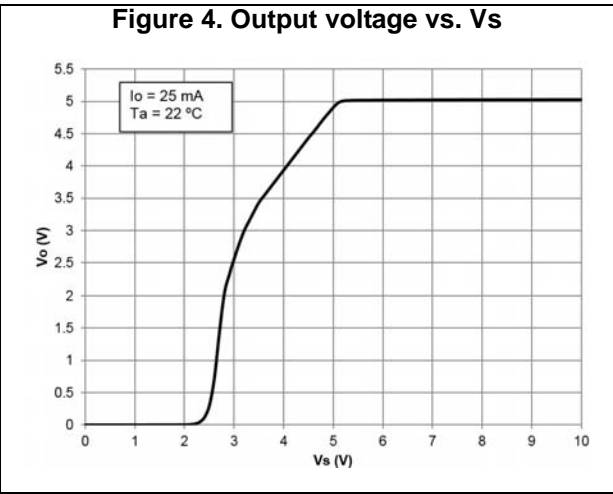
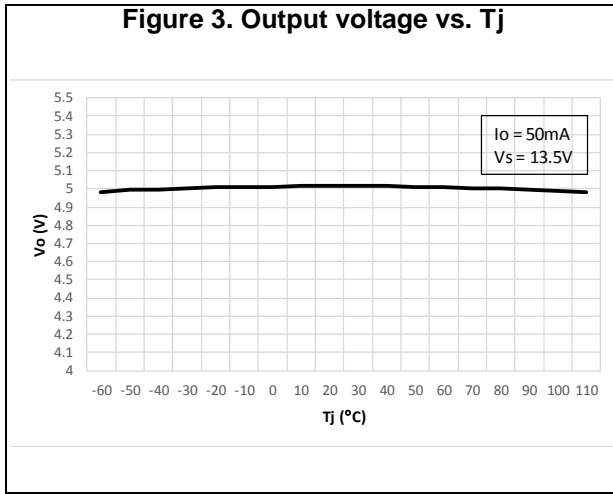
Item	Pin	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
A.006	V <sub>o</sub>	V <sub>load</sub>	Load regulation voltage	I <sub>o</sub> = 5 to 50 mA, V <sub>S</sub> = 5.6 to 31 V			55	mV
A.007	V <sub>S</sub> , V <sub>o</sub>	V <sub>dp</sub>	Drop voltage	I <sub>o</sub> = 50 mA			500	mV
A.008	V <sub>S</sub> , V <sub>o</sub>	SVR	Ripple rejection	fr = 100 Hz <sup>(2)</sup>		60		dB
A.009	V <sub>o</sub>	I <sub>o<sub>th_H</sub></sub>	Normal consumption mode output current		4			mA
A.010	V <sub>o</sub>	I <sub>o<sub>th_L</sub></sub>	Very low consumption mode output current				0.1	mA
A.011	V <sub>S</sub> , V <sub>o</sub>	I <sub>qn</sub>	Current consumption with regulator disabled I <sub>qn</sub> = I <sub>Vs</sub> – I <sub>o</sub>	V <sub>S</sub> = 13.5 V, En = low		5	10	μA
A.012	V <sub>S</sub> , V <sub>o</sub>	I <sub>qn_1</sub>	Current consumption with regulator enabled I <sub>qn_1</sub> = I <sub>Vs</sub> – I <sub>o</sub>	I <sub>o</sub> = 0.1 mA to 0.3 mA; En = high		50	70	μA
A.013	V <sub>S</sub> , V <sub>o</sub>	I <sub>qn_50</sub>	Current consumption with regulator enabled I <sub>qn_50</sub> = I <sub>Vs</sub> – I <sub>o</sub>	I <sub>o</sub> = I <sub>o<sub>th_H</sub></sub> to 50 mA; En = high		2	4.2	mA
A.014		T <sub>w</sub>	Thermal protection temperature <sup>(3)</sup>		150		190	°C
A.015		T <sub>w_hy</sub>	Thermal protection temperature hysteresis			10		°C

1. Measured output current when the output voltage has dropped 200 mV from its nominal value obtained at V<sub>S</sub>=10.5 V and I<sub>o</sub> = 25 mA.
2. Guaranteed by design.
3. Thermal protection is guaranteed by design and characterization.

Table 6. Enable

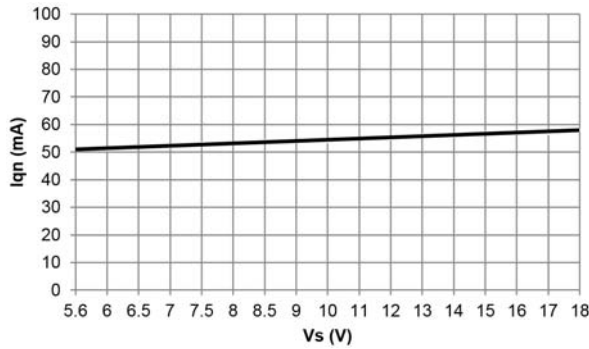
Item	Pin	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
A.016	En	V <sub>En_low</sub>	En input low voltage				1	V
A.017	En	V <sub>En_high</sub>	En input high voltage		3			V
A.018	En	V <sub>En_hyst</sub>	En input hysteresis			800		mV
A.019	En	I <sub>leak</sub>	Pull down current	V <sub>En</sub> = 5 V		3	10	μA

### 2.3 Electrical characteristics curves

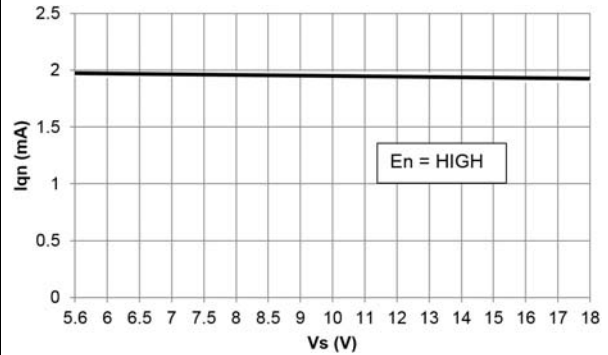




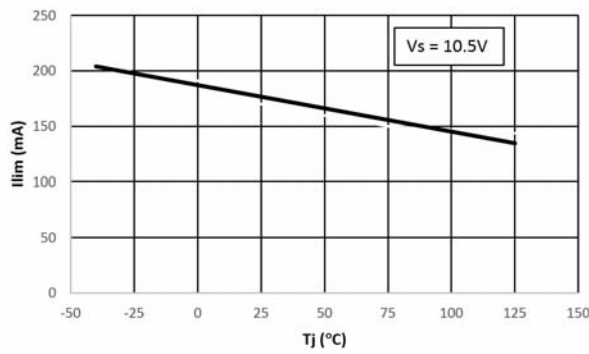
**Figure 9. Current consumption vs input voltage**  
( $I_o = 0.15 \text{ mA}$ )



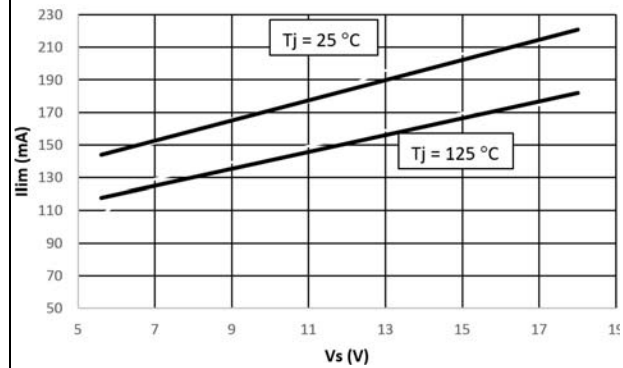
**Figure 10. Current consumption vs input voltage**  
( $I_o = 50 \text{ mA}$ )



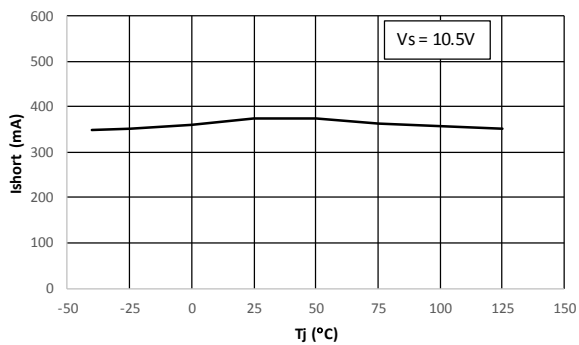
**Figure 11. Current limitation vs  $T_j$**



**Figure 12. Current limitation vs input voltage**



**Figure 13. Short circuit current vs  $T_j$**



**Figure 14. Short circuit current vs input voltage**

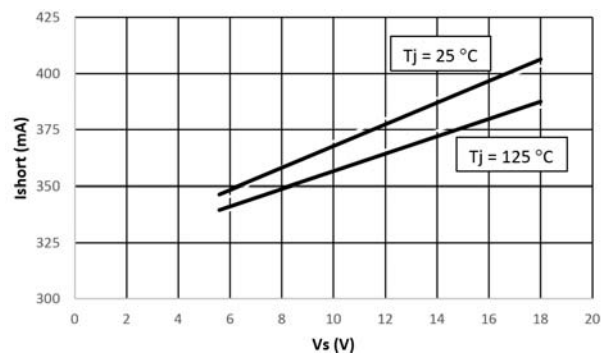


Figure 15. VEn\_high vs Tj

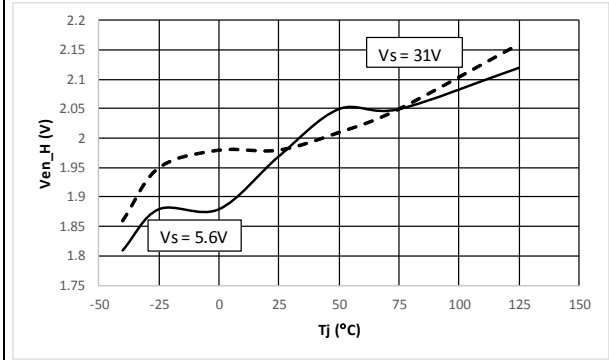


Figure 16. VEn\_low vs Tj

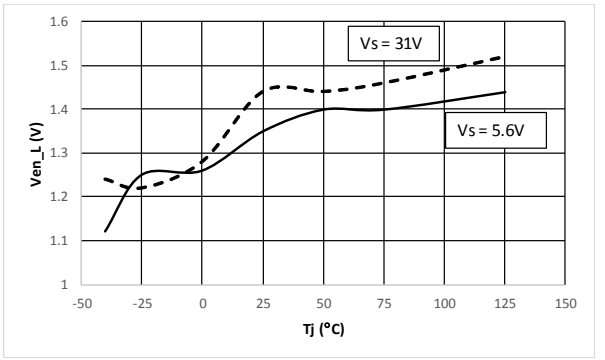
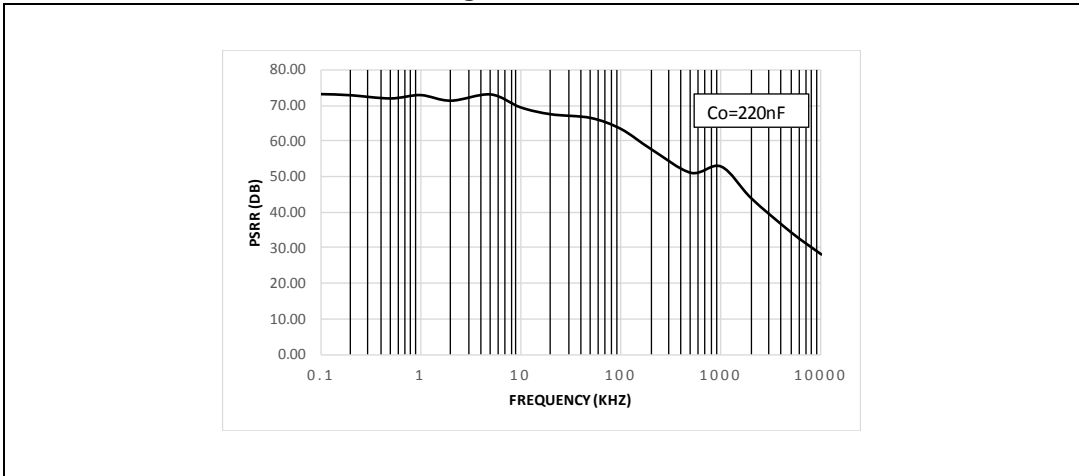


Figure 17. PSRR

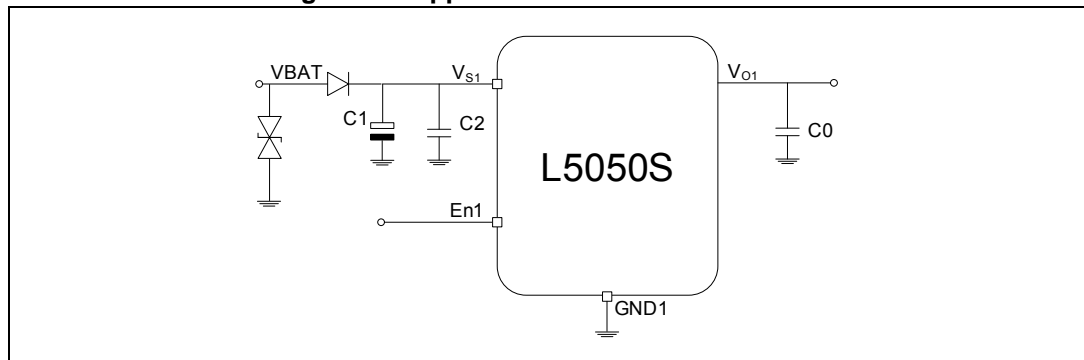


## 3 Protection features

### 3.1 Voltage regulator

Voltage regulator uses a p-channel MOS transistor as a regulating element. With that structure, a very low dropout voltage at current up to 50mA is obtained. The output voltage is regulated up to transient input supply voltage of 40 V. The high-precision of the output voltages ( $\pm 2\%$ ) is obtained with a pre-trimmed reference voltage. The voltage regulator automatically adapts its own quiescent current to the output current level. In light load conditions, the quiescent current goes down to 50  $\mu\text{A}$  only in low consumption mode. This procedure features a certain hysteresis on the output current (see [Figure 8](#)). Short-circuit protection to GND and a thermal shutdown are provided.

**Figure 18. Application schematic – L5050S**



The input capacitor  $C_1$  is necessary as backup supply for short battery voltage interruption which may occur on the line. Its value should be chosen according to the relevant application requirement. The second input capacitor  $C_2 \geq 220 \text{ nF}$  is needed when the  $C_1$  is too distant from the  $V_{S1}$  pin and it compensates smooth line disturbances. The  $C_0$  ceramic capacitor, connected to the output pin, is for bypassing to GND the high-frequency noise and it guarantees stability even during sudden line and load variations. Suggested value is  $C_0 = 220 \text{ nF}$  with  $\text{ESR} \geq 100 \text{ m}\Omega$ .

Stability region is reported in [Figure 19](#).

**Figure 19. Stability region**

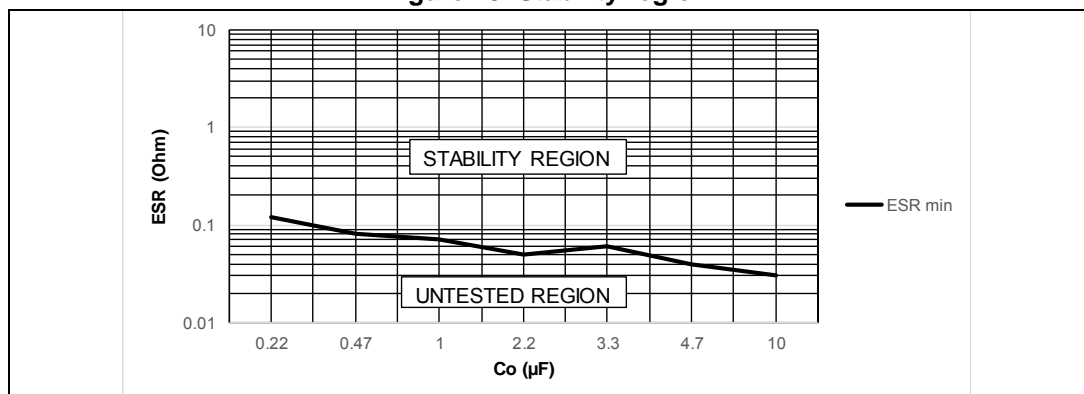
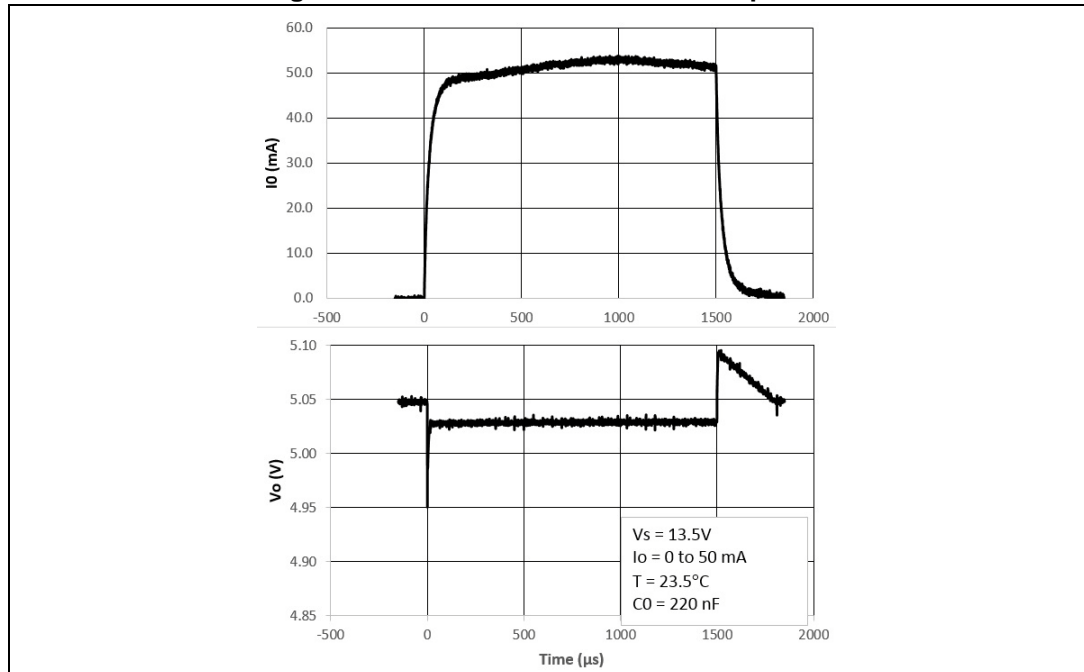


Figure 20. Maximum load variation response

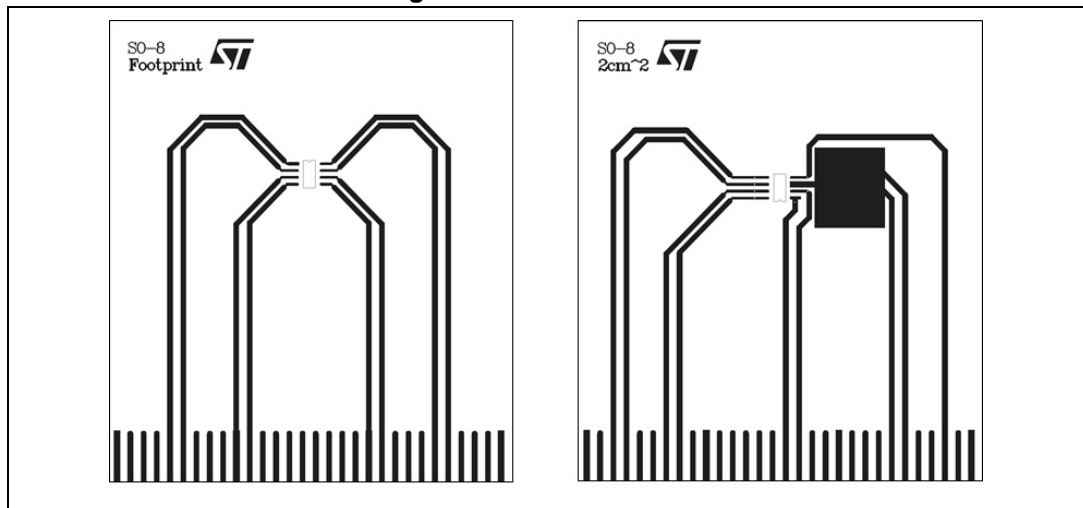


### 3.2 Enable

The L5050S features one enable input. A high signal switches the regulator element ON. In standby mode, the output is disabled and the current consumption of the device (quiescent current) is typically 5  $\mu\text{A}$ .

## 4 Package and PCB thermal data

Figure 21. SO-8 PC board



Layout condition of Rth and Zth measurements (PCB: double layer; FR4 area = 77 mm x 86 mm; PCB thickness = 1.6 mm; Cu thickness = 70 μm (front and back side); Cu thickness on vias of 0.025 mm in PCB with a dissipation area of 2cm<sup>2</sup> (picture on the right).

Figure 22. Rthj-amb vs PCB copper area in open box free air condition

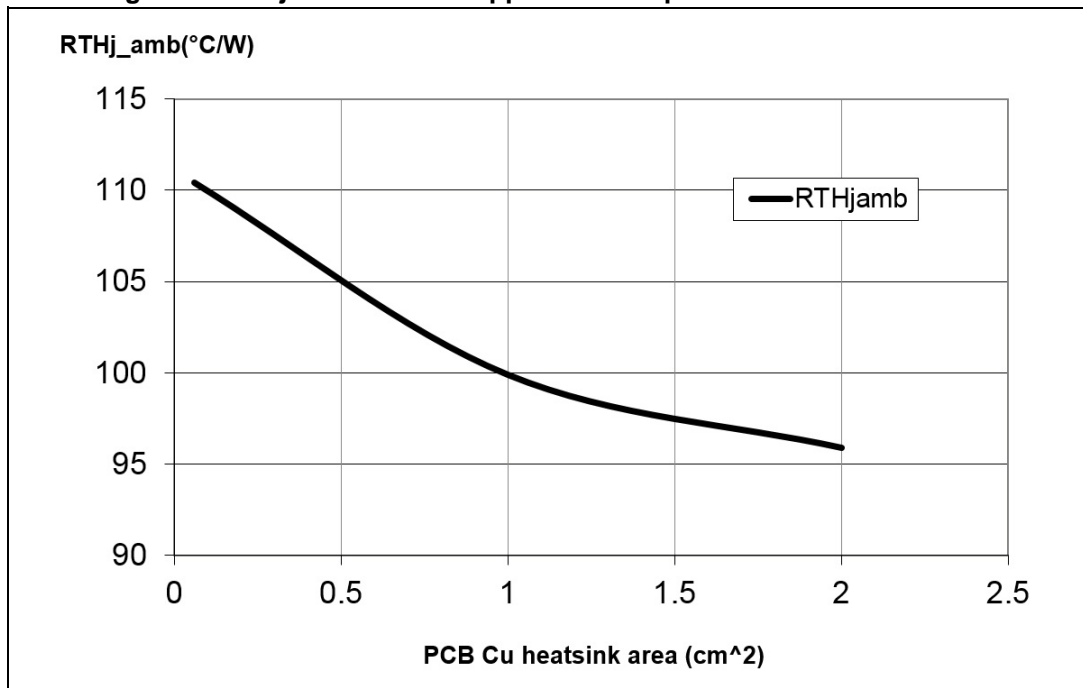
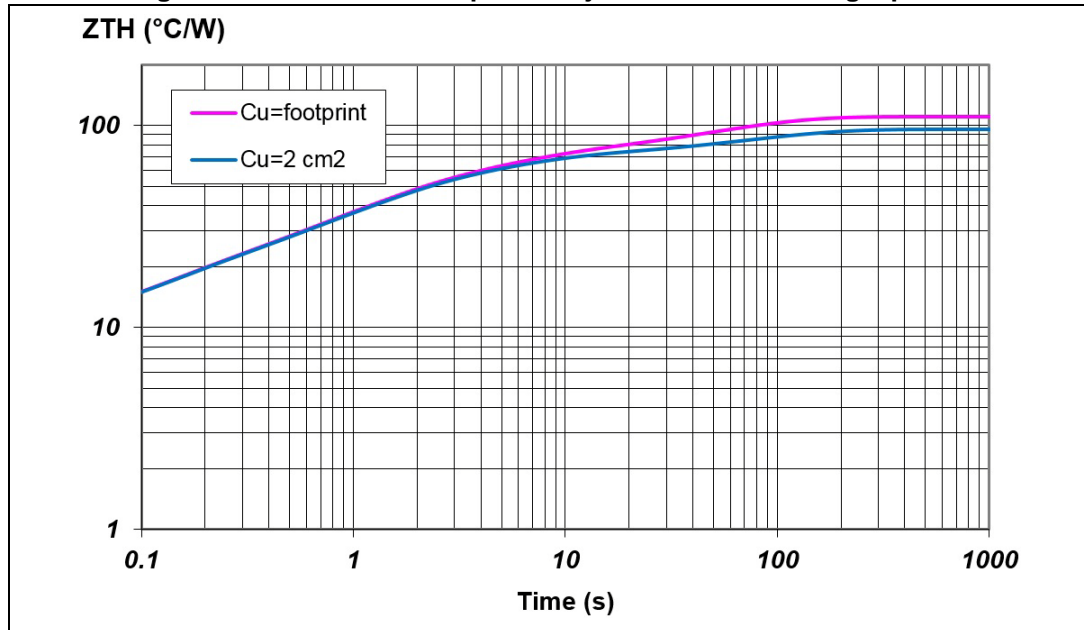


Figure 23. SO-8 thermal impedance junction ambient single pulse



Equation 1: Pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp} \cdot (1 - \delta)$$

where

$$\delta = (tp)/T$$

Figure 24. Thermal fitting model of a Vreg in SO-8

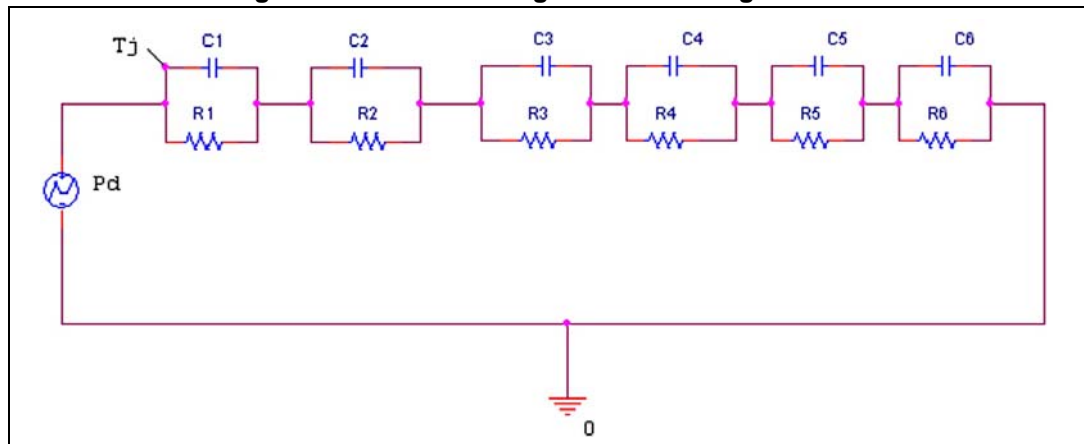


Table 7. SO-8 thermal parameter

Area/island (cm <sup>2</sup> )	FP	2
R1 (°C/W)	3.2	
R2 (°C/W)	4.2	
R3 (°C/W)	7.9	

Table 7. SO-8 thermal parameter (continued)

Area/island (cm <sup>2</sup> )	FP	2
R4 (°C/W)	26.5	
R5 (°C/W)	27	
R6 (°C/W)	41.6	27.1
C1 (W.s/°C)	0.00001	
C2 (W.s/°C)	0.0015	
C3 (W.s/°C)	0.014	
C4 (W.s/°C)	0.04	
C5 (W.s/°C)	0.165	
C6 (W.s/°C)	1.4	3

## 5 Package information

### 5.1 ECOPACK

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

### 5.2 SO-8 package information

Figure 25. SO-8 package outline

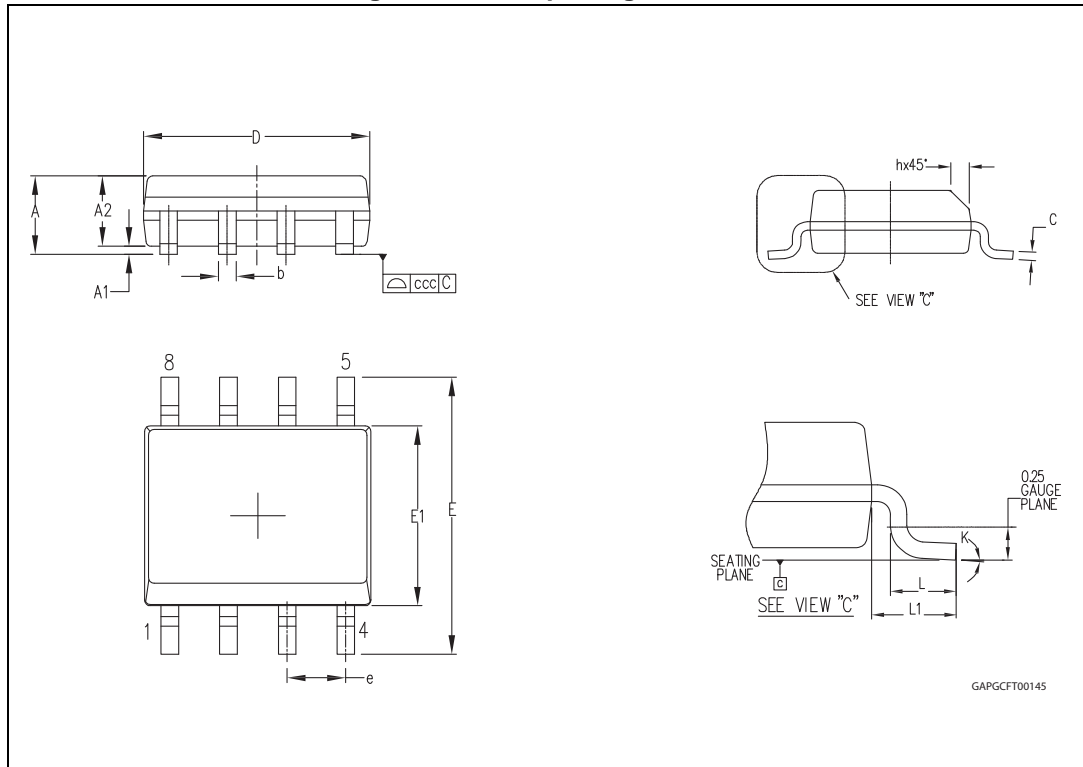


Table 8. SO-8 package mechanical data

Symbol	Millimeters		
	Min	Typ.	Max
A			1.75
A1	0.10		0.25
A2	1.25		
b	0.28		0.48
c	0.17		0.23
D <sup>(1)</sup>	4.80	4.90	5.00



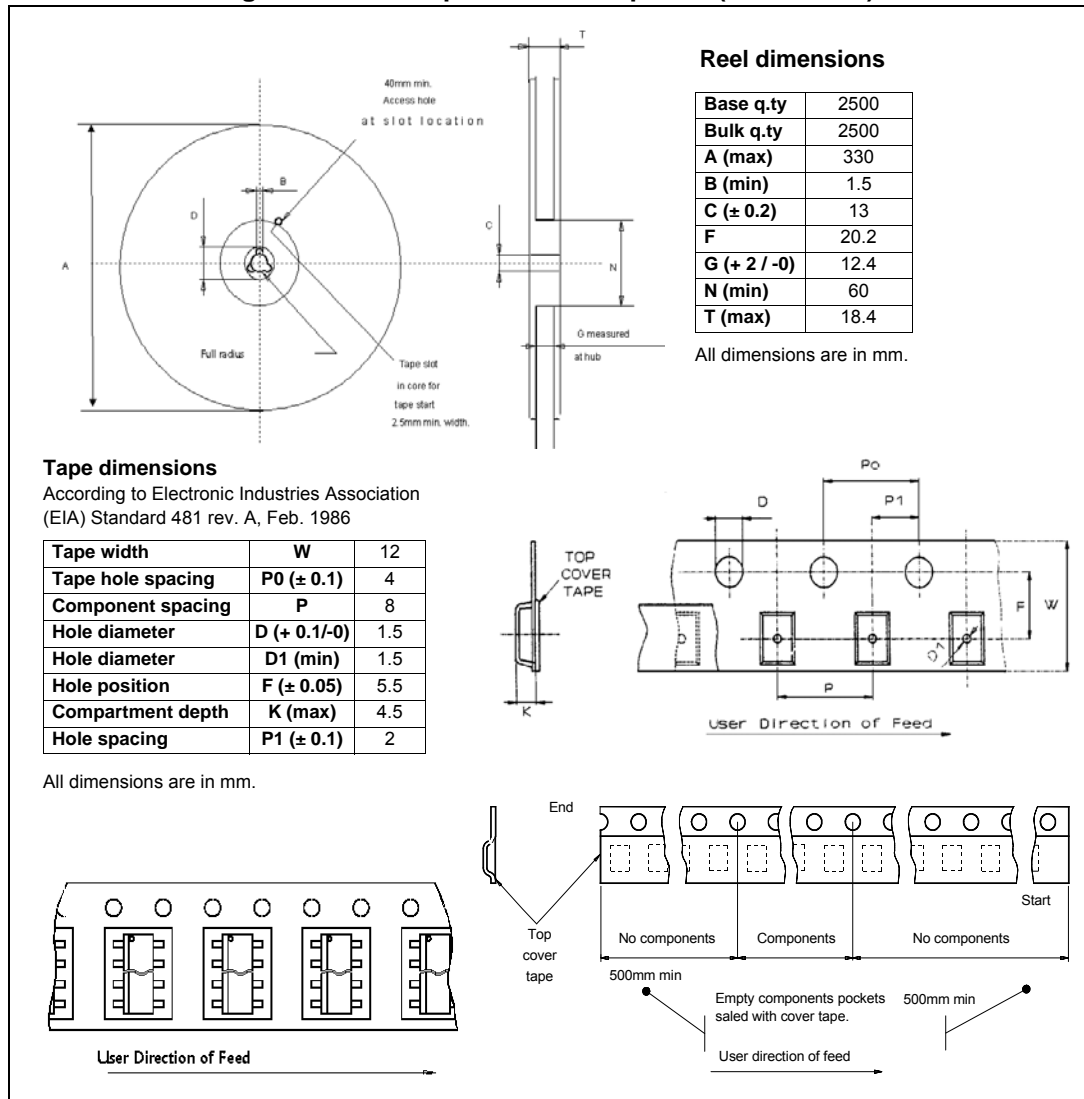
Table 8. SO-8 package mechanical data (continued)

Symbol	Millimeters		
	Min	Typ.	Max
E	5.80	6.00	6.20
E1 <sup>(2)</sup>	3.80	3.90	4.00
e		1.27	
h	0.25		0.50
L	0.40		1.27
L1		1.04	
k	0°		8°
ccc			0.10

1. Dimension D does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 mm in total (both side).
2. Dimension "E1" does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25 mm per side.

### 5.3 SO-8 packing information

Figure 26. SO-8 tape and reel shipment (suffix "TR")



## 6 Revision history

Table 9. Revision history

Date	Revision	Changes
18-Dec-2018	1	Initial release.
08-Apr-2019	2	Updated <i>Description</i> in cover page. Updated <i>Table 1: Device summary</i> . Updated <i>Section 3.1: Voltage regulator</i> .
15-Apr-2019	3	Deleted figure SO-8 tube shipment (no suffix).

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[T](#) [MAX663CPA](#) [NCV4269CPD50R2G](#) [NCV8716MT30TBG](#) [AZ1117IH-1.2TRG1](#) [MP2013GQ-P](#)