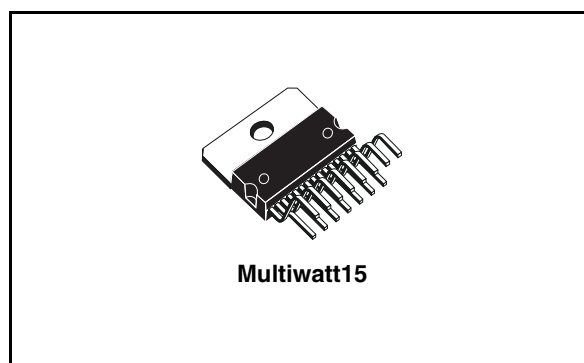

Multifunction voltage regulator for car radio

Features

- Four outputs
 - 8.5V @ 200mA (V8P5)
 - 8/10V @ 1000mA selectable 10V or 8V (V810)
 - 3.3V @ 100mA permanent (VSTBY)
 - 3.3V @ 800mA (VREGSW)
- Two protected high side driver (HSD1, HSD2)
- Reset function
- Battery voltage (under/over) warning output
- Load dump protection
- Independent thermal shutdown on all regulators and HSDs
- Overcurrent limitation
- Storage CAP output (STCAP)
- Small CAP required by stability of regulators
- All pins ESD protected



Description

The L5959 contains a four voltage regulator and two protected HSDs. HSDs are protected against loss of ground and loss of battery.

The IC includes a monitoring circuit for detection.

The IC features a very low quiescent current in stand-by and independent thermal shutdown.

Table 1. Device summary

Order code	Package	Packing
L5959	Multiwatt15	Tube

Contents

1	Block diagram	5
2	Pins description	6
	2.1 Pins connection	6
3	Electrical specification	7
	3.1 Absolute maximum ratings	7
	3.2 Thermal data	7
	3.3 Electrical characteristics	7
4	Timing diagrams	13
5	Package information	17
6	Revision history	18

List of tables

Table 1.	Device summary	1
Table 2.	Enable logic	5
Table 3.	Absolute maximum ratings	7
Table 4.	Thermal data	7
Table 5.	Electrical characteristics	7
Table 6.	Document revision history	18

List of figures

Figure 1.	Block diagram	5
Figure 2.	Pins connection (top view)	6
Figure 3.	Timing diagram of regulators and HSD	13
Figure 4.	STCAP and RST diagram.	13
Figure 5.	VBATVW (over/under voltage warning)	14
Figure 6.	Independent thermal shutdown	15
Figure 7.	RST glitch rejection.	16
Figure 8.	Enable on/off delay	16
Figure 9.	Multiwatt15 (vertical) mechanical data and package dimensions.	17

1 Block diagram

Figure 1. Block diagram

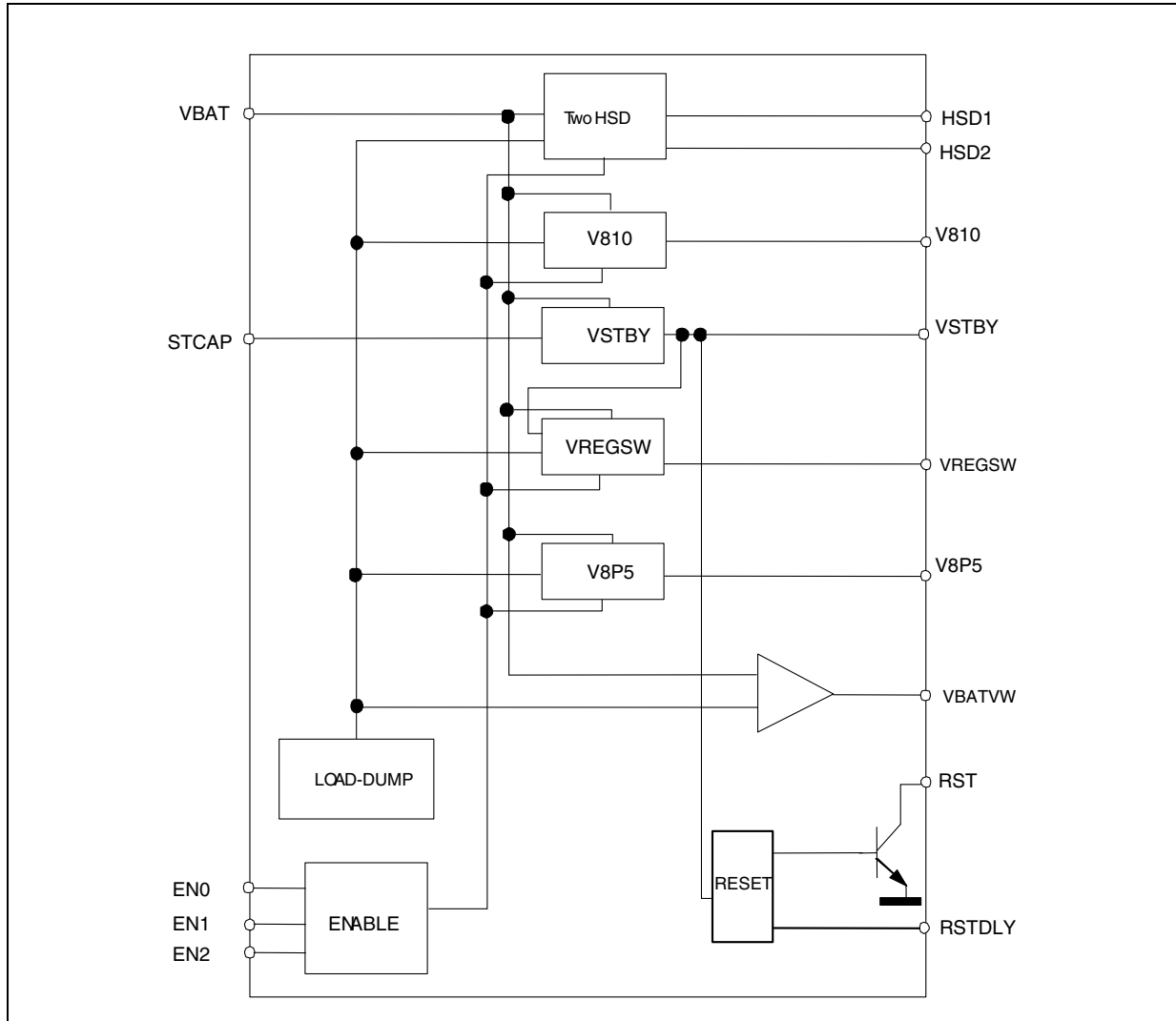


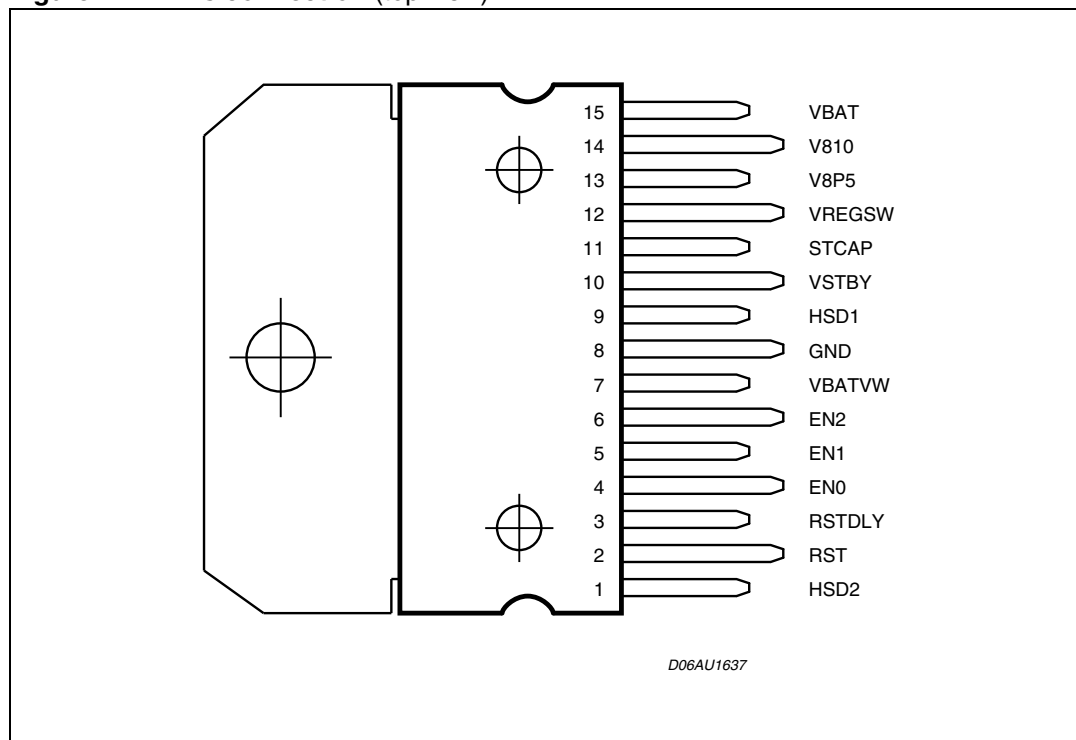
Table 2. Enable logic

EN2	EN1	EN0	VREGSW	V8P5	HSD1	V810 (8V)	V810 (10V)	HSD2
0	0	0	Off	Off	Off	Off	Off	Off
0	0	1	On	On	On	Off	On	On
0	1	0	On	Off	Off	Off	Off	Off
0	1	1	On	On	On	Off	Off	On
1	0	0	On	On	On	Off	Off	Off
1	0	1	On	On	On	Off	On	Off
1	1	0	On	On	On	On	Off	Off
1	1	1	On	On	On	On	Off	On

2 Pins description

2.1 Pins connection

Figure 2. Pins connection (top view)



3 Electrical specification

3.1 Absolute maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{BATDC}	DC operating supply voltage	30	V
V_{BATTR}	Transient supply voltage	50	V
I_O	Output current	internally limited	
R_{ESR}	Output capacitor series eq. resistance (MAX.)	0.5	Ω
T_{op}	Operating temperature range	-40 to 105	$^{\circ}C$
T_{stg}	Storage temperature	-55 to 150	$^{\circ}C$
T_j	Junction temperature	-55 to 150	$^{\circ}C$
P_d	Power dissipation $T_{case} = 85^{\circ}C$	43	W

3.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Multiwatt	Unit
$R_{th\ j-case}$	Thermal resistance junction to case max.	1.8	$^{\circ}C/W$

3.3 Electrical characteristics

Table 5. Electrical characteristics

($V_S = 14.4V$; $T_{amb} = 25^{\circ}C$; unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
INPUT SUPPLIES						
V_{bat}	Input supply	Operating	9		18	V
V_{STCAP}	Input supply voltage 2	Operating	6		18	V
V_{bat}	Battery voltage	Reverse polarity		non operating		
V_{STCAP}	Input supply voltage 2	Reverse polarity		non operating		
I_q	Total quiescent current	EN0 = EN1 = EN2 = 0 V; VBAT = 14 V; $I_{VSTBY} = 100\ \mu A$		55	75	μA
V_{OV}	VBAT Over-voltage shutdown	Verify all outputs except VSTBY disabled and VBATVW* asserted low (VBAT Rising)	24	27	30	V
V_{HYSOV}	Hysteresis of over-voltage shutdown		200	750	1500	mV

Table 5. Electrical characteristics (continued)
 ($V_S = 14.4V$; $T_{amb} = 25^{\circ}C$; unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{UV}	VBAT Under-voltage warning	Verify VBATVW* asserted low (VBAT Falling)	7	7.4	7.8	V
V_{HYSUV}	Hysteresis of under-voltage warning		70	300	500	mV
VSTBY						
V_o (VSTBY)	Output voltage of VSTBY		3.14	3.3	3.46	V
ΔV	Line regulation	$V_{BAT} = 6$ to $18V$; $I = 100mA$	-10	0	+10	mV
ΔV_i	Load regulation	$I_{VSTBY} = 0.5$ to 100 mA	-40	-5	+10	mV
V_{over}	Over shoot	$I_{VSTBY} = 100$ to 0.5 mA, $C_o = 1\mu F$		2.5	6	%
PSRR	Supply voltage ripple rejection	$I_{VSTBY} = 50$ mA; $f_o = 20$ to 1 kHz; $V_{BAT} = 14 V_{dc}, 1.0 V_{ac(pp)}$	50	70		dB
		$I_{VSTBY} = 50$ mA; $f_o = 20$ to 20 kHz; $V_{BAT} = 14 V_{dc}, 1.0 V_{ac(pp)}$	45	55		dB
V_N	Output noise	Weighted filter $f_o = 20$ Hz to 20 kHz $I_{VSTBY} = 5$ mA		85	200	μV
V_{drop}	Drop out voltage	$I_{VSTBY} = 100mA^{(1)}$			2.6	V
	Drop out voltage	$I_{VSTBY} = 5$ mA			2.3	V
I_m	Current limit	$R_{short} = 0\Omega$	150	200	300	mA
TS_{EN}	VSTBY thermal shutdown	$I_{VSTBY} = 500 \mu A$; Increase T_a until VSTBY disabled	150		190	$^{\circ}C$
VREGSW						
V_o (VREGSW)	Output voltage 3.3V		3.14	3.3	3.46	V
V_{TRK}	VREGSW output tracking voltage on VSTBY	$I_{VSTBY} = 50$ mA $I_{VREGSW} = 0.5$ to 800 mA Measure VSTBY – VREGSW	-40		40	mV
		$I_{VSTBY} = 0.5$ mA to 100 mA $I_{VREGSW} = 0.5$ to 800 mA Measure VSTBY – VREGSW	-50		50	mV
ΔV	Line regulation	$V_{in1} = 9$ to $18V$; $I = 800mA$	-40	10	40	mV
ΔV_i	Load regulation	$I_{VREGSW} = 1$ to $800mA$	-50	-15	10	mV

Table 5. Electrical characteristics (continued) $(V_S = 14.4V; T_{amb} = 25^{\circ}C; \text{ unless otherwise specified})$

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
PSRR	Supply voltage ripple rejection	$I_{VREGSW} = 400 \text{ mA};$ $f_o = 20 \text{ to } 1 \text{ kHz};$ $V_{BAT} = 14 V_{dc}, 1.0 V_{ac(pp)}$	50	70		dB
		$I_{VREGSW} = 400 \text{ mA};$ $f_o = 20 \text{ to } 20 \text{ kHz};$ $V_{BAT} = 14 V_{dc}, 1.0 V_{ac(pp)}$	45	55		dB
V_N	Output noise	Weighted filter $f_o = 20 \text{ Hz to } 20 \text{ kHz}$ $I_{VREGSW} = 5 \text{ mA}$		85	200	μV
V_{drop}	Drop out voltage	$I_{VREGSW} = 800 \text{ mA}$			2.6	V
V_{drop}	Drop out voltage	$I_{VREGSW} = 5 \text{ mA}$			2.3	V
I_m	Current limit	$R_{short} = 0\Omega$	1	1.5	2.5	A
TS_{EN}	VREGSW thermal shutdown	$I_{VREGSW} = 500 \mu\text{A};$ Increase T_a until VREGSW disabled	150		190	$^{\circ}\text{C}$
t_{don}	Turn-on delay;	$I_{vregsw} = 5 \text{ mA}$	10	45	110	μs
t_{doff}	Turn-off delay,	$I_{VREGSW} = 700 \text{ mA}$		45	110	μs
V8P5 ($V_{BAT} = 9.5V \text{ to } 18V$)						
V_o (V8P5)	Output voltage 8.5V		8.3	8.5	8.7	V
ΔV	Line regulation	$V_{BAT} = 9.5 \text{ to } 18V; I = 200 \text{ mA}$	-50	3.0	50	mV
ΔV_i	Load regulation	$I_{V8P5} = 1 \text{ to } 200 \text{ mA}$	-30	3	20	mV
PSRR	Supply voltage ripple rejection	$I_{V8P5} = 100 \text{ mA};$ $f_o = 20 \text{ to } 1 \text{ kHz};$ $V_{BAT} = 14 V_{dc}, 1.0 V_{ac(pp)}$	50	60		dB
		$I_{V8P5} = 100 \text{ mA};$ $f_o = 20 \text{ to } 20 \text{ kHz};$ $V_{BAT} = 14 V_{dc}, 1.0 V_{ac(pp)}$	35	40		dB
V_N	Output noise	Weighted filter $f_o = 20 \text{ Hz to } 20 \text{ kHz}$ $I_{V8P5} = 5 \text{ mA}$		190	450	μV
V_{drop}	Drop out voltage	$I_{V8P5} = 200 \text{ mA}$		0.45	0.9	V
I_m	Current limit	$R_{short} = 0\Omega$	275	450	700	mA
TS_{EN}	V8P5 thermal shutdown	$I_{V8P5} = 500 \mu\text{A};$ Increase T_a until V8P5 disabled	150		190	$^{\circ}\text{C}$
t_{don}	Turn-on delay;	$I_{V8P5} = 5 \text{ mA}$	10	45	110	μs
t_{doff}	Turn-off delay,	$I_{V8P5} = 200 \text{ mA}$		45	110	μs
V810 (8V) ($V_{BAT} = 9.2V \text{ to } 18V$)						
V_o (V810)	Output voltage 8.0V		7.6	8.0	8.4	V
ΔV	Line regulation	$V_{BAT} = 9.2 \text{ to } 18V;$ $I = 1000 \text{ mA}$	-50	3	50	mV

Table 5. Electrical characteristics (continued)

 $(V_S = 14.4V; T_{amb} = 25^\circ C; \text{ unless otherwise specified})$

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
ΔV_i	Load regulation	$I_{V810} = 0.5 \text{ to } 1000 \text{ mA}$	-100	-20	10	mV
PSRR	Supply voltage ripple rejection	$I_{V810} = 500 \text{ mA};$ $f_o = 20 \text{ to } 1 \text{ kHz};$ $V_{BAT} = 14 V_{dc}, 1.0 V_{ac(pp)}$	50	55		dB
		$I_{V810} = 500 \text{ mA};$ $f_o = 20 \text{ to } 20 \text{ kHz};$ $V_{BAT} = 14 V_{dc}, 1.0 V_{ac(pp)}$	30	35		dB
V_N	Output noise	Weighted filter $f_o = 20 \text{ Hz to } 20 \text{ kHz}$ $I_{V810} = 5 \text{ mA}$		175	450	μV
Vdrop	Drop out voltage	$I_{V810(8V)} = 1000\text{mA}^{(1)}$		0.45	0.9	V
I_m	Current limit	$R_{short} = 0\Omega$	1.5	2.3	3.5	A
TS _{EN}	V810(8V) thermal shutdown	$I_{V810(8V)} = 500 \mu A;$ Increase T_a until V810(8V) disabled	150		190	$^\circ C$
t_{don}	Turn-on delay;	$I_{V810(8V)} = 5\text{mA}$	10	45	110	μs
t_{doff}	Turn-off delay,	$I_{V810(8V)} = 1000 \text{ mA}$		45	110	μs
V810 (10V) ($V_{BAT}=11.2V \text{ to } 18 V$)						
V_o (V810)	Output Voltage 10.0V		9.5	10.0	10.5	V
ΔV	Line regulation	$V_{BAT} = 11.2 \text{ to } 18V; I = 1000\text{mA}$	-50	2.5	50	mV
ΔV_i	Load regulation	$I_{V810} = 0.5 \text{ to } 1000 \text{ mA}$	-100	-25	10	mV
PSRR	Supply voltage ripple rejection	$I_{V810} = 500 \text{ mA};$ $f_o = 20 \text{ to } 1 \text{ kHz};$ $V_{BAT} = 14 V_{dc}, 1.0 V_{ac(pp)}$	50	55		dB
		$I_{V810} = 500 \text{ mA};$ $f_o = 20 \text{ to } 20 \text{ kHz};$ $V_{BAT} = 14 V_{dc}, 1.0 V_{ac(pp)}$	30	35		dB
V_N	Output noise	Weighted filter $f_o = 20 \text{ Hz to } 20 \text{ kHz}$ $I_{V810} = 5 \text{ mA}$		175	450	μV
Vdrop	Drop out voltage	$I_{V810(10V)} = 1000\text{mA}^{(1)}$		0.4	0.9	V
I_m	Current limit	$R_{short} = 0\Omega$	1.5	2.3	3.5	A
TS _{EN}	V810(10V) thermal shutdown	$I_{V810(8V)} = 500 \mu A;$ Increase T_a until V810(10V) disabled	150		190	$^\circ C$
t_{don}	Turn-on delay;	$I_{V810(8V)} = 5\text{mA}$	10	45	110	μs
t_{doff}	Turn-off delay,	$I_{V810(8V)} = 1000 \text{ mA}$		45	110	μs
HIGH SIDE DRIVER1						
VdropSW	Drop voltage HDS1	$I_{dc} = 100\text{mA}$		0.25	0.6	V
		$I_{dc} = 200\text{mA}, t = 5S$		0.50	1.2	V

Table 5. Electrical characteristics (continued)
 ($V_S = 14.4V$; $T_{amb} = 25^\circ C$; unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
I_{STG}	HSD1 short to ground current	VHSD1=0V	240	300	400	mA
I_{STB}	HSD1 short to V_{BAT} current	VHSD1= V_{BAT}		2	10	mA
$\Delta I_{Q(VBAT)}$	HSD1 bias current change	$I_{HSD1} = 0$ to 100 mA; Measure change in V_{BAT} current		0.15	10	mA
T_{SEN}	HSD1 thermal shutdown	$I_{HSD1} = 500 \mu A$; Increase T_a until HSD1 disabled	150		190	$^\circ C$
t_{don}	Turn-on delay;	$I_{HSD1} = 10mA$	10	50	110	μs
t_{doff}	Turn-off delay,	$I_{HSD1} = 100 mA$		70	110	μs
t_r	Rise time	10% to 90%, $I_{HSD1} = 10mA$		35	75	μs
HIGH SIDE DRIVER2						
V_{dropSW}	Drop voltage HDS2	$I_{dc} = 300mA$		0.2	0.6	V
		$I_{dc} = 450mA, t=5S$		0.3	1.2	V
I_{STG}	HSD2 short to ground current	VHSD2=0V	0.55	0.75	1	A
I_{STB}	HSD2 short to V_{BAT} current	VHSD2= V_{BAT}		3.5	10	mA
$\Delta I_{Q(VBAT)}$	HSD2 bias current change	$I_{HSD2} = 0$ to 300 mA; Measure change in V_{BAT} current		0.15	10	mA
T_{SEN}	HSD2 thermal shutdown	$I_{HSD2} = 500 \mu A$; Increase T_a until HSD2 disabled	150		190	$^\circ C$
t_{don}	Turn-on delay;	$I_{HSD2} = 10mA$	10	45	110	μs
t_{doff}	Turn-off delay,	$I_{HSD2} = 300 mA$		70	110	μs
t_r	Rise time	10% to 90%, $I_{HSD2} = 10mA$		30	75	μs
RST (open collector output)						
V_{TH}	VSTBY reset threshold	Force VSTBY low until RST* asserted	0.93 * VSTBY	0.95 * VSTBY	0.97 * VSTBY	V
V_{HYS}	Hysteresis of reset on rising VSTBY		10	50	200	mV
t_{rRST}	Rise time	10% to 90%, $R_{RST} = 47 k\Omega$, $C_{RST} = 50 pF$		20	30	μs
t_{fRST}	Fall time	90% to 10%, $R_{RST} = 47 k\Omega$, $C_{RST} = 50 pF$		300	1000	ns
V_{IH_RSTDLY}	RSTDLY input voltage threshold	Verify RST is de asserted	2.5	2.75	3.5	V
I_{SRC}	RSTDLY current	RSTDLY = 0 VDC	6	8.5	12	μA

Table 5. Electrical characteristics (continued) $(V_S = 14.4V; T_{amb} = 25^{\circ}C; \text{ unless otherwise specified})$

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
t_{por}	RST POR delay time	$C_{RSTDLY} = 0.1 \mu F$	20	30	50	ms
T_{glitch}	Glitch rejection filter time		5	12.5	20	μs
ENABLE INPUT (VREGSW, V8P5, V810, HSD1, HSD2)						
V_{IH}	Threshold recognized as high level				2.0	V
V_{IL}	Threshold recognized as low level		0.8			V
V_{HYSEN}	Hysteresis of enable		0.15	0.35		V
I_{LKGEN}	Enable input pull-down current	$V_{EN} = V_{IL(min)} \text{ to } V_{STBY}$	10	30	50	μA

1. Drop condition means that the supply voltage drop down to 100 mV from the regulated output and the regulator is sourcing its maximal load.
2. Stability Request is design info, not tested.

4 Timing diagrams

Figure 3. Timing diagram of regulators and HSD

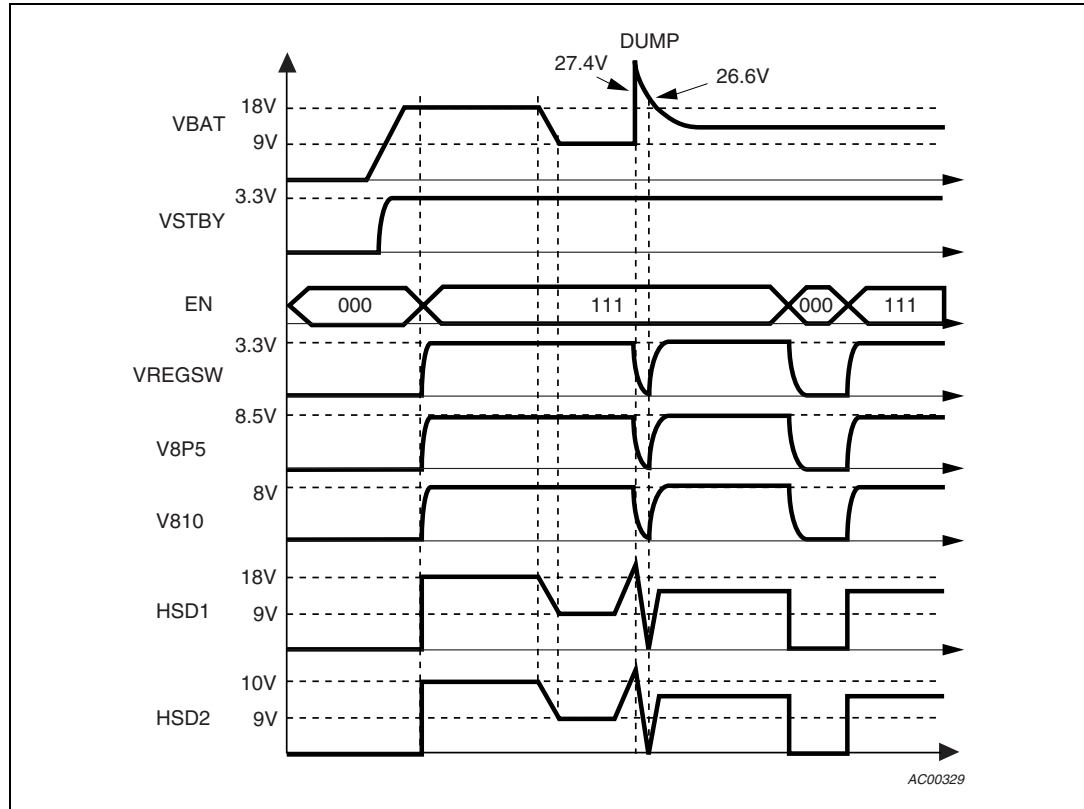


Figure 4. STCAP and RST diagram

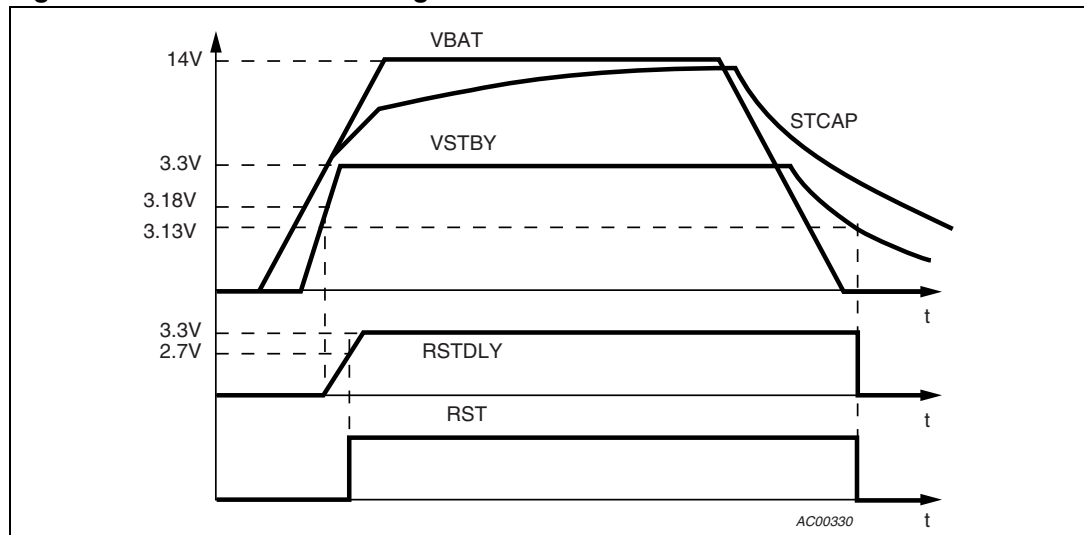


Figure 5. VBATVW (over/under voltage warning)

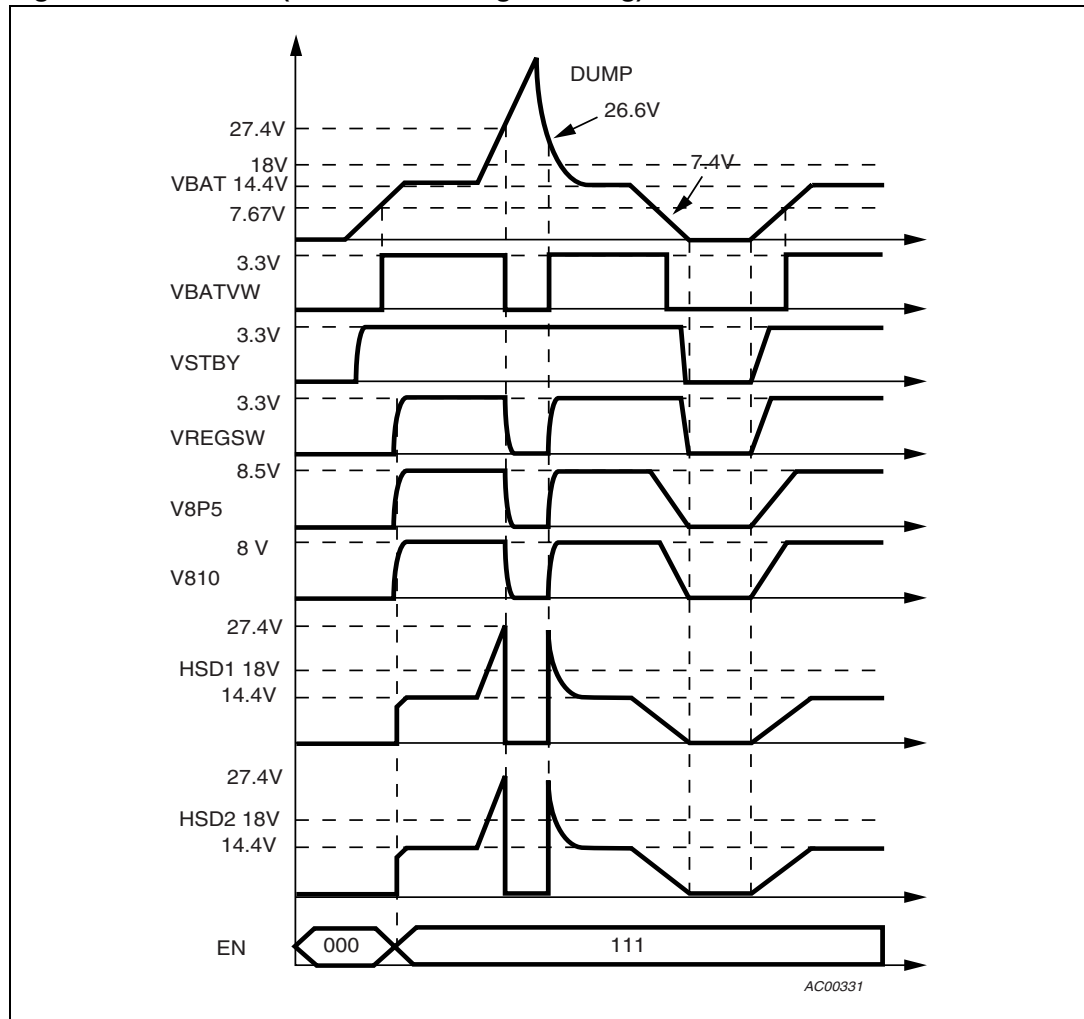


Figure 6. Independent thermal shutdown

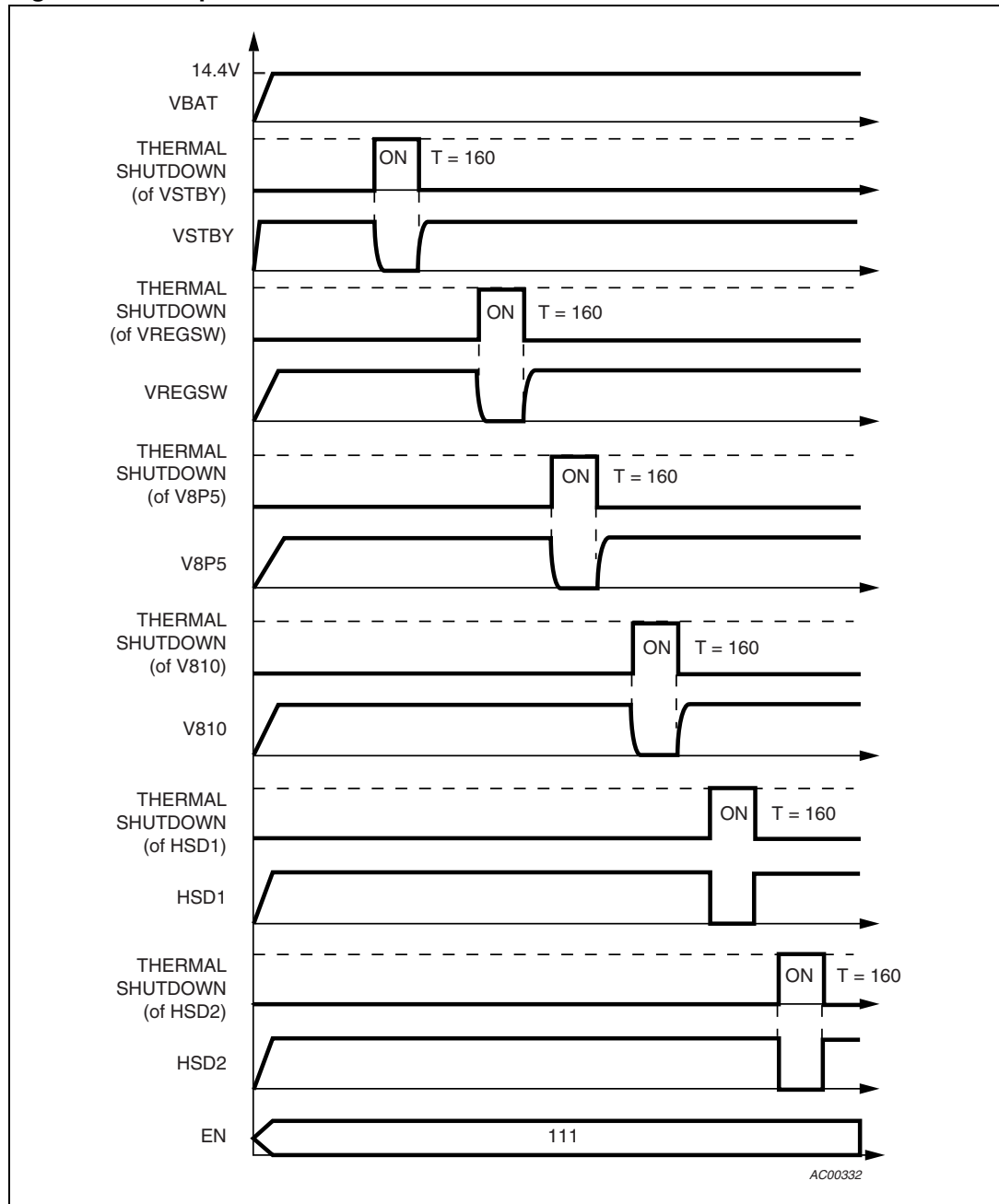


Figure 7. RST glitch rejection

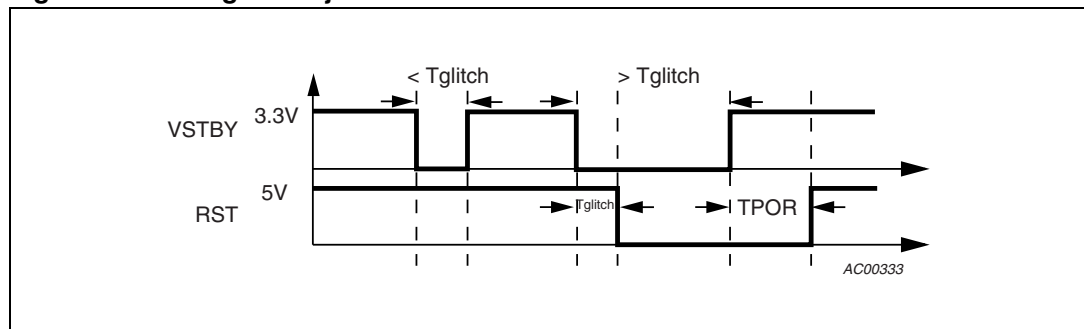
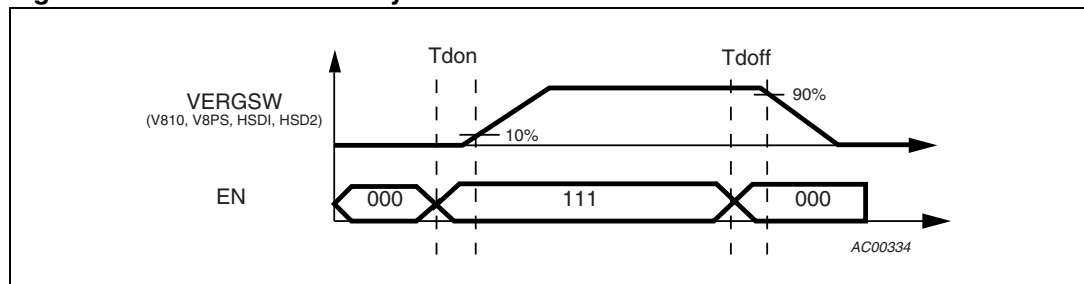


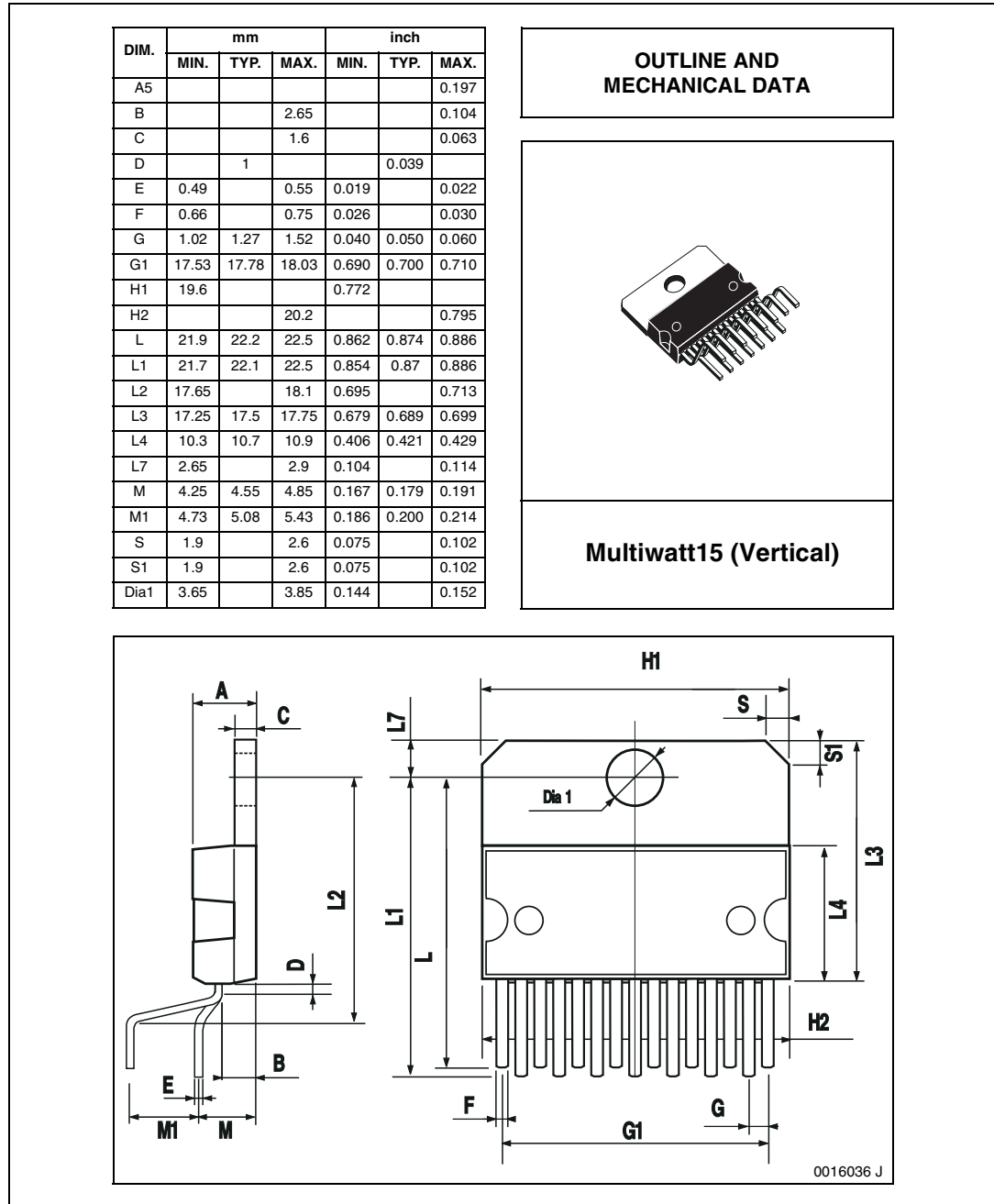
Figure 8. Enable on/off delay



5 Package information

In order to meet environmental requirements, ST offers these devices in ECOPACK[®] packages. These packages have a Lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Figure 9. Multiwatt15 (vertical) mechanical data and package dimensions



6 Revision history

Table 6. Document revision history

Date	Revision	Changes
26-Jun-2006	1	Initial release.
28-Aug-2007	2	Minor changes, improved quality of the drawings.
17-Sep-2013	3	Updated Disclaimer.

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