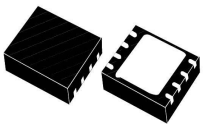
L5983

1.5 A step-down switching regulator

Datasheet - production data



VFQFPN8 3 x 3 mm

Features

- 1.5 A DC output current
- 2.9 V to 18 V input voltage
- Output voltage adjustable from 0.6 V
- 250 kHz switching frequency, programmable up to 1 MHz
- Internal soft-start and inhibit
- Low dropout operation: 100% duty cycle
- Voltage feedforward
- Zero load current operation
- Overcurrent and thermal protection
- VFQFPN8 3 x 3 mm package

Applications

- Consumer: STB, DVD, DVD recorder, car audio, LCD TV and monitors
- Industrial: chargers, PLD, PLA, FPGA
- Networking: XDSL, modems, DC-DC modules
- Computer: optical storage, hard disk drive, printers, audio/graphic cards
- LED driving

Description

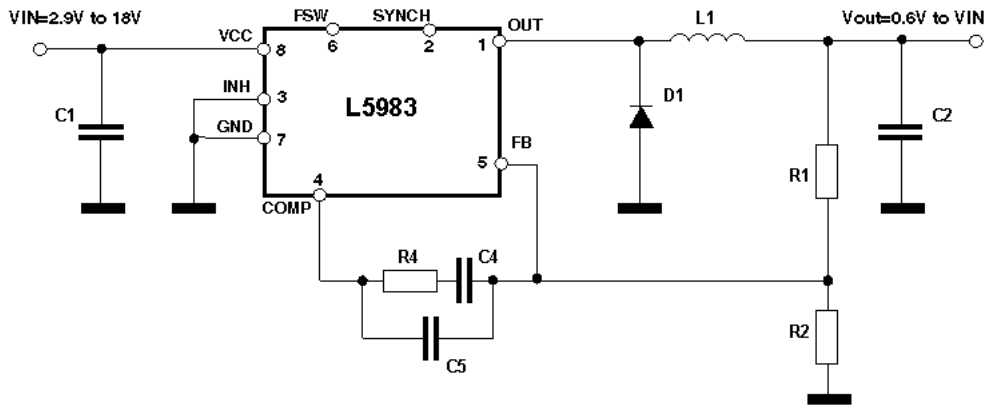
The L5983 is a step-down switching regulator with a 2.0 A (min.) current limited embedded Power MOSFET, so it is able to deliver an output current in excess of 1.5 A DC to the load.

The input voltage can range from 2.9 V to 18 V, while the output voltage can be set starting from 0.6 V to V_{IN}. Having a minimum input voltage of 2.9 V, the device is suitable also for a 3.3 V bus.

Requiring a minimum set of external components, the device includes an internal 250 kHz switching frequency oscillator that can be externally adjusted up to 1 MHz.

The VFQFPN package with an exposed pad allows reducing the R_{thJA} down to approximately 60 °C/W.

Figure 1. Application circuit

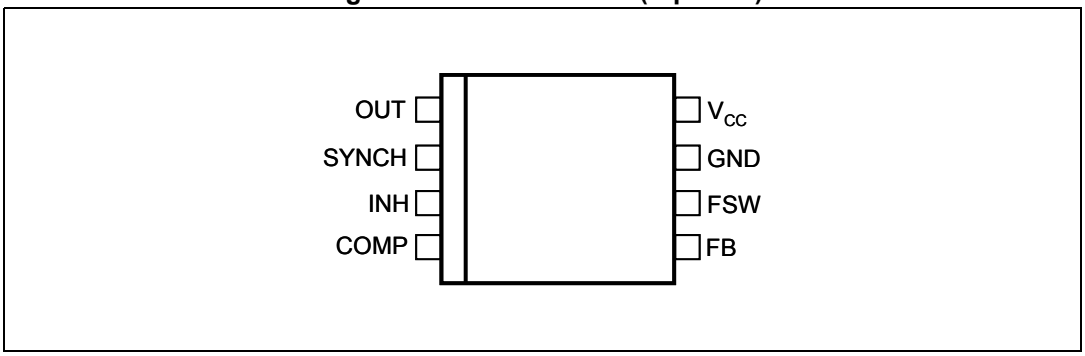


Contents

1 Pin settings

1.1 Pin connection

Figure 2. Pin connection (top view)



1.2 Pin description

Table 1. Pin description

No.	Type	Description
1	OUT	Regulator output
2	SYNCH	Master/slave synchronization. When it is left floating, a signal with a phase shift of half a period with respect to the power turn-on is present at the pin. When connected to an external signal at a frequency higher than the internal one, then the device is synchronized by the external signal, with zero phase shift. Connecting together the SYNCH pin of two devices, the one with the higher frequency works as a master and the other as a slave; so the turn-on of the two power switches has a phase shift of half a period.
3	INH	A logical signal (active high) disables the device. With INH higher than 1.9 V the device is OFF and with INH lower than 0.6 V the device is ON.
4	COMP	Error amplifier output to be used for loop frequency compensation
5	FB	Feedback input. Connecting the output voltage directly to this pin the output voltage is regulated at 0.6 V. To have higher regulated voltages an external resistor divider is required from the Vout to the FB pin.
6	F_{SW}	The switching frequency can be increased connecting an external resistor from the FSW pin and ground. If this pin is left floating the device works at its free running frequency of 250 kHz.
7	GND	Ground
8	V_{CC}	Unregulated DC input voltage

2 Maximum ratings

2.1 Absolute maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Input voltage	20	V
OUT	Output DC voltage	-0.3 to V_{CC}	
F_{SW}, COMP, SYNCH	Analog pin	-0.3 to 4	
INH	Inhibit pin	-0.3 to V_{CC}	
FB	Feedback voltage	-0.3 to 1.5	
P_{TOT}	Power dissipation at T_A < 60 °C	1.5	W
T_J	Junction temperature range	-40 to 150	°C
T_{stg}	Storage temperature range	-55 to 150	°C

2.2 Thermal data

Table 3. Thermal data

Symbol	Parameter		Value	Unit
R_{thJA}	Maximum thermal resistance junction ambient(1)	VFQFPN	60	°C/W

1. Package mounted on demonstration board.

3 Electrical characteristics

T_J = 25 °C, V_{CC} = 12 V, unless otherwise specified.

Table 4. Electrical characteristics

Symbol	Parameter	Test condition	Values			Unit
			Min.	Typ.	Max.	
V_{CC}	Operating input voltage range	(1)	2.9		18	V
V_{CCON}	Turn-on V_{CC} threshold	(1)			2.9	
V_{CCHYS}	V_{CC} UVLO hysteresis	(1)	0.175		0.3	
$R_{DS(on)}$	MOSFET on resistance			140	170	mΩ
		(1)		140	220	
I_{LIM}	Maximum limiting current		2.0	2.3	2.6	A
Oscillator						
F_{SW}	Switching frequency		225	250	275	kHz
		(1)	220		275	
V_{FSW}	FSW pin voltage			1.254		V
D	Duty cycle		0		100	%
F_{ADJ}	Adjustable switching frequency	R_{FSW} = 33 kΩ		1000		kHz
Dynamic characteristics						
V_{FB}	Feedback voltage	2.9 V < V_{CC} < 18 V(1)	0.593	0.6	0.607	V
	DC characteristics					
I_Q	Quiescent current	Duty cycle = 0, V_{FB} = 0.8 V			2.4	mA
I_{QST-BY}	Total standby quiescent current			20	30	µA
Inhibit						
	INH threshold voltage	Device ON level			0.6	V
		Device OFF level	1.9			
	INH current	INH = 0		7.5	10	µA
Soft-start						
T_{SS}	Soft-start duration	FSW pin floating	7.4	8.2	9.1	ms
		F_{SW} = 1 MHz, R_{FSW} = 33 kΩ		2		
Error amplifier						
V_{CH}	High level output voltage	V_{FB} < 0.6 V	3			V
V_{CL}	Low level output voltage	V_{FB} > 0.6 V			0.1	
I_{FB}	Bias source current	V_{FB} = 0 V to 0.8 V		1		µA

Table 4. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Values			Unit
			Min.	Typ.	Max.	
$I_{O\ SOURCE}$	Source COMP pin	V_{FB} = 0.5 V, V_{COMP} = 1 V		20		mA
$I_{O\ SINK}$	Sink COMP pin	V_{FB} = 0.7 V, V_{COMP} = 1 V		25		mA
G_V	Open loop voltage gain	(2)		100		dB
Synchronization function						
	High input voltage		2		3.3	V
	Low input voltage				1	
	Slave sink current	V_{SYNCH} = 2.9 V		0.7	0.9	mA
	Master output amplitude	I_{SOURCE} = 4.5 mA	2.0			V
	Output pulse width	SYNCH floating		110		ns
	Input pulse width		70			
Protection						
I_{FBDISC}	FB disconnection source current			1		µA
T_{SHDN}	Thermal shutdown			150		°C
	Hysteresis			30		

1. Specification referred to T_J from -40 to +125 °C. Specifications in the -40 to +125 °C temperature range are assured by design, characterization and statistical correlation.
2. Guaranteed by design.

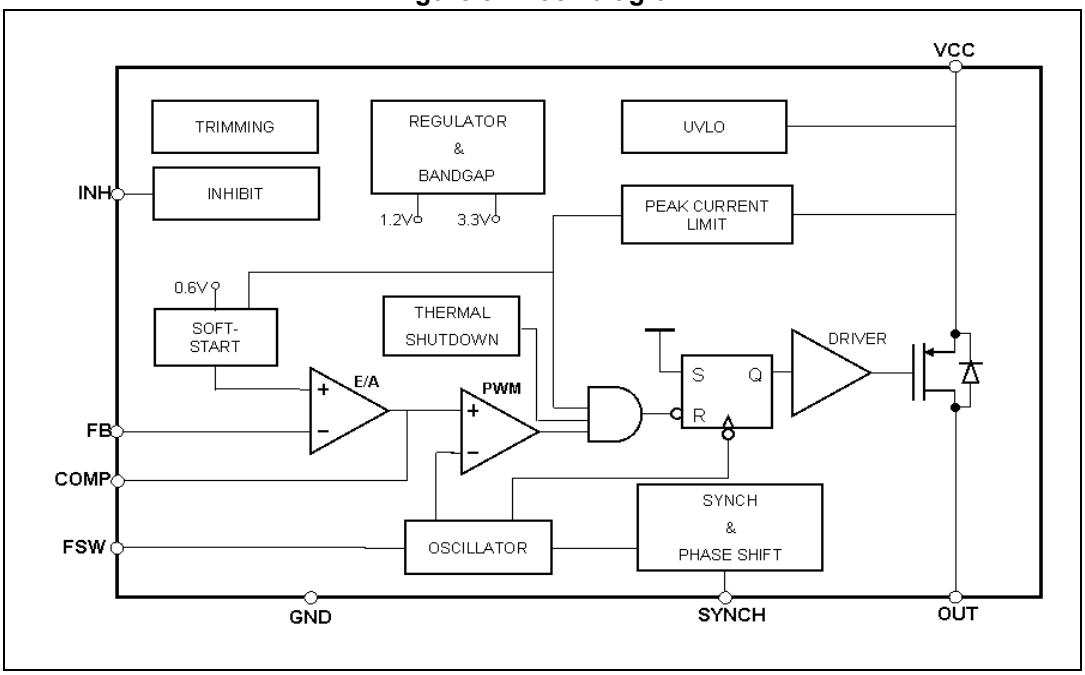
4 Functional description

The L5983 device is based on a “voltage mode”, constant frequency control. The output voltage V_{OUT} is sensed by the feedback pin (FB) compared to an internal reference (0.6 V) providing an error signal that, compared to a fixed frequency sawtooth, controls the ON and OFF time of the power switch.

The main internal blocks are shown in the block diagram in *Figure 3*. They are:

- A fully integrated oscillator that provides sawtooth to modulate the duty cycle and the synchronization signal. Its switching frequency can be adjusted by an external resistor. The voltage and frequency feedforward are implemented.
- The soft-start circuitry to limit inrush current during the startup phase
- The voltage mode error amplifier
- The pulse width modulator and the relative logic circuitry necessary to drive the internal power switch
- The high-side driver for embedded P-channel Power MOSFET switch
- The peak current limit sensing block, to handle overload and short-circuit conditions
- A voltage regulator and internal reference. It supplies internal circuitry and provides a fixed internal reference.
- A voltage monitor circuitry (UVLO) that checks the input and internal voltages.
- A thermal shutdown block, to prevent thermal runaway.

Figure 3. Block diagram



4.1 Oscillator and synchronization

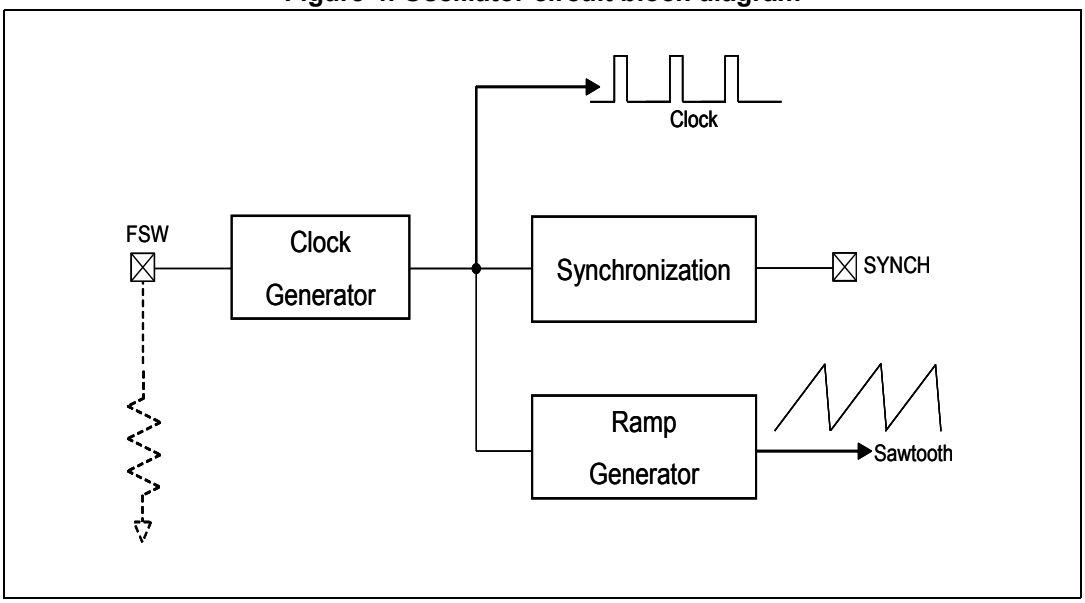
Figure 4 shows the block diagram of the oscillator circuit. The internal oscillator provides a constant frequency clock. Its frequency depends on the resistor externally connected to the FSW pin. In case the FSW pin is left floating the frequency is 250 kHz; it can be increased as shown in *Figure 6* by the external resistor connected to ground.

To improve the line transient performance, keeping the PWM gain constant versus the input voltage, the voltage feedforward is implemented by changing the slope of the sawtooth according to the input voltage change (see *Figure 5*.a).

The slope of the sawtooth also changes if the oscillator frequency is increased by the external resistor. In this way a frequency feedforward is implemented (*Figure 5*.b) in order to keep the PWM gain constant versus the switching frequency (see *Section 5.4 on page 18* for PWM gain expression).

The synchronization signal is generated on the SYNCH pin. This signal has a phase shift of 180° with respect to the clock. This delay is useful when two devices are synchronized connecting the SYNCH pins together. When SYNCH pins are connected, the device with a higher oscillator frequency works as a master, so the slave device switches at the frequency of the master but with a delay of half a period. This minimizes the RMS current flowing through the input capacitor (see the L5988D datasheet: *"4 A continuous (more than 5 A pulsed) step-down switching regulator with synchronous rectification*").

Figure 4. Oscillator circuit block diagram



The device can be synchronized to work at a higher frequency feeding an external clock signal. The synchronization changes the sawtooth amplitude, changing the PWM gain (*Figure 5*.c). This change has to be taken into account when the loop stability is studied. To minimize the change of the PWM gain, the free running frequency should be set (with a resistor on the FSW pin) only slightly lower than the external clock frequency. This pre-adjusting of the frequency changes the sawtooth slope in order to render the truncation of sawtooth negligible, due to the external synchronization.

Figure 5. Sawtooth: voltage and frequency feedforward; external synchronization

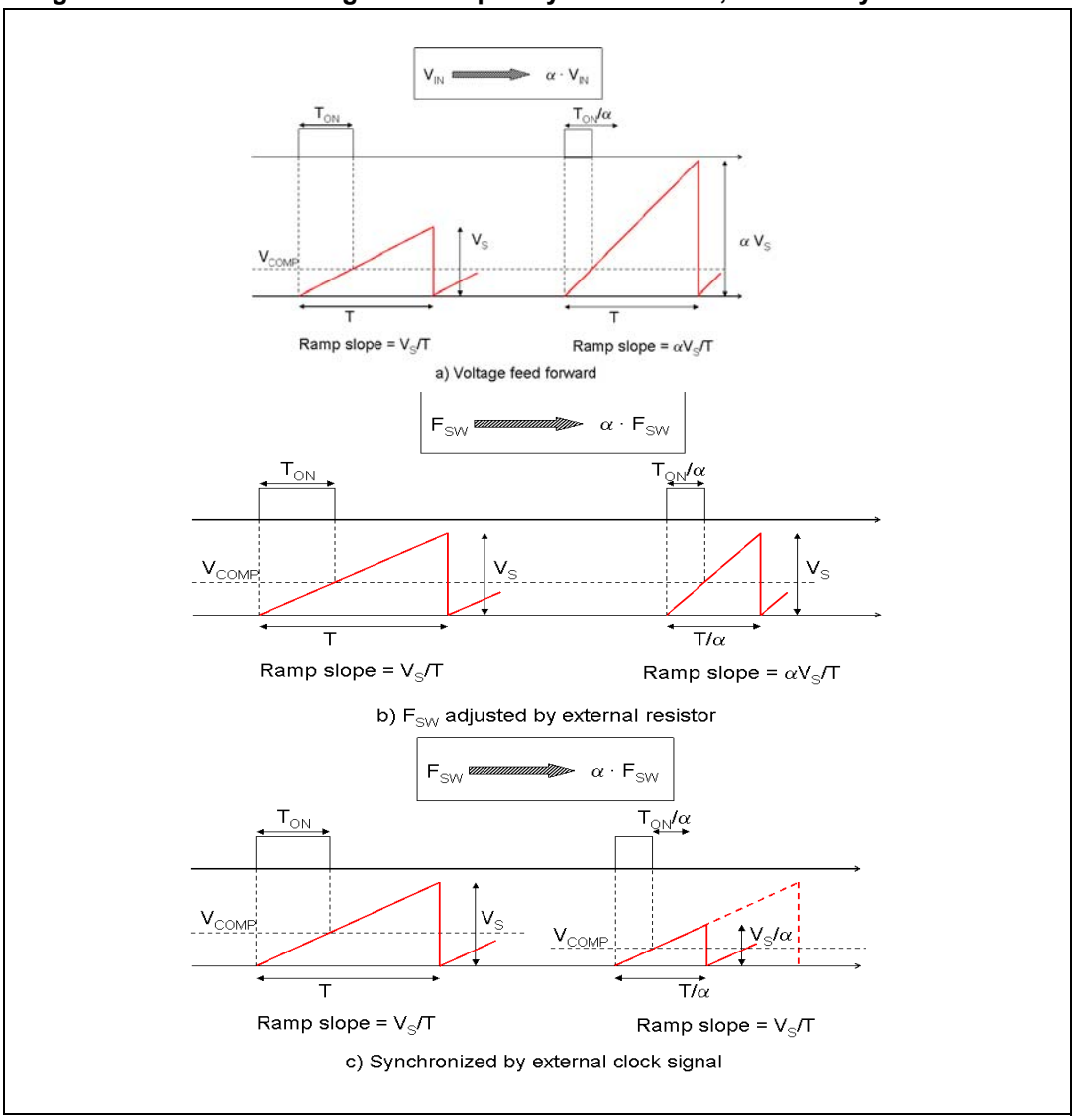
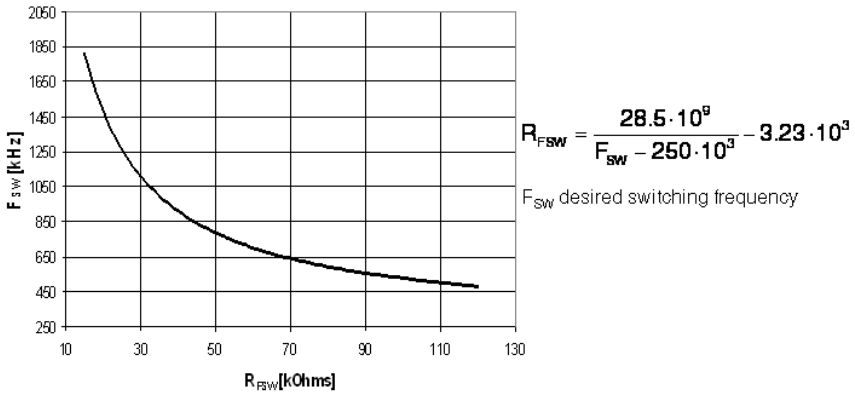


Figure 6. Oscillator frequency vs. FSW pin resistor



4.2 Soft-start

The soft-start is essential to assure a correct and safe startup of the step-down converter. It avoids inrush current surge and makes the output voltage increase monotonically.

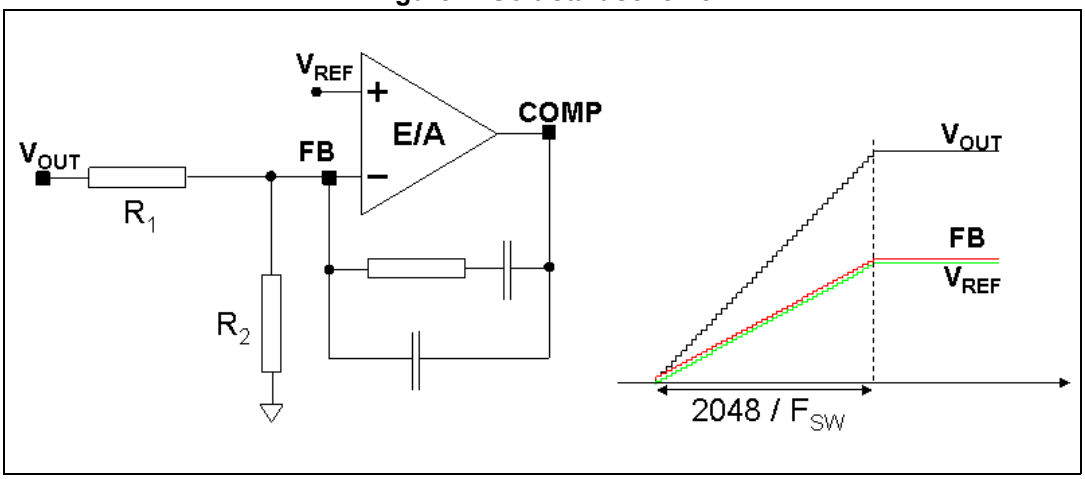
The soft-start is performed by a staircase ramp on the non-inverting input (V_{REF}) of the error amplifier. So the output voltage slew rate is:

Equation 1

$$SR_{OUT} = SR_{VREF} \cdot \left(1 + \frac{R1}{R2}\right)$$

where SR_{VREF} is the slew rate of the non-inverting input, while *R1* and *R2* is the resistor divider to regulate the output voltage (see *Figure 7*). The soft-start staircase consists of 64 steps of 9.5 mV each, from 0 V to 0.6 V. The time base of one step is of 32 clock cycles. So the soft-start time and then the output voltage slew rate depend on the switching frequency.

Figure 7. Soft-start scheme



Soft-start time results:

Equation 2

$$SS_{TIME} = \frac{32 \cdot 64}{Fsw}$$

For example, with a switching frequency of 250 kHz the SS_{TIME} is 8 ms.

4.3 Error amplifier and compensation

The error amplifier (E/A) provides the error signal to be compared with the sawtooth to perform the pulse width modulation. Its non-inverting input is internally connected to a 0.6 V voltage reference, while its inverting input (FB) and output (COMP) are externally available for feedback and frequency compensation. In this device the error amplifier is a voltage mode operational amplifier so with high DC gain and low output impedance.

The uncompensated error amplifier characteristics are the following:

Table 5. Uncompensated error amplifier characteristics

Error amplifier	Value
Low frequency gain	100 dB
GBWP	4.5 MHz
Slew rate	7 V/µs
Output voltage swing	0 to 3.3 V
Maximum source/sink current	25 mA/40 mA

In continuous conduction mode (CCM), the transfer function of the power section has two poles due to the LC filter and one zero due to the ESR of the output capacitor. Different kinds of compensation networks can be used depending on the ESR value of the output capacitor. In case the zero introduced by the output capacitor helps to compensate the double pole of the LC filter a type II compensation network can be used. Otherwise, a type III compensation network has to be used (see *Section 5.4 on page 18* for details of the compensation network selection).

However, the methodology to compensate the loop is to introduce zeros to obtain a safe phase margin.

4.4 Overcurrent protection

The L5983 device implements the overcurrent protection sensing current flowing through the Power MOSFET. Due to the noise created by the switching activity of the Power MOSFET, the current sensing is disabled during the initial phase of the conduction time. This avoids an erroneous detection of a fault condition. This interval is generally known as “masking time” or “blanking time”. The masking time is about 200 ns.

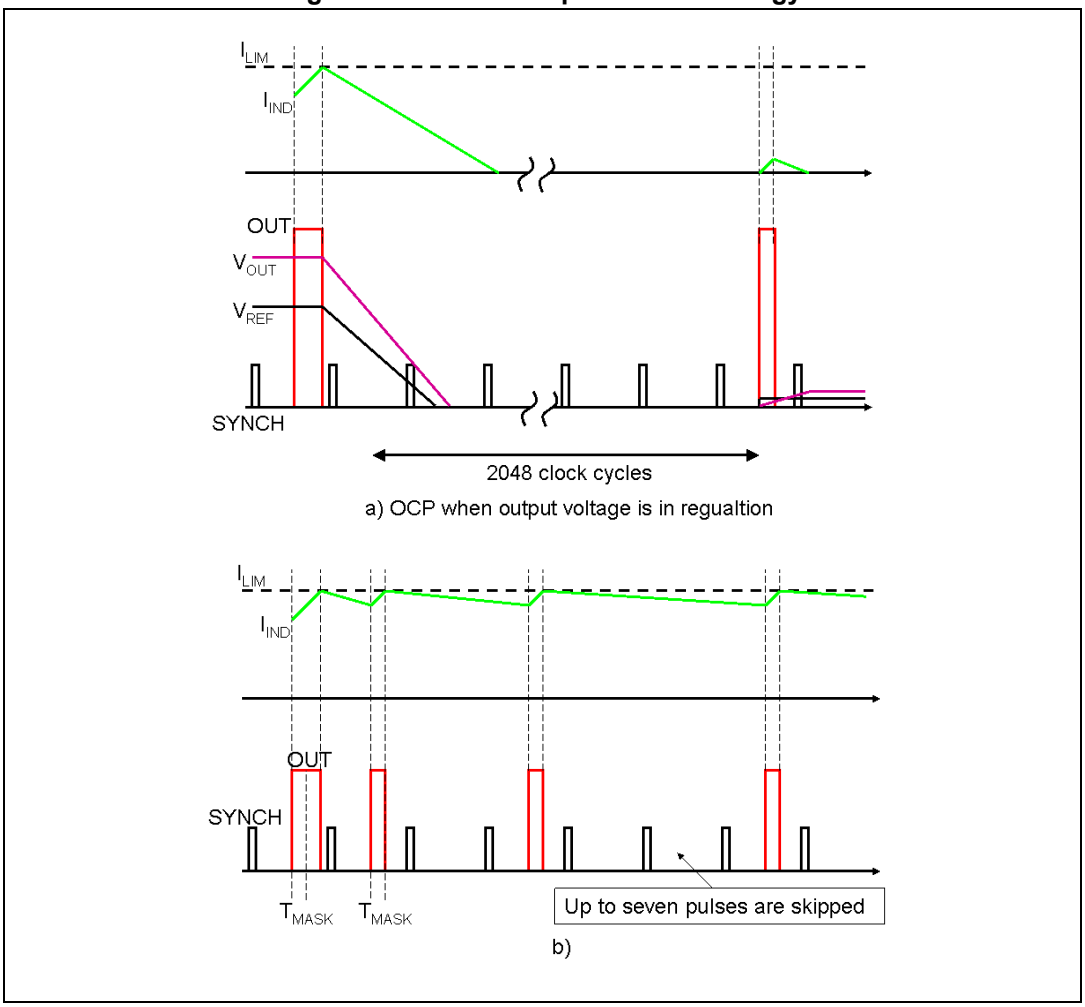
When the overcurrent is detected, two different behaviors are possible depending on the operating condition.

1. **Output voltage in regulation**. When the overcurrent is sensed, the Power MOSFET is switched off and the internal reference (V_{REF}), that biases the non-inverting input of the error amplifier, is set to zero and kept in this condition for a soft-start time (T_{SS}, 2048 clock cycles). After this time, a new soft-start phase takes place and the internal reference begins ramping (see *Figure 8*.a).
2. **Soft-start phase**. If the overcurrent limit is reached, the Power MOSFET is turned off implementing the pulse by pulse overcurrent protection. During the soft-start phase, under the overcurrent condition, the device can skip pulses in order to keep the output current constant and equal to the current limit. If, at the end of the “masking time”, the current is higher than the overcurrent threshold, the Power MOSFET is turned off and it skips one pulse. If, at the next switching on at the end of the “masking time”, the current is still higher than the threshold, the device skips two pulses. This mechanism is repeated and the device can skip up to seven pulses. While, if at the end of the “masking time” the current is lower than the overcurrent threshold, the number of skipped cycles is decreased by one unit. At the end of the soft-start phase the output voltage is in regulation and if the overcurrent persists, the behavior explained above takes place (see *Figure 8*.b).

So the overcurrent protection can be summarized as a “hiccup” intervention when the output is in regulation and a constant current during the soft-start phase.

If the output is shorted to ground when the output voltage is in regulation, the overcurrent is triggered and the device starts cycling with a period of 2048 clock cycles between the “hiccup” (Power MOSFET off and no current to the load) and “constant current” with very short ON time and with reduced switching frequency (up to one eighth of normal switching frequency). See *Figure 32 on page 33* for short-circuit behavior.

Figure 8. Overcurrent protection strategy



4.5 Inhibit function

The inhibit feature allows the device to be put into standby mode. With the INH pin higher than 1.9 V, the device is disabled and the power consumption is reduced to less than 30 µA. With the INH pin lower than 0.6 V, the device is enabled. If the INH pin is left floating, an internal pull-up ensures that the voltage at the pin reaches the inhibit threshold and the device is disabled. The pin is also V_{CC} compatible.

4.6 Hysteretic thermal shutdown

The thermal shutdown block generates a signal that turns off the power stage if the junction temperature goes above 150 °C. Once the junction temperature goes back to about 130 °C, the device restarts in normal operation. The sensing element is very close to the PDMOS area, therefore ensuring an accurate and fast temperature detection.

5 Application information

5.1 Input capacitor selection

The capacitor connected to the input must be able to support the maximum input operating voltage and the maximum RMS input current required by the device. The input capacitor is subject to a pulsed current, the RMS value of which is dissipated over its ESR, affecting the overall system efficiency.

So the input capacitor must have an RMS current rating higher than the maximum RMS input current and an ESR value compliant with the expected efficiency.

The maximum RMS input current flowing through the capacitor can be calculated as:

Equation 3

$$I_{RMS} = I_O \cdot \sqrt{D - \frac{2 \cdot D^2}{\eta} + \frac{D^2}{\eta^2}}$$

where I_O is the maximum DC output current, D is the duty cycle, η is the efficiency. Considering $\eta = 1$, this function has a maximum at D = 0.5 and it is equal to $I_O/2$.

In a specific application the range of possible duty cycles must be considered in order to find out the maximum RMS input current. The maximum and minimum duty cycles can be calculated as:

Equation 4

$$D_{MAX} = \frac{V_{OUT} + V_F}{V_{INMIN} - V_{SW}}$$

and

Equation 5

$$D_{MIN} = \frac{V_{OUT} + V_F}{V_{INMAX} - V_{SW}}$$

where V_F is the forward voltage on the freewheeling diode and V_{SW} is voltage drop across the internal PDMOS.

In *Table 6* some multi-layer ceramic capacitors suitable for this device are reported.

Table 6. Input capacitors

Manufacturer	Series	Cap value (µF)	Rated voltage (V)
MURATA	GRM31	10	25
	GRM55	10	25
TDK	C3225	10	25

5.2 Inductor selection

The inductance value fixes the current ripple flowing through the output capacitor. So the minimum inductance value, in order to have the expected current ripple, must be selected. The rule to fix the current ripple value is to have a ripple at 20% - 40% of the output current. The inductance value can be calculated by the following equation:

Equation 6

$$\Delta I_L = \frac{V_{IN} - V_{OUT}}{L} \cdot T_{ON} = \frac{V_{OUT}}{L} \cdot T_{OFF}$$

where T_{ON} is the conduction time of the internal high-side switch and T_{OFF} is the conduction time of the external diode [in CCM, $F_{SW} = 1 / (T_{ON} + T_{OFF})$]. The maximum current ripple, at fixed V_{OUT}, is obtained at maximum T_{OFF} that is at minimum duty cycle (see *Section 5.1* to calculate minimum duty). So fixing ΔI_L = 20% to 40% of the maximum output current, the minimum inductance value can be calculated as:

Equation 7

$$L_{MIN} = \frac{V_{OUT} + V_F}{\Delta I_{MAX}} \cdot \frac{1 - D_{MIN}}{F_{SW}}$$

where F_{SW} is the switching frequency, $1 / (T_{ON} + T_{OFF})$.

For example, for V_{OUT} = 3.3 V, V_{IN} = 12 V, I_O = 1.5 A and F_{SW} = 250 kHz, the minimum inductance value to have ΔI_L = 30% of I_O is about 21 µH.

The peak current through the inductor is given by:

Equation 8

$$I_{L,PK} = I_O + \frac{\Delta I_L}{2}$$

So if the inductor value decreases, the peak current (which must be lower than the current limit of the device) increases. The higher the inductor value, the higher the average output current that can be delivered, without reaching the current limit.

In *Table 7* some inductor part numbers are listed.

Table 7. Inductors

Manufacturer	Series	Inductor value (µH)	Saturation current (A)
Wurth	PD	3.3 to 6.8	2.75 to 4.2
Coilcraft	MSS1038	15 to 18	3.2 to 3.6
	MSS7341	3.3 to 6.2	2.5 to 3.5
Coiltronics	CD1	15 to 22	2.9 to 3.6
	UP2.8B	4.7 to 10	2.7 to 3.9
BI	HM76-3	15 to 33	2.5 to 3.7
SUMIDA	CDRH8D28	4.7 to 10	2.5 to 3.4
	CDRH8D28/HP	15 to 22	2.5 to 2.8

5.3 Output capacitor selection

The current in the capacitor has a triangular waveform which generates a voltage ripple across it. This ripple is due to the capacitive component (charge and discharge of the output capacitor) and the resistive component (due to the voltage drop across its ESR). So the output capacitor must be selected in order to have a voltage ripple compliant with the application requirements.

The amount of the voltage ripple can be calculated starting from the current ripple obtained by the inductor selection.

Equation 9

$$\Delta V_{OUT} = ESR \cdot \Delta I_{MAX} + \frac{\Delta I_{MAX}}{8 \cdot C_{OUT} \cdot f_{SW}}$$

Usually the resistive component of the ripple is much higher than the capacitive one, if the output capacitor adopted is not a multi-layer ceramic capacitor (MLCC) with very low ESR value.

The output capacitor is important also for loop stability: it fixes the double LC filter pole and the zero due to its ESR. In *Section 5.4*, how to consider its effect in the system stability is illustrated.

For example, with V_{OUT} = 3.3 V, V_{IN} = 12 V, ΔI_L = 0.5 A (resulting from the inductor value), in order to have a $\Delta V_{OUT} = 0.01 \cdot V_{OUT}$, if the multi-layer ceramic capacitor is adopted, 10 µF is needed and the ESR effect on the output voltage ripple can be neglected. In case of not negligible ESR (electrolytic or tantalum capacitors), the capacitor is chosen taking into account its ESR value.

So in case of 100 µF with ESR = 40 mΩ, the resistive component of the drop dominates and the voltage ripple is 20 mV.

The output capacitor is also important to sustain the output voltage when a load transient with high slew rate is required by the load. When the load transient slew rate exceeds the system bandwidth, the output capacitor provides the current to the load. So if the high slew rate load transient is required by the application, the output capacitor and system bandwidth must be chosen in order to sustain the load transient.

In *Table 8* some capacitor series are listed.

Table 8. Output capacitors

Manufacturer	Series	Cap value (µF)	Rated voltage (V)	ESR (mΩ)
MURATA	GRM32	22 to 100	6.3 to 25	< 5
	GRM31	10 to 47	6.3 to 25	< 5
PANASONIC	ECJ	10 to 22	6.3	< 5
	EEFCD	10 to 68	6.3	15 to 55
SANYO	TPA/B/C	100 to 470	4 to 16	40 to 80
TDK	C3225	22 to 100	6.3	< 5

5.4 Compensation network

The compensation network has to assure stability and good dynamic performance. The loop of the L5983 device is based on the voltage mode control. The error amplifier is a voltage operational amplifier with high bandwidth. So, by selecting the compensation network the E/A is considered as ideal, that is, its bandwidth is much larger than that of the system.

The transfer functions of the PWM modulator and the output LC filter are studied (see *Figure 9*). The transfer function of the PWM modulator, from the error amplifier output (COMP pin) to the OUT pin, results:

Equation 10

$$G_{PW0} = \frac{V_{IN}}{V_s}$$

where V_S is the sawtooth amplitude. As seen in *Section 4.1 on page 9*, the voltage feedforward generates a sawtooth amplitude directly proportional to the input voltage, that is:

Equation 11

$$V_S = K \cdot V_{IN}$$

In this way the PWM modulator gain results constant and equal to:

Equation 12

$$G_{PW0} = \frac{V_{IN}}{V_s} = \frac{1}{K} = 9$$

The synchronization of the device with an external clock provided trough the SYNCH pin can modify the PWM modulator gain (see *Section 4.1* to understand how this gain changes and how to keep it constant in spite of the external synchronization).

The transfer function on the LC filter is given by:

Equation 13

$$G_{LC}(s) = \frac{1 + \frac{s}{2\pi \cdot f_{zESR}}}{1 + \frac{s}{2\pi \cdot Q \cdot f_{LC}} + \left(\frac{s}{2\pi \cdot f_{LC}}\right)^2}$$

where:

Equation 14

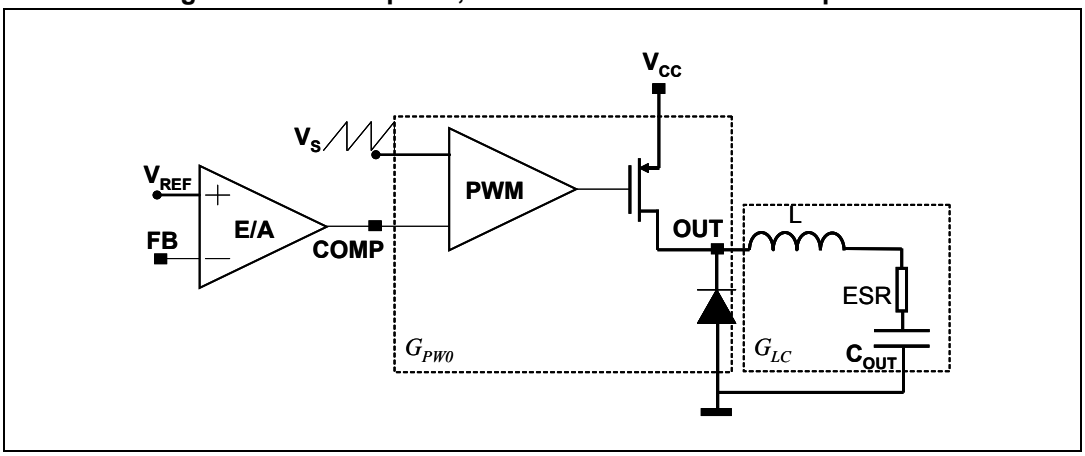
$$f_{LC} = \frac{1}{2\pi \cdot \sqrt{L \cdot C_{OUT}} \cdot \sqrt{1 + \frac{ESR}{R_{OUT}}}}, \qquad f_{zESR} = \frac{1}{2\pi \cdot ESR \cdot C_{OUT}}$$

Equation 15

$$Q = \frac{\sqrt{R_{OUT} \cdot L \cdot C_{OUT} \cdot (R_{OUT} + ESR)}}{L + C_{OUT} \cdot R_{OUT} \cdot ESR}, \qquad R_{OUT} = \frac{V_{OUT}}{I_{OUT}}$$

As seen in *Section 4.3 on page 12*, two different kinds of network can compensate the loop. In the two following paragraphs the guidelines to select the type II and type III compensation network are illustrated.

Figure 9. Error amplifier, PWM modulator and LC output filter



5.4.1 Type III compensation network

The methodology to stabilize the loop consists of placing two zeros to compensate the effect of the LC double pole, therefore increasing phase margin; then to place one pole in the origin to minimize the DC error on regulated output voltage; finally to place other poles far from the zero dB frequency.

If the equivalent series resistance (ESR) of the output capacitor introduces a zero with a frequency higher than the desired bandwidth (that is: $2\pi * ESR * C_{OUT} < 1 /BW$), the type III compensation network is needed. Multi-layer ceramic capacitors (MLCC) have very low ESR (< 1 mΩ), with very high frequency zero, so a type III network is adopted to compensate the loop.

In *Figure 10* the type III compensation network is shown. This network introduces two zeros (f_{Z1}, f_{Z2}) and three poles (f_{P0}, f_{P1}, f_{P2}). They are expressed as:

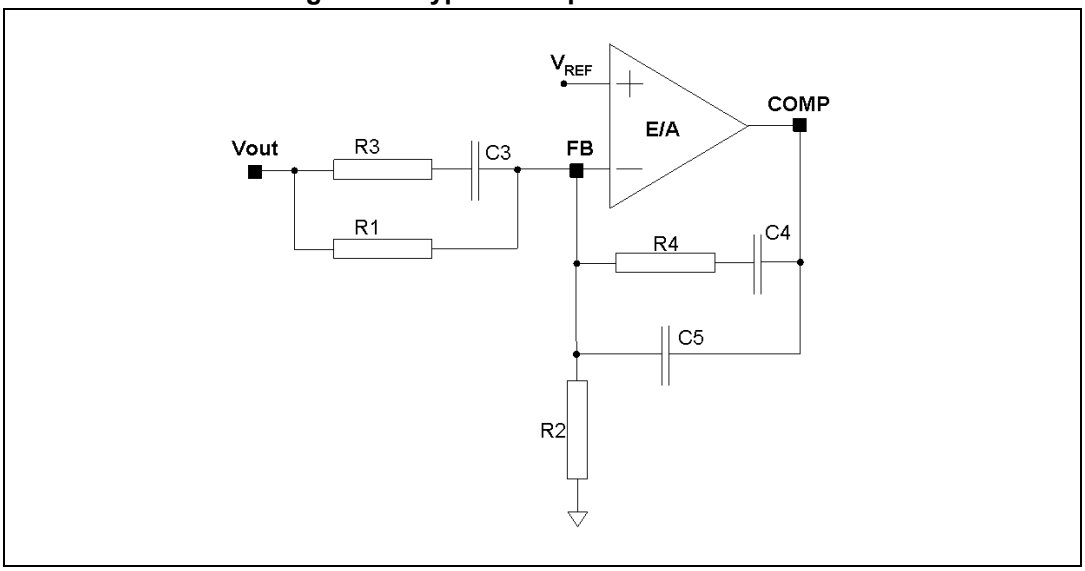
Equation 16

$$f_{Z1} = \frac{1}{2\pi \cdot C_3 \cdot (R_1 + R_3)}, \qquad f_{Z2} = \frac{1}{2\pi \cdot R_4 \cdot C_4}$$

Equation 17

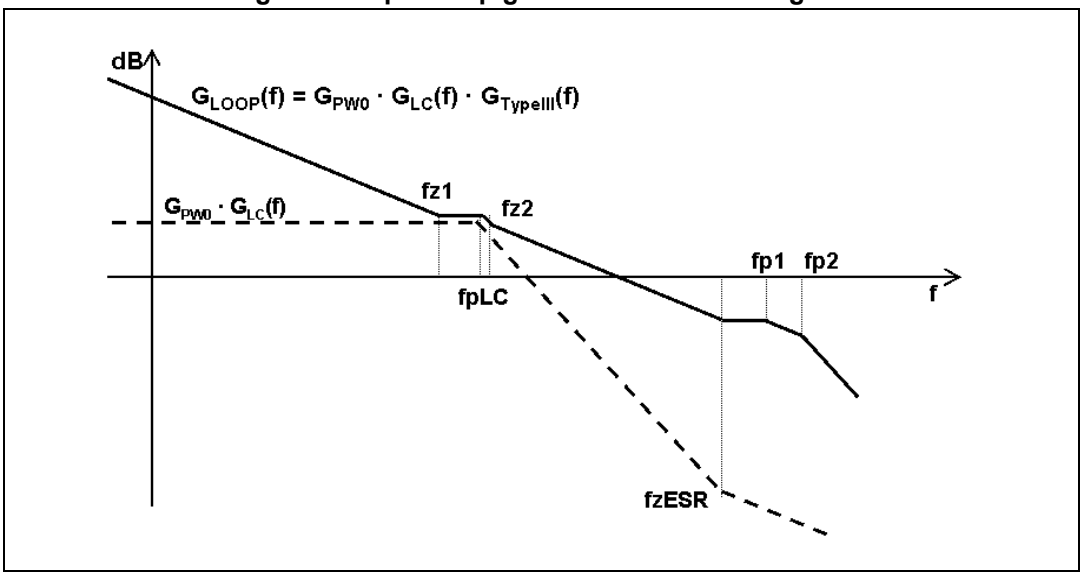
$$f_{P0} = 0, \qquad f_{P1} = \frac{1}{2\pi \cdot R_3 \cdot C_3}, \qquad f_{P2} = \frac{1}{2\pi \cdot R_4 \cdot \frac{C_4 \cdot C_5}{C_4 + C_5}}$$

Figure 10. Type III compensation network



In *Figure 11* the Bode diagram of the PWM and LC filter transfer function [$G_{PW0} \cdot G_{LC}(f)$] and the open loop gain [$G_{LOOP}(f) = G_{PW0} \cdot G_{LC}(f) \cdot G_{TYPEIII}(f)$] is given.

Figure 11. Open loop gain: module Bode diagram



The guidelines for positioning the poles and the zeros and for calculating the component values can be summarized as follows:

1. Choose a value for R_1, usually between 1 kΩ and 5 kΩ.
2. Choose a gain (R_4/R_1) in order to have the required bandwidth (BW), that means:

Equation 18

$$R_4 = \frac{BW \cdot K}{f_{LC}} \cdot R_1$$

where *K* is the feedforward constant and 1 / K is equal to 9.

3. Calculate C_4 by placing the zero at 50% of the output filter double pole frequency (f_{LC}):

Equation 19

$$C_4 = \frac{1}{\pi \cdot R_4 \cdot f_{LC}}$$

4. Calculate C_5 by placing the second pole at four times the system bandwidth (BW):

Equation 20

$$C_5 = \frac{C_4}{2\pi \cdot R_4 \cdot C_4 \cdot 4 \cdot BW - 1}$$

5. Set the first pole also at four times the system bandwidth and also the second zero at the output filter double pole:

Equation 21

$$R_3 = \frac{R_1}{\frac{4 \cdot BW}{f_{LC}} - 1}, \qquad C_3 = \frac{1}{2\pi \cdot R_3 \cdot 4 \cdot BW}$$

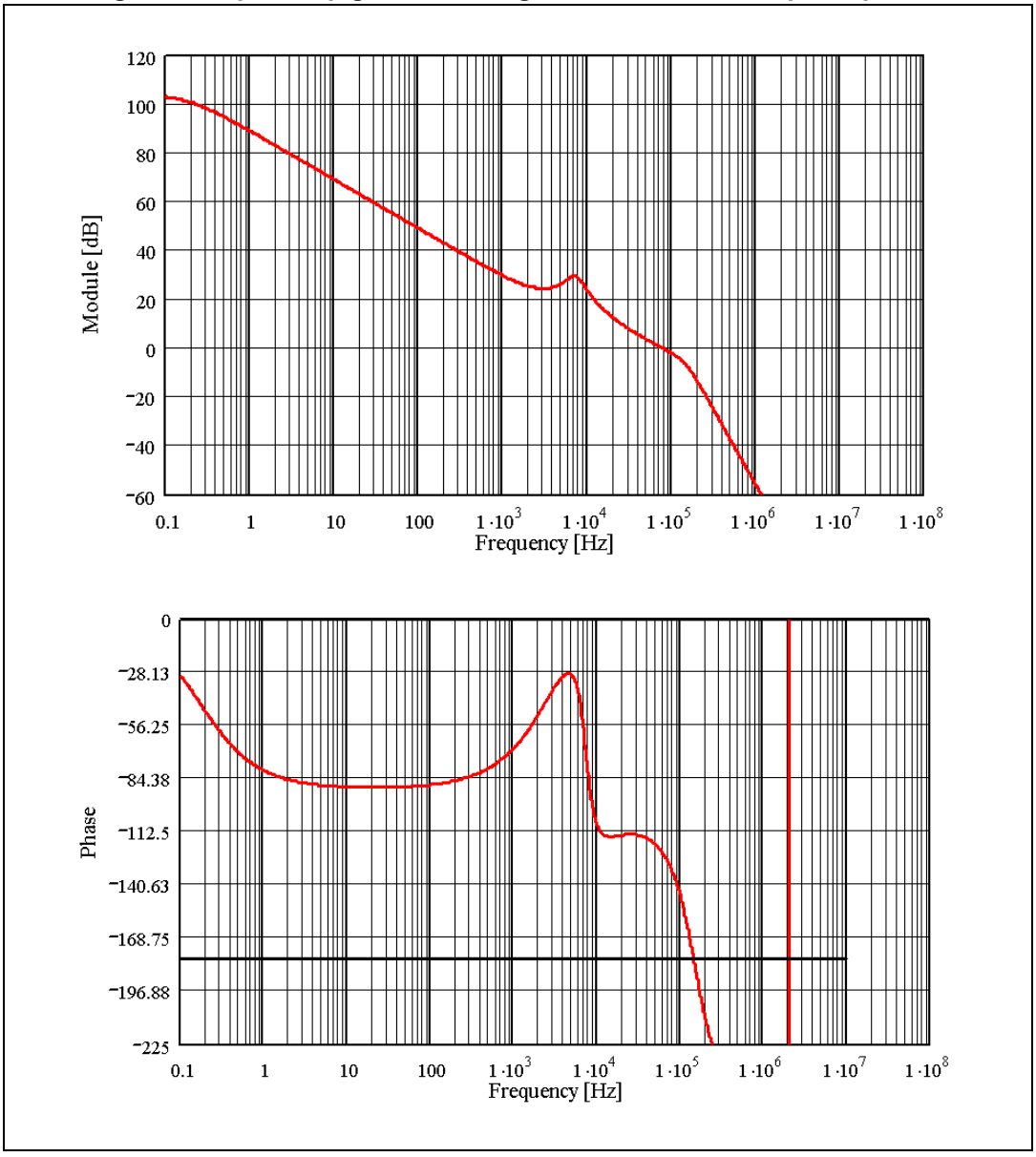
The suggested maximum system bandwidth is equal to the switching frequency divided by 3.5 (F_{SW} / 3.5), but lower than 100 kHz if the F_{SW} is set higher than 500 kHz.

For example, with V_{OUT} = 3.3 V, V_{IN} = 12 V, I_O = 1.5 A, L = 22 µH, C_{OUT} = 22 µF, ESR < 1 mΩ, the type III compensation network is:

$R_1 = 4.99k\Omega$, $R_2 = 1.1k\Omega$, $R_3 = 120\Omega$, $R_4 = 4.99k\Omega$, $C_3 = 4.7nF$, $C_4 = 10nF$, $C_5 = 68pF$

In *Figure 12* the module and phase of the open loop gain is shown. The bandwidth is about 77 kHz and the phase margin is 47°.

Figure 12. Open loop gain Bode diagram with ceramic output capacitor

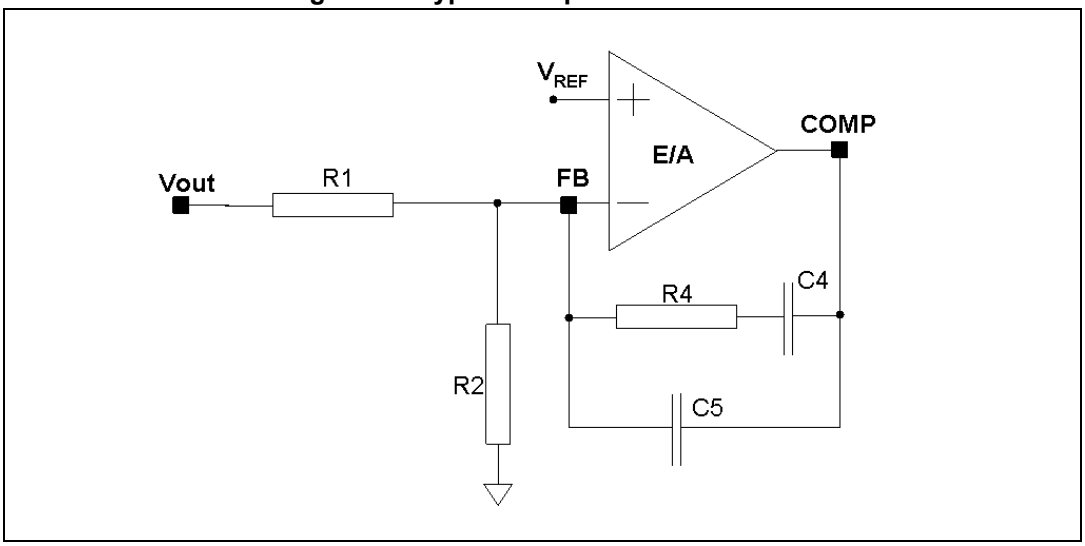


5.4.2 Type II compensation network

If the equivalent series resistance (ESR) of the output capacitor introduces a zero with a frequency lower than the desired bandwidth (that is: $2\pi * ESR * C_{OUT} > 1 / BW$), this zero helps stabilize the loop. Electrolytic capacitors show not negligible ESR (> 30 mΩ), so with this kind of the output capacitor the type II network combined with the zero of the ESR allows the loop to be stabilized.

In *Figure 13* the type II network is shown.

Figure 13. Type II compensation network



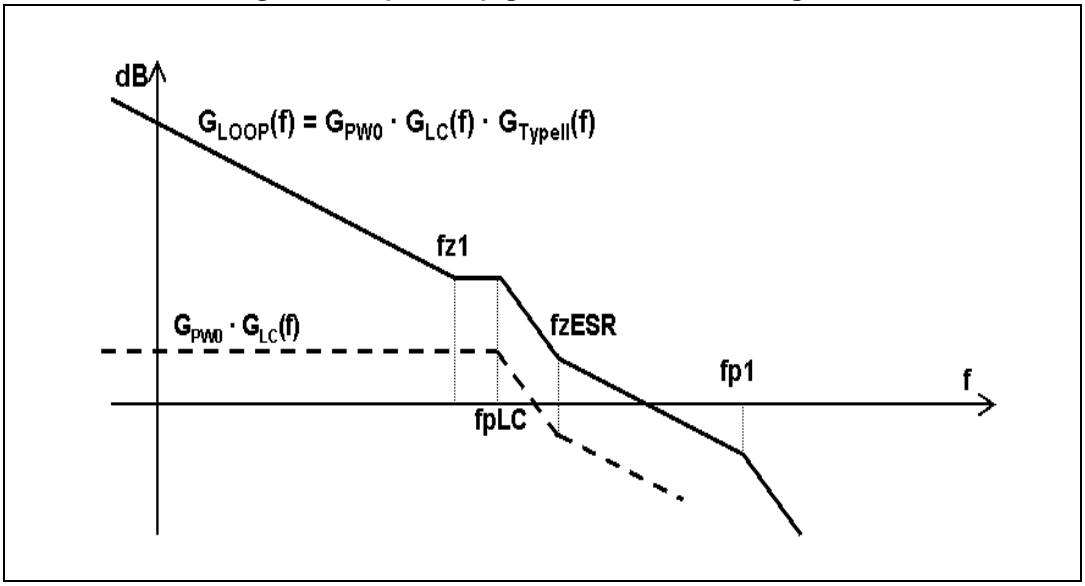
The singularities of the network are:

Equation 22

$$f_{Z1} = \frac{1}{2\pi \cdot R_4 \cdot C_4}, \quad f_{P0} = 0, \quad f_{P1} = \frac{1}{2\pi \cdot R_4 \cdot \frac{C_4 \cdot C_5}{C_4 + C_5}}$$

In *Figure 14* the Bode diagram of the PWM and LC filter transfer function [$G_{PW0} \cdot G_{LC}(f)$] and the open loop gain [$G_{LOOP}(f) = G_{PW0} \cdot G_{LC}(f) \cdot G_{TYPEII}(f)$] is given.

Figure 14. Open loop gain: module Bode diagram



The guidelines for positioning the poles and the zeros and for calculating the component values can be summarized as follows:

1. Choose a value for R_1, usually between 1 kΩ and 5 kΩ, in order to have values of C4 and C5 not comparable with parasitic capacitance of the board.
2. Choose a gain (R_4/R_1) in order to have the required bandwidth (BW), that means:

Equation 23

$$R_4 = \left(\frac{f_{ESR}}{f_{LC}}\right)^2 \cdot \frac{BW}{f_{ESR}} \cdot \frac{V_S}{V_{IN}} \cdot R_1$$

where f_{ESR} is the ESR zero:

Equation 24

$$f_{ESR} = \frac{1}{2\pi \cdot ESR \cdot C_{OUT}}$$

and V_S is the sawtooth amplitude. The voltage feedforward keeps the ratio V_S/V_{IN} constant.

3. Calculate C_4 by placing the zero one decade below the output filter double pole:

Equation 25

$$C_4 = \frac{10}{2\pi \cdot R_4 \cdot f_{LC}}$$

4. Then calculate C_3 in order to place the second pole at four times the system bandwidth (BW):

Equation 26

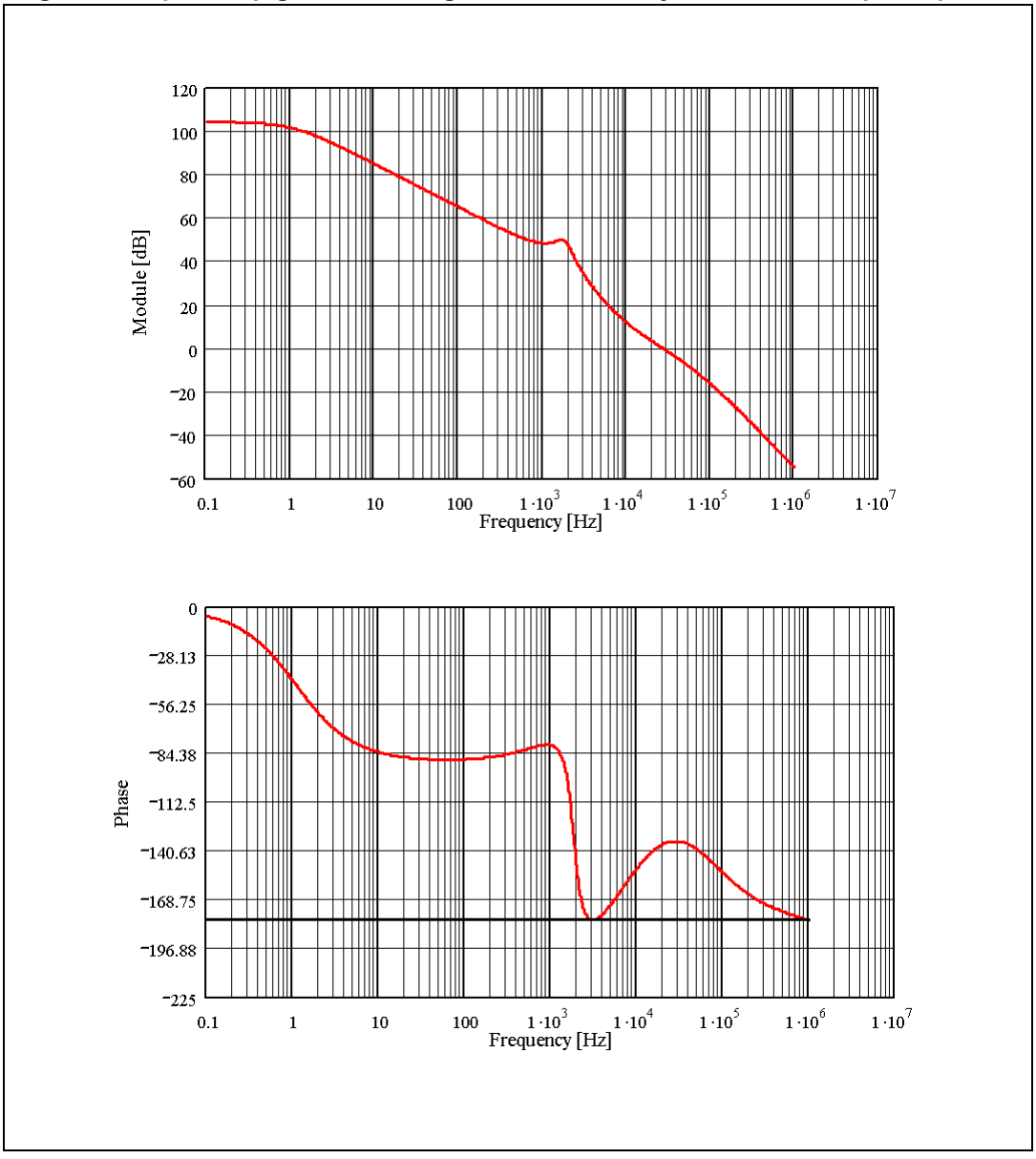
$$C_5 = \frac{C_4}{2\pi \cdot R_4 \cdot C_4 \cdot 4 \cdot BW - 1}$$

For example, with V_{OUT} = 3.3 V, V_{IN} = 12 V, I_O = 1.5 A, L = 22 µH, C_{OUT} = 330 µF, ESR = 50 mΩ, the type II compensation network is:

$$R_1 = 1.1k\Omega, \quad R_2 = 249\Omega, \quad R_4 = 10k\Omega, \quad C_4 = 6.8nF, \quad C_5 = 68pF$$

In *Figure 15* the module and phase of the open loop gain is shown. The bandwidth is about 30 kHz and the phase margin is 45°.

Figure 15. Open loop gain Bode diagram with electrolytic/tantalum output capacitor



5.5 Thermal considerations

The thermal design is important to prevent the thermal shutdown of the device if junction temperature goes above 150 °C. The three different sources of losses within the device are:

a) Conduction losses due to the not negligible $R_{DS(on)}$ of the power switch; these are equal to:

Equation 27

$$P_{ON} = R_{DS(on)} \cdot (I_{OUT})^2 \cdot D$$

where *D* is the duty cycle of the application and the maximum $R_{DS(on)}$ is 220 mΩ.

Note that the duty cycle is theoretically given by the ratio between V_{OUT} and V_{IN}, but actually it is quite higher to compensate the losses of the regulator. So the conduction losses increase compared with the ideal case.

b) Switching losses due to Power MOSFET turn-on and -off; these can be calculated as:

Equation 28

$$P_{SW} = V_{IN} \cdot I_{OUT} \cdot \frac{(T_{RISE} + T_{FALL})}{2} \cdot Fsw = V_{IN} \cdot I_{OUT} \cdot T_{SW} \cdot F_{SW}$$

where T_{RISE} and T_{FALL} are the overlap times of the voltage across the power switch (V_{DS}) and the current flowing into it during turn-on and turn-off phases, as shown in *Figure 16*. T_{SW} is the equivalent switching time.

For this device the typical value for the equivalent switching time is 50 ns.

c) Quiescent current losses, calculated as:

Equation 29

$$P_Q = V_{IN} \cdot I_Q$$

where I_Q is the quiescent current. (I_Q = 2.4 mA).

The junction temperature T_J can be calculated as:

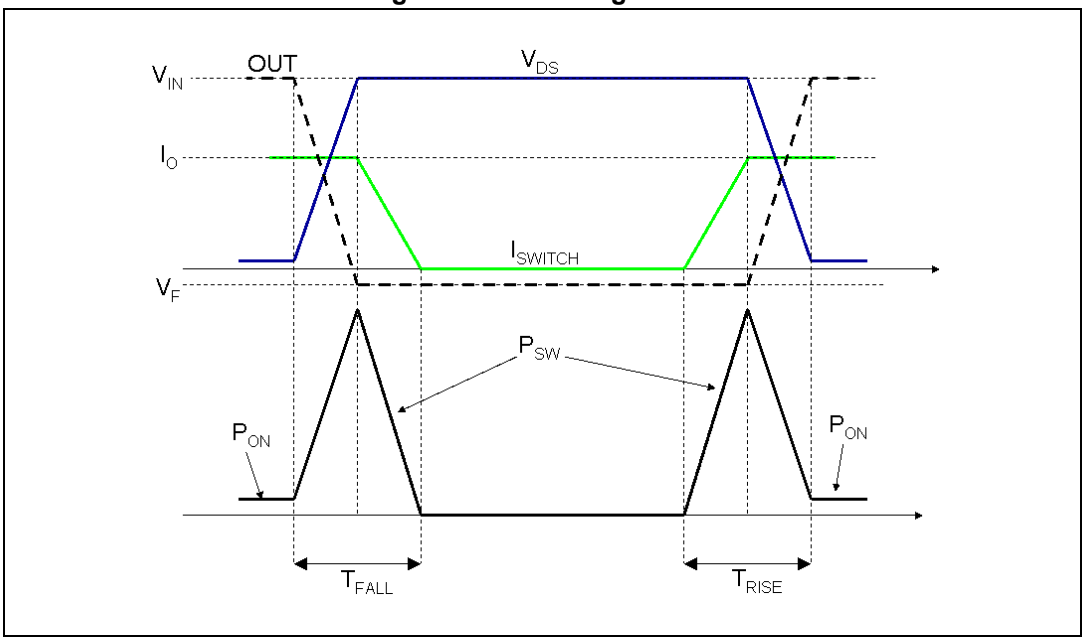
Equation 30

$$T_J = T_A + Rth_{JA} \cdot P_{TOT}$$

where T_A is the ambient temperature and P_{TOT} is the sum of the power losses just seen.

Rth_{JA} is the equivalent thermal resistance junction to ambient of the device; it can be calculated as the parallel of many paths of heat conduction from the junction to the ambient. For this device the path through the exposed pad is the one conducting the largest amount of heat. The Rth_{JA}, measured on the demonstration board described in *Section 5.6: Layout considerations*, is about 60 °/W.

Figure 16. Switching losses



5.6 Layout considerations

The PC board layout of the switching DC/DC regulator is very important to minimize the noise injected in high impedance nodes and interferences generated by the high switching current loops.

In a step-down converter the input loop (including the input capacitor, the Power MOSFET and the freewheeling diode) is the most critical one. This is due to the fact that the high value pulsed current is flowing through it. In order to minimize the EMI, this loop must be as short as possible.

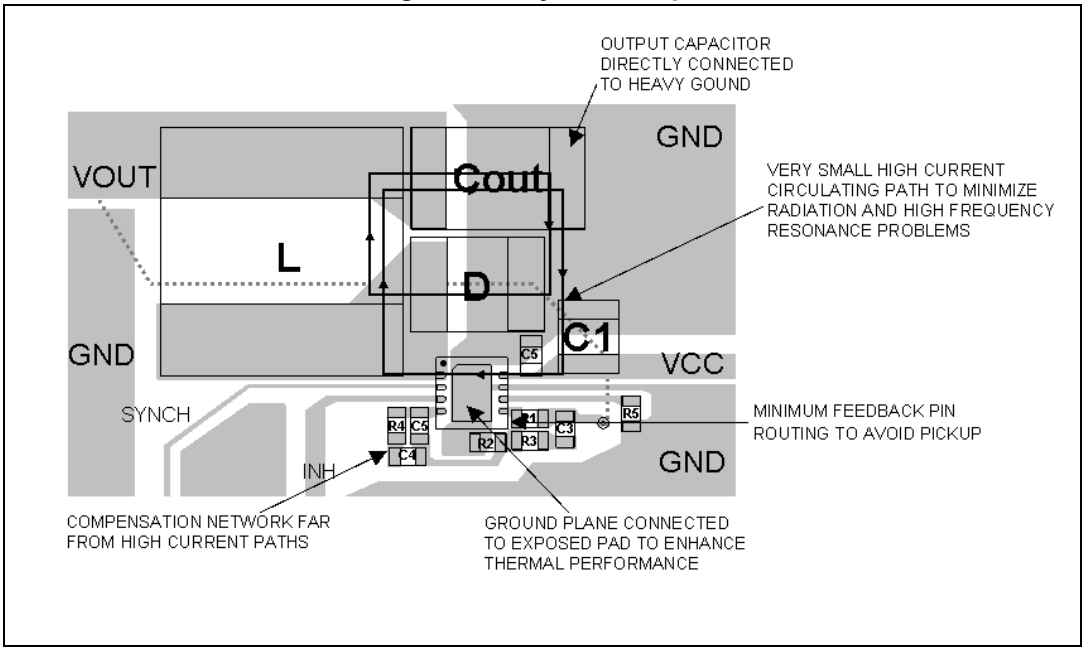
To filter the high frequency noise, a small capacitor can be added as close as possible to the input voltage pin of the device.

The feedback pin (FB) connection to the external resistor divider is a high impedance node, so the interferences can be minimized placing the routing of the feedback node as far as possible from the high current paths. To reduce the pick up noise the resistor divider has to be placed very close to the device.

Thanks to the exposed pad of the device, the ground plane helps to reduce the thermal resistance junction to ambient; so a large ground plane enhances the thermal performance of the converter allowing high power conversion.

In *Figure 17* a layout example is shown.

Figure 17. Layout example



5.7 Application circuit

In *Figure 18* the demonstration board application circuit is shown.

Figure 18. Demonstration board application circuit

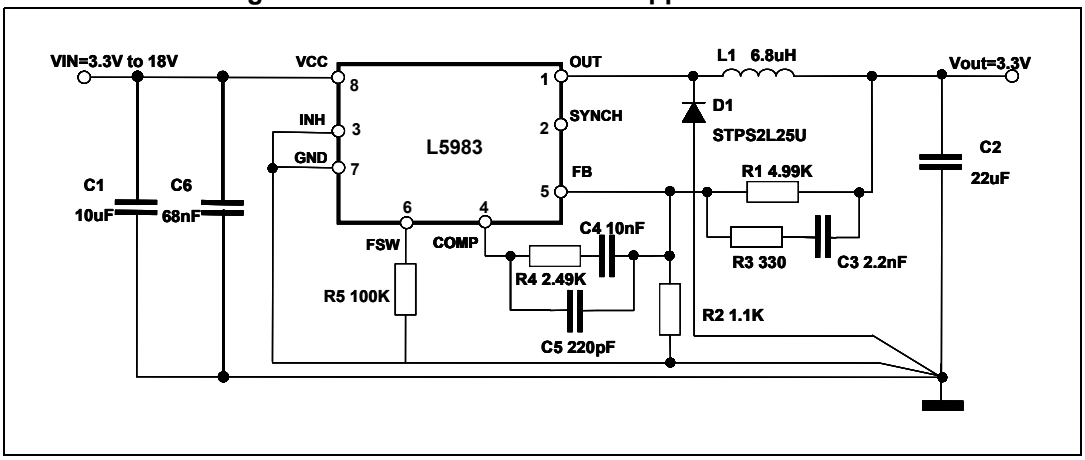


Table 9. Component list

Reference	Part number	Description	Manufacturer
C1	GRM31CR61E106KA12	10 µF, 25 V	MURATA
C2	GRM31CR61C226KE15B	22 µF, 16 V	MURATA
C3		2.2 nF, 50 V	
C4		10 nF, 50 V	
C5		220 pF, 50 V	
C6		68 nF, 25 V	
R1		4.99 kΩ, 1%, 0.1 W 0603	
R2		1.1 kΩ, 1%, 0.1 W 0603	
R3		330 Ω, 1%, 0.1 W 0603	
R4		2.99 kΩ, 1%, 0.1 W 0603	
R5		100 kΩ, 1%, 0.1 W 0603	
L1	7447779006	6.8 µH, 30%, 2.91 A	Coilcraft
D1	STPS2L25V	2 A, 25 V	STMicroelectronics

Figure 19. PCB layout (component side)

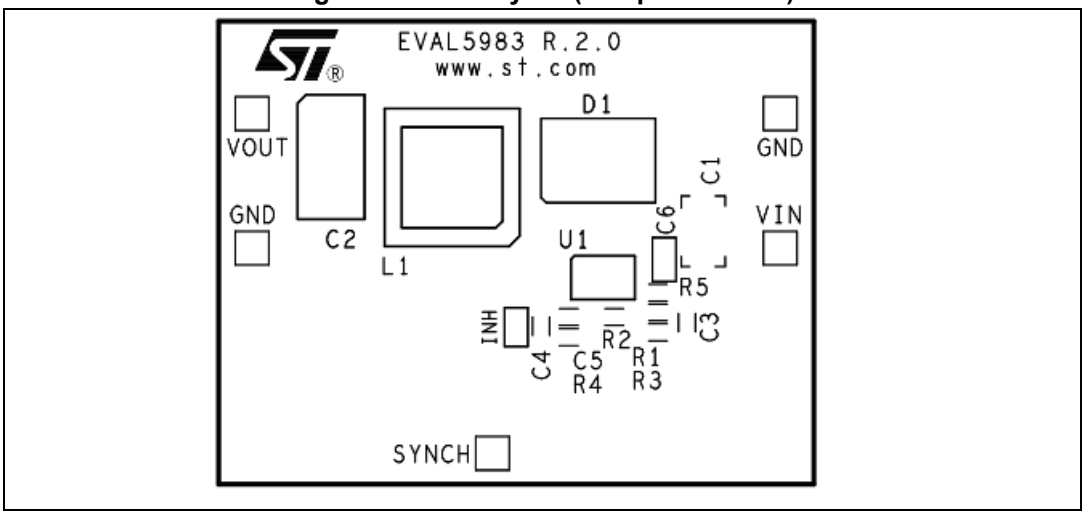


Figure 20. PCB layout (bottom side)

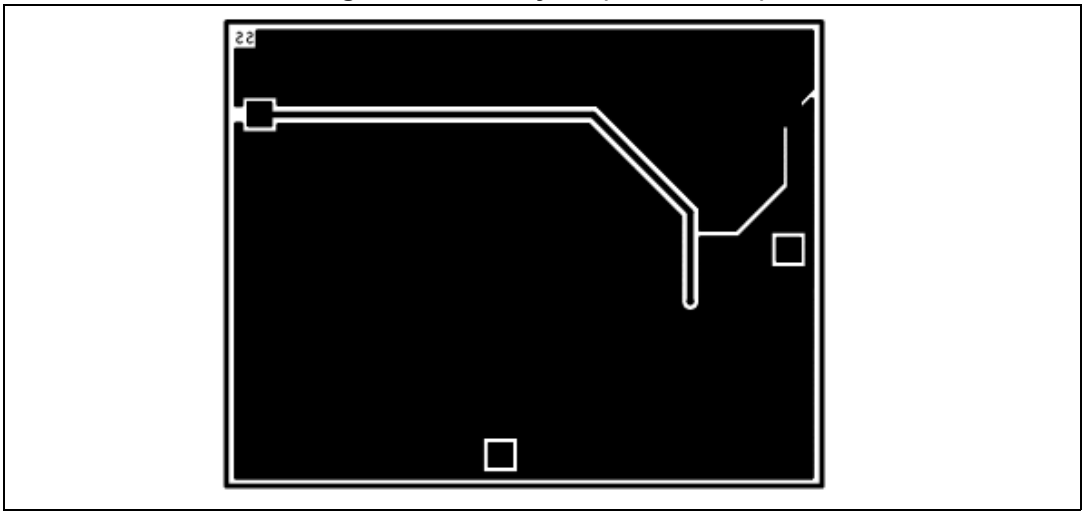


Figure 21. PCB layout (front side)

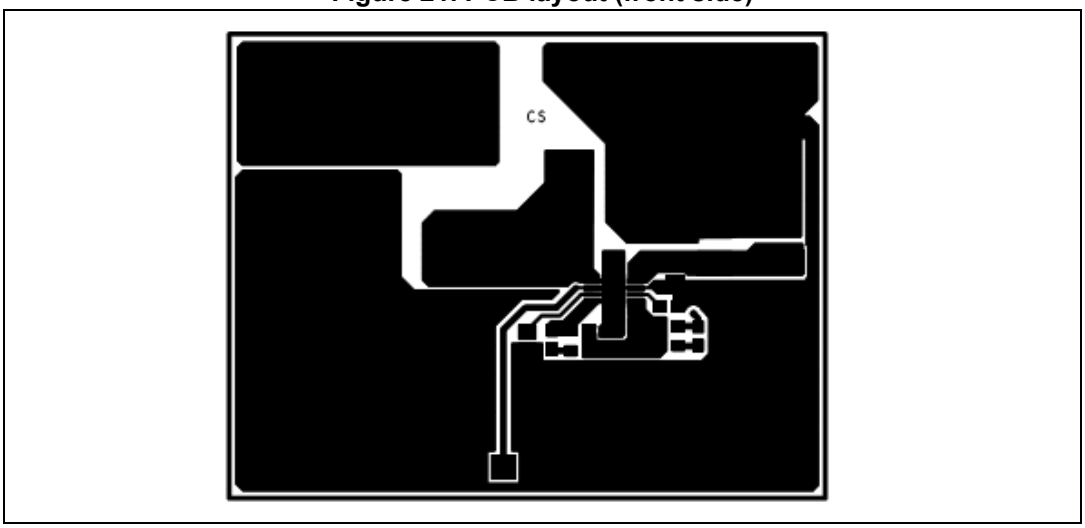


Figure 22. Junction temperature vs. output current - V_{CC} = 5 V

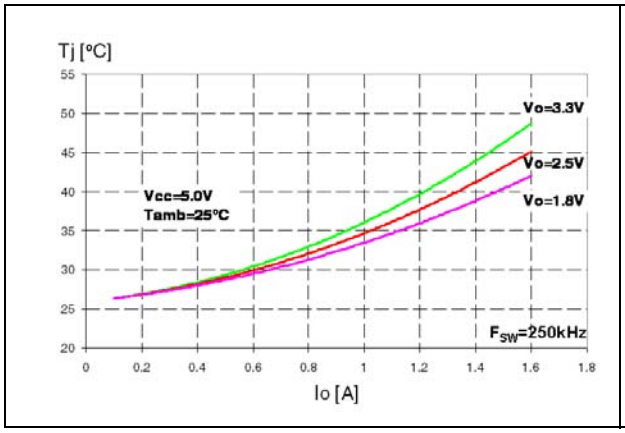


Figure 23. Junction temperature vs. output current - V_{CC} = 12 V

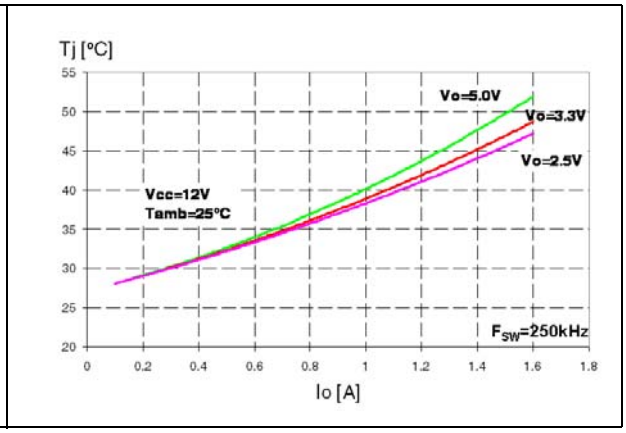


Figure 24. Junction temperature vs. output current - V_{CC} = 18 V

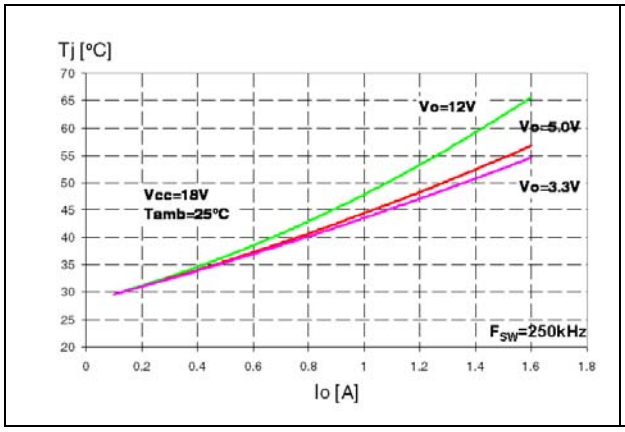


Figure 25. Efficiency vs. output current - V_{CC} = 12 V

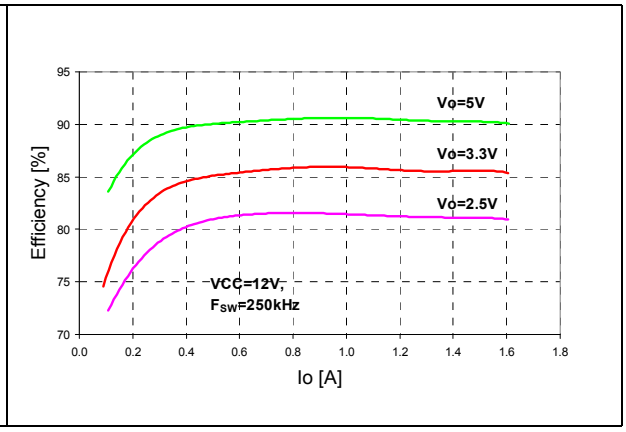


Figure 26. Efficiency vs. output current - V_{CC} = 5 V

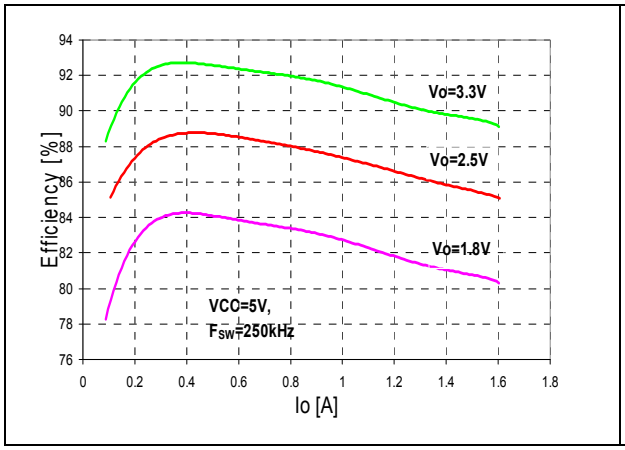


Figure 27. Efficiency vs. output current - V_{CC} = 3.3 V

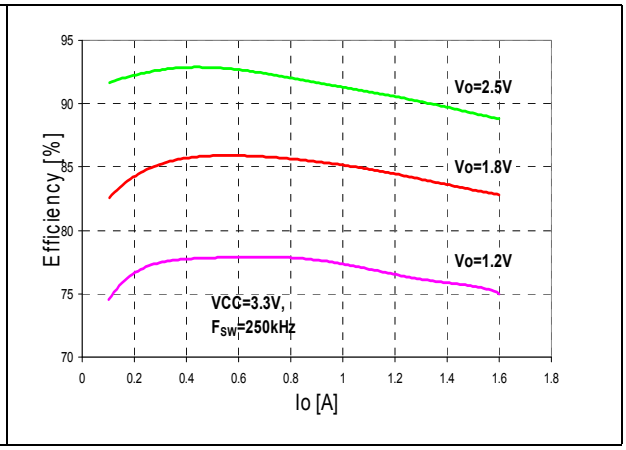


Figure 28. Load regulation

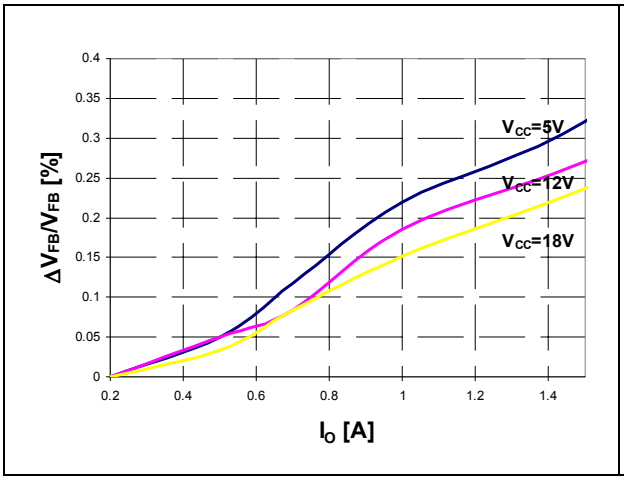


Figure 29. Line regulation

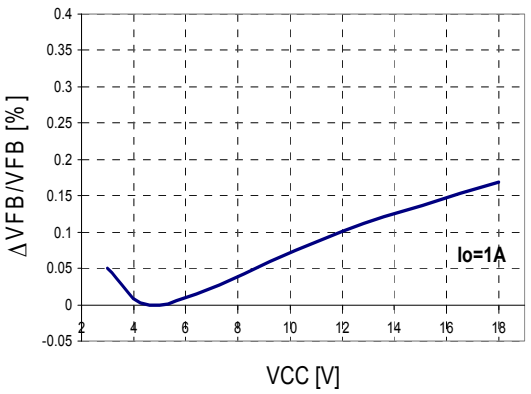


Figure 30. Load transient: from 300 mA to 1.3 A

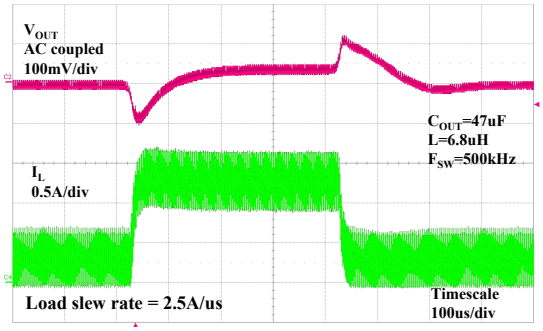


Figure 31. Soft-start

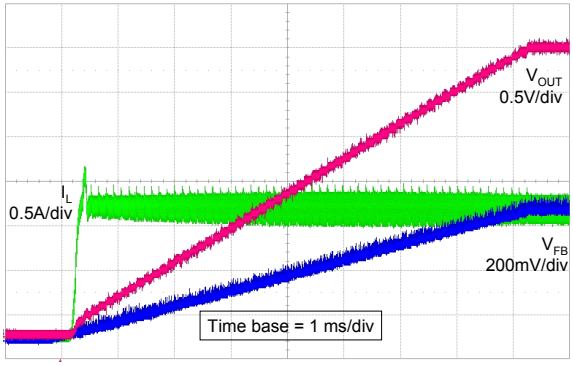
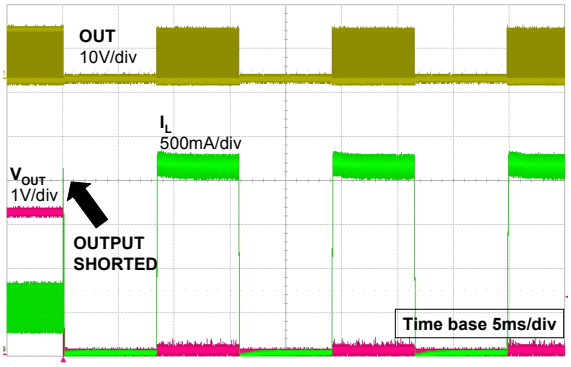


Figure 32. Short-circuit behavior



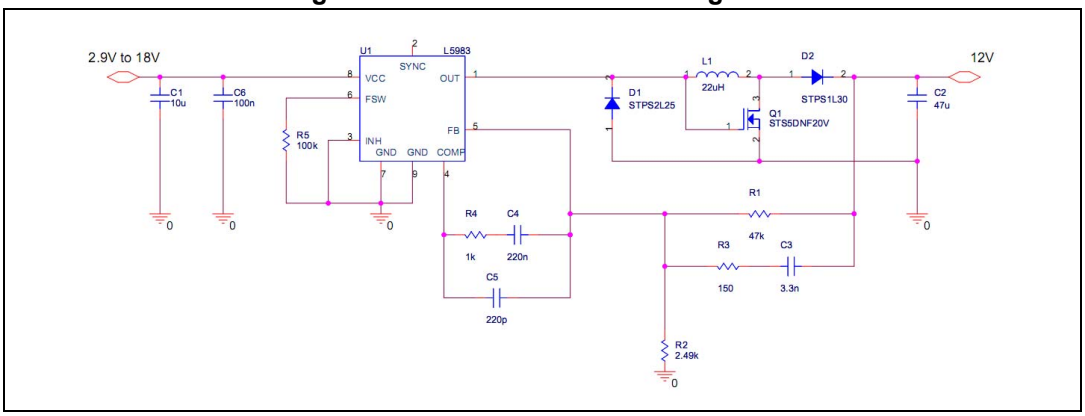
6 Application ideas

6.1 Positive buck-boost

The L5983 device can implement the step-up/down converter with a positive output voltage.

Figure 33 shows the schematic: one Power MOSFET and one Schottky diode are added to the standard buck topology to provide 12 V output voltage with input voltage from 2.9 V to 18 V.

Figure 33. Positive buck-boost regulator



The relationship between input and output voltage is:

Equation 31

$$V_{OUT} = V_{IN} \cdot \frac{D}{1-D}$$

so the duty cycle is:

Equation 32

$$D = \frac{V_{OUT}}{V_{OUT} + V_{IN}}$$

The output voltage is not limited by the maximum operating voltage of the device (18 V), because the output voltage is sensed only through the resistor divider. The external Power MOSFET maximum drain to source voltage, must be higher than output voltage; the maximum gate to source voltage must be higher than the input voltage (in *Figure 33*, if V_{IN} is higher than 16 V, the gate must be protected through a Zener diode and a resistor).

The current flowing through the internal Power MOSFET is transferred to the load only during the OFF time, so according to the maximum DC switch current (1.5 A), the maximum output current for the buck-boost topology can be calculated from the following equation.

Equation 33

$$I_{SW} = \frac{I_{OUT}}{1-D} < 1.5\ A$$

where I_{SW} is the average current in the embedded Power MOSFET in the ON time.

To chose the right value of the inductor and to manage transient output current, which for a short time can exceed the maximum output current calculated by *Equation 33*, the peak current in the Power MOSFET must also be calculated. The peak current, shown in *Equation 34*, must be lower than the minimum current limit (2.0 A).

Equation 34

$$I_{SW,PK} = \frac{I_{OUT}}{1-D} \cdot \left[1 + \frac{r}{2}\right] < 2.0A$$

$$r = \frac{V_{OUT}}{I_{OUT} \cdot L \cdot F_{SW}} \cdot (1-D)^2$$

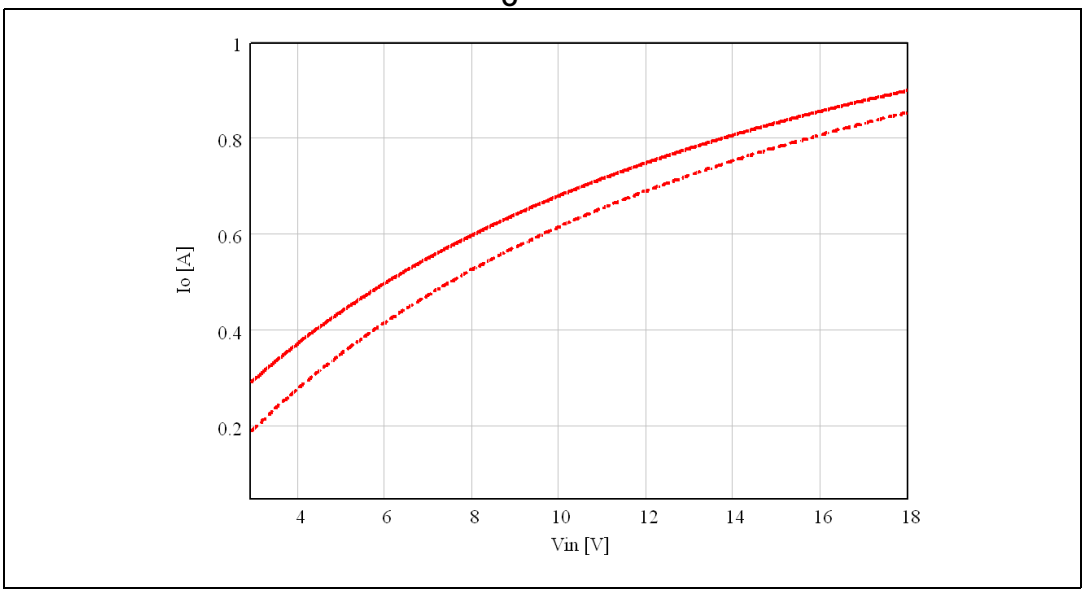
where *r* is defined as the ratio between the inductor current ripple and the inductor DC current.

Therefore, in the buck-boost topology the maximum output current depends on the application conditions (firstly input and output voltage, secondly switching frequency and inductor value).

In *Figure 34* the maximum output current for the above configuration is depicted varying the input voltage from 2.9 V to 18 V.

The dashed line considers a more accurate estimation of the duty cycles given by *Equation 35*, where power losses across diodes, the external Power MOSFET, and the internal Power MOSFET are taken into account.

Figure 34. Maximum output current according to max DC switch current (1.5 A): V_O = 12 V



Equation 35

$$D = \frac{V_{OUT} + 2 \cdot V_D}{V_{IN} - V_{SW} - V_{SWE} + V_{OUT} + 2 \cdot V_D}$$

where V_D is the voltage drop across the diodes, and V_{SW} and V_{SWE} across the internal and external Power MOSFET.

6.2 Inverting buck-boost

The L5983 device can implement the step-up/down converter with a negative output voltage.

Figure 33 shows the schematic to regulate -5 V: no further external components are added to the standard buck topology.

The relationship between input and output voltage is:

Equation 36

$$V_{OUT} = -V_{IN} \cdot \frac{D}{1-D}$$

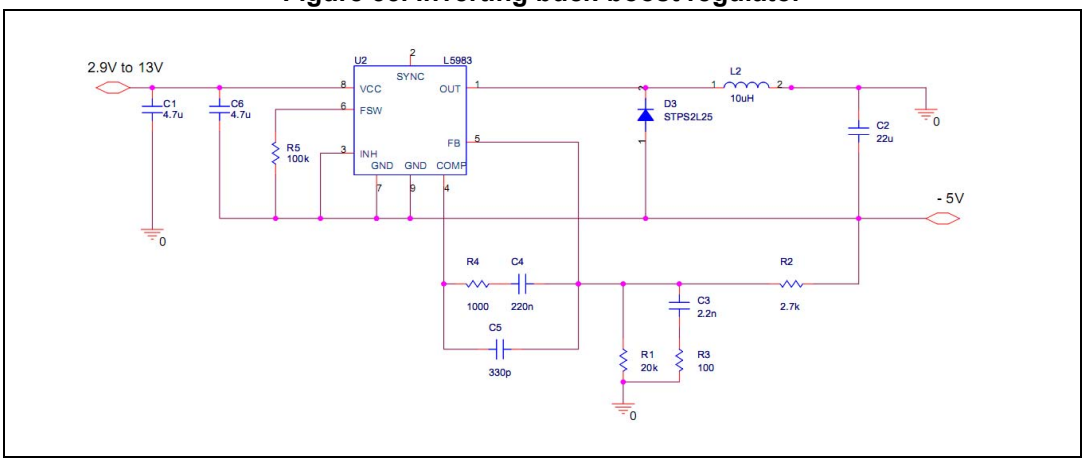
so the duty cycle is:

Equation 37

$$D = \frac{V_{OUT}}{V_{OUT} - V_{IN}}$$

As in the positive one, in the inverting buck-boost the current flowing through the Power MOSFET is transferred to the load only during the OFF time. So according to the maximum DC switch current (1.5 A), the maximum output current can be calculated from *Equation 33*, where the duty cycle is given by *Equation 37*.

Figure 35. Inverting buck-boost regulator



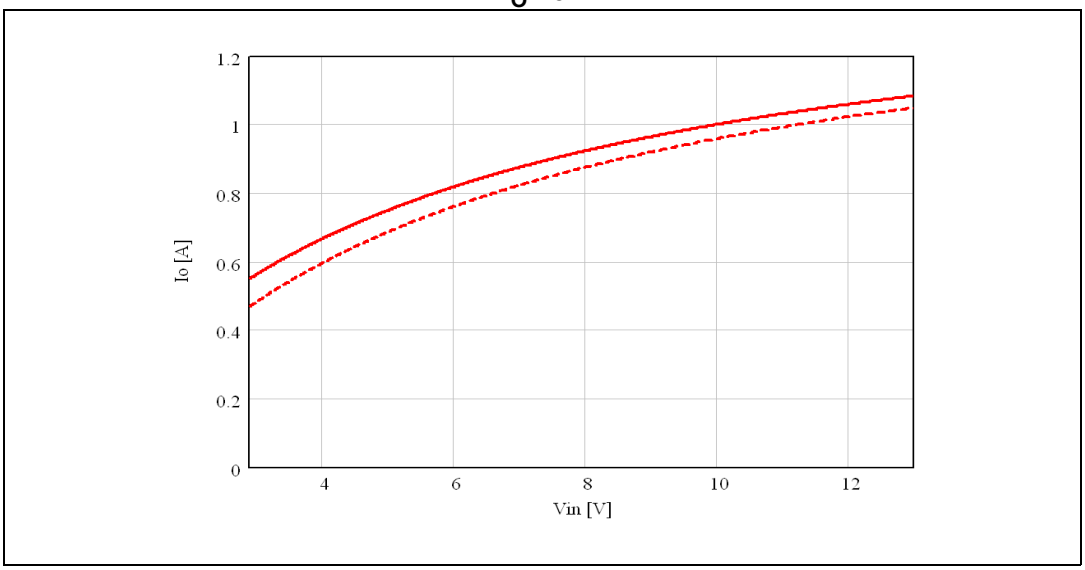
The GND pin of the device is connected to the output voltage so, given the output voltage, the input voltage range is limited by the maximum voltage, the device can withstand across V_{CC} and GND (18 V). Therefore, if the output is -5 V, the input voltage can range from 2.9 V to 13 V.

As in the positive buck-boost, the maximum output current according to application conditions is shown in *Figure 36*. The dashed line considers a more accurate estimation of the duty cycles given by *Equation 38*, where power losses across diodes and the internal Power MOSFET are taken into account:

Equation 38

$$D = \frac{V_{OUT} - V_D}{-V_{IN} - V_{SW} + V_{OUT} - V_D}$$

Figure 36. Maximum output current according to max DC switch current (1.5 A): V_O=-5 V



7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST registered trademark.

Figure 37. VFQFPN8 (3 x 3 x 1.08 mm) package outline

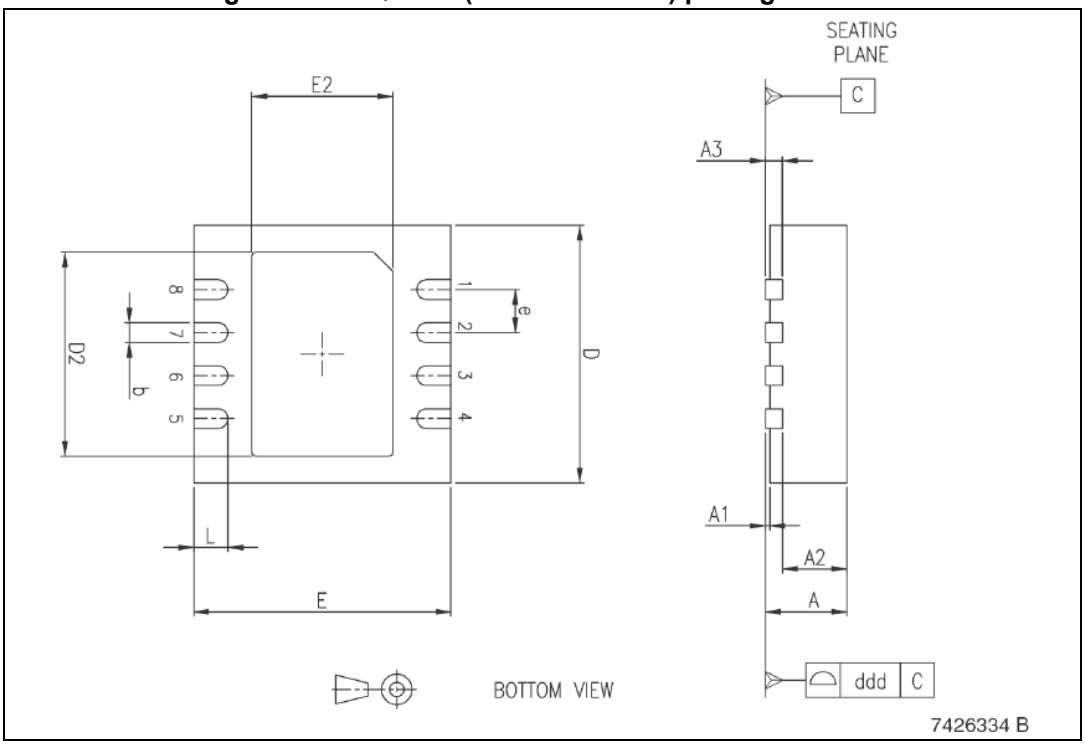


Table 10. VFQFPN8 (3 x 3 x 1.08 mm) package mechanical data

Symbol	Dimensions					
	mm			inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.80	0.90	1.00	0.0315	0.0354	0.0394
A1		0.02	0.05		0.0008	0.0020
A2		0.70			0.0276	
A3		0.20			0.0079	
b	0.18	0.23	0.30	0.0071	0.0091	0.0118
D	2.95	3.00	3.05	0.1161	0.1181	0.1200
D2	2.23	2.38	2.48	0.0878	0.0937	0.0976
E	2.95	3.00	3.05	0.1161	0.1181	0.1200
E2	1.65	1.70	1.75	0.0649	0.0669	0.0689
e		0.50			0.0197	
L	0.35	0.40	0.45	0.0137	0.0157	0.0177
ddd			0.08			0.0031

8 Order codes

Table 11. Order codes

Order codes	Package	Packaging
L5983TR	VFQFPN8 (3 x 3 x 1.08 mm)	Tape and reel

9 Revision history

Table 12. Document revision history

Date	Revision	Changes
21-Dec-2006	1	Initial release
16-Oct-2007	2	Document status promoted from preliminary data to datasheet
27-May-2008	3	Updated: Cover page, *Figure 2 on page 4*, *Figure 8 on page 14*, *Figure 5 on page 10*, *Figure 17 on page 29*, *Figure 18 on page 30*, *Table 8 on page 17*, *Table 10 on page 39* Added: *Table 3 on page 5*
16-Sep-2008	4	Updated: *Table 4 on page 6* and *Figure 18 on page 30*
28-Jan-2009	5	Updated: *Equation 18*
15-Jun-2009	6	Updated *Table 4 on page 6* and *Figure 6 on page 10*
29-Nov-2010	7	Added: *Section 6 on page 34* Updated: *Figure 19*, *Figure 20* and *Figure 21 on page 31*
12-May-2014	8	Numbered *Equation 22 on page 23*. Added V_{CC} values to titles from *Figure 22 on page 32* to *Figure 27 on page 32*. Updated *Section 7: Package information on page 38* (updated titles, reversed order of *Figure 37* and *Table 10*, minor modifications). Updated *Table 11: Order codes* (removed the L5983 order code related to the VFQFPN8 in tube, updated “Packaging” of the L5983TR order code). Updated cross-references throughout document. Minor modifications throughout document.

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