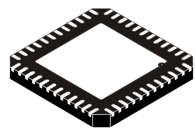
L6235Q

DMOS driver for 3-phase brushless dc motor

Features

- Operating supply voltage from 8 to 52 V
- 5.6 A output peak current
- $R_{DS(on)}$ 0.3 Ω typ. value @ T_J = 25 °C
- Operating frequency up to 100 kHz
- Non-dissipative overcurrent protection
- Diagnostic output
- Constant t_{OFF} PWM current controller
- Slow decay synchronous rectification
- 60° and 120° Hall effect decoding logic
- Brake function
- Tacho output for speed loop
- Cross conduction protection
- Thermal shutdown
- Undervoltage lockout
- Integrated fast freewheeling diodes

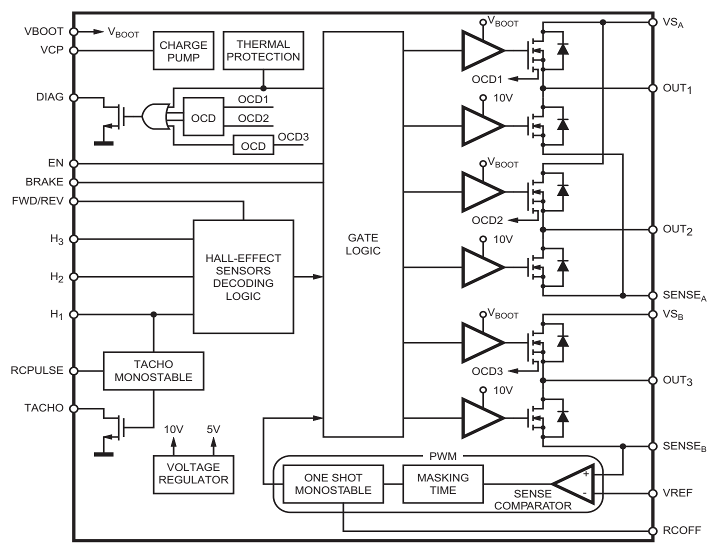


QFN-48
(7 x 7 mm)

Description

The L6235Q is a DMOS fully integrated 3-phase motor driver with overcurrent protection. Realized in BCDmultipower technology, the device combines isolated DMOS power transistors with CMOS and bipolar circuits on the same chip. The device includes all the circuitry needed to drive a 3-phase BLDC motor including: a 3-phase DMOS bridge, a constant OFF time PWM current controller and the decoding logic for single ended Hall sensors that generates the required sequence for the power stage. Available in QFN48 7x7 package, the L6235Q features a non-dissipative overcurrent protection on the high-side power MOSFETs and thermal shutdown.

Figure 1. Block diagram



AM02555v1

Contents

1 Electrical data

1.1 Absolute maximum ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Parameter	Value	Unit
V_S	Supply voltage	$V_{SA} = V_{SB} = V_S$	60	V
V_{OD}	Differential voltage between VS_A, $OUT1_A$, $OUT2_A$, $SENSE_A$ and VS_B, $OUT1_B$, $OUT2_B$, $SENSE_B$	$V_{SA} = V_{SB} = V_S = 60$ V; $VSENSE_A = VSENSE_B =$ GND	60	V
V_{BOOT}	Bootstrap peak voltage	$V_{SA} = V_{SB} = V_S$	$V_S + 10$	V
V_{IN}, V_{EN}	Input and enable voltage range		-0.3 to +7	V
V_{REF}	Voltage range at pin V_{REF}		-0.3 to +7	V
V_{RCOFF}	Voltage range at pin RC_{OFF}		-0.3 to +7	V
V_{SENSE}	Voltage range at pins $SENSE_A$ and $SENSE_B$		-1 to +4	V
$I_{S(peak)}$	Pulsed supply current (for each V_{SA} and V_{SB} pin)	$V_{SA} = V_{SB} = V_S$; $t_{PULSE} < 1$ ms	7.1	A
I_S	DC supply current (for each VS_A and VS_B pin)	$VS_A = VS_B = V_S$	2.5	A
T_{stg}, T_{OP}	Storage and operating temperature range		-40 to 150	°C

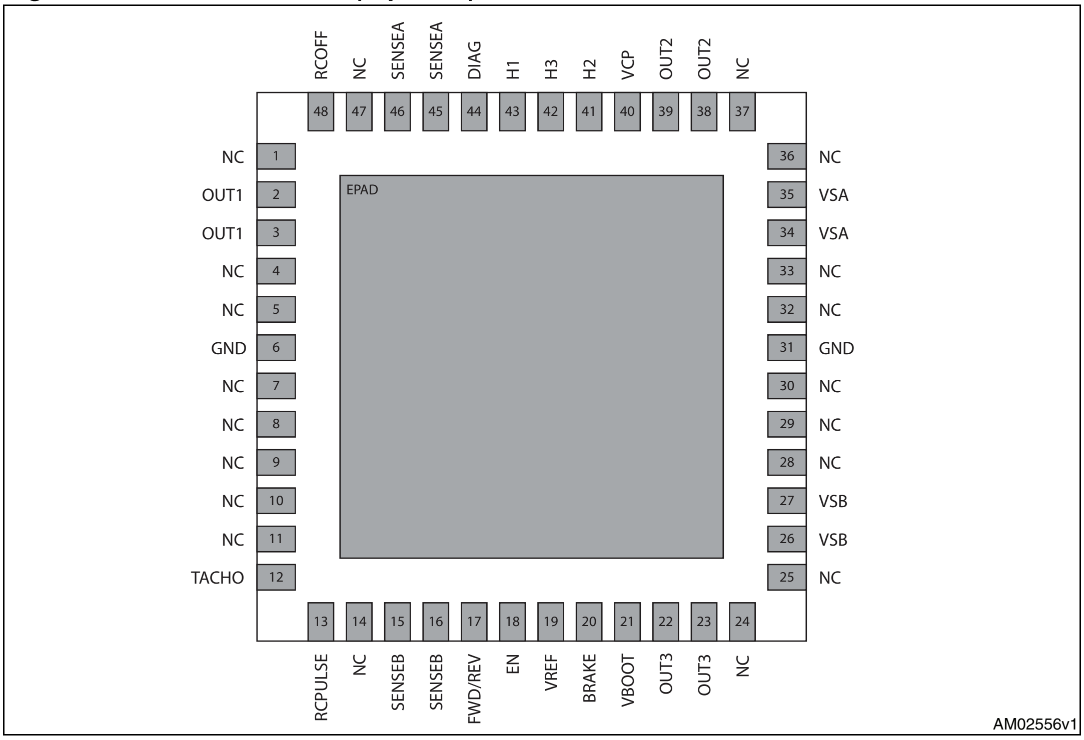
1.2 Recommended operating conditions

Table 2. Recommended operating conditions

Symbol	Parameter	Parameter	Min.	Max.	Unit
V_S	Supply voltage	$VS_A = VS_B = V_S$	8	52	V
V_{OD}	Differential voltage between VS_A, $OUT1_A$, $OUT2_A$, $SENSE_A$ and VS_B, $OUT1_B$, $OUT2_B$, $SENSE_B$	$VS_A = VS_B = V_S$; $V_{SENSEA} = V_{SENSEB}$		52	V
V_{REF}	Voltage range at pin V_{REF}		-0.1	5	V
V_{SENSE}	Voltage range at pins $SENSE_A$ and $SENSE_B$	Pulsed $t_W < t_{rr}$	-6	6	V
		DC	-1	1	V
I_{OUT}	DC output current	$VS_A = VS_B = V_S$;		2.5	A
T_j	Operating junction temperature		-25	+125	°C
f_{sw}	Switching frequency			100	kHz

2 Pin connection

Figure 2. Pin connection (top view)



Note: The exposed PAD must be connected to GND pin.

Table 3. Pin description

Pin	Name	Type	Function
43	H1	Sensor input	Single ended Hall effect sensor input 1.
44	DIAG	Open drain output	Overcurrent detection and thermal protection pin. An internal open drain transistor pulls to GND when an overcurrent on one of the high-side MOSFETs is detected or during thermal protection.
45, 46	$SENSE_A$	Power supply	Half bridge 1 and half bridge 2 source pin. This pin must be connected together with pin $SENSE_B$ to power ground through a sensing power resistor.
48	RC_{OFF}	RC pin	RC network pin. A parallel RC network connected between this pin and ground sets the current controller OFF time.
2, 3	OUT1	Power output	Output 1
6, 31	GND	GND	Ground terminals.
12	TACHO	Open drain output	Frequency-to-voltage open drain output. Every pulse from pin H_1 is shaped as a fixed and adjustable length pulse.
13	RCPULSE	RC pin	RC network pin. A parallel RC network connected between this pin and ground sets the duration of the monostable pulse used for the frequency-to-voltage converter.

Table 3. Pin description (continued)

Pin	Name	Type	Function
15, 16	$SENSE_B$	Power supply	Half bridge 3 source pin. This pin must be connected together with pin $SENSE_A$ to power ground through a sensing power resistor. At this pin also the inverting input of the sense comparator is connected.
17	FWD/REV	Logic input	Selects the direction of the rotation. High logic level sets forward operation, whereas low logic level sets reverse operation. If not used, it must be connected to GND or +5 V.
18	EN	Logic input	Chip enable. Low logic level switches off all power MOSFETs. If not used, it must be connected to +5 V.
19	VREF	Logic input	Current controller reference voltage. Do not leave this pin open or connect to GND.
20	BRAKE	Logic input	Brake input pin. Low logic level switches on all high-side power MOSFETs, implementing the brake function. If not used, it must be connected to +5 V.
21	VBOOT	Supply voltage	Bootstrap voltage needed for driving the upper power MOSFETs.
22, 23	OUT_3	Power output	Output 3.
26, 27	VS_B	Power supply	Half bridge 3 power supply voltage. It must be connected to the supply voltage together with pin VS_A.
34, 35	VS_A	Power supply	Half bridge 1 and half bridge 2 power supply voltage. It must be connected to the supply voltage together with pin VS_B.
38, 39	OUT_2	Power output	Output 2.
40	VCP	Output	Charge pump oscillator output.
41	H_2	Sensor input	Single ended Hall effect sensor input 2.
42	H_3	Sensor input	Single ended Hall effect sensor input 3.

3 Electrical characteristics

V_S = 48 V, T_A = 25 °C, unless otherwise specified.

Table 4. Electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$V_{Sth(ON)}$	Turn-on threshold		6.6	7	7.4	V
$V_{Sth(OFF)}$	Turn-off threshold		5.6	6	6.4	V
I_S	Quiescent supply current	All bridges OFF; Tj = -25 °C to 125 °C (1)		5	10	mA
$T_{j(OFF)}$	Thermal shutdown temperature			165		°C
Output DMOS transistors						
$R_{DS(ON)}$	High-side switch ON resistance	Tj = 25 °C		0.34	0.4	Ω
		Tj =125 °C (1)		0.53	0.59	
	Low-side switch ON resistance	Tj = 25 °C		0.28	0.34	
		Tj =125 °C (1)		0.47	0.53	
I_{DSS}	Leakage current	EN = low; OUT = V_S			2	mA
		EN = low; OUT = GND	-0.15			mA
Source drain diodes						
V_{SD}	Forward ON voltage	I_{SD} = 2.5 A, EN = low		1.15	1.3	V
t_{rr}	Reverse recovery time	If = 2.5 A		300		ns
t_{fr}	Forward recovery time			200		ns
Logic input (H1, H2, H3, EN, FWD/REV, BRAKE)						
V_{IL}	Low level logic input voltage		-0.3		0.8	V
V_{IH}	High level logic input voltage		2		7	V
I_{IL}	Low level logic input current	GND logic input voltage	-10			µA
I_{IH}	High level logic input current	7 V logic input voltage			10	µA
$V_{th(ON)}$	Turn-on input threshold			1.8	2.0	V
$V_{th(OFF)}$	Turn-off input threshold		0.8	1.3		V
$V_{th(HYS)}$	Input threshold hysteresis		0.25	0.5		V
Switching characteristics						
$t_{D(on)EN}$	Enable to out turn ON delay time (2)	I_{LOAD} =2.5 A, resistive load	100	250	400	ns
$t_{D(off)EN}$	Enable to out turn OFF delay time (2)	I_{LOAD} =2.5 A, resistive load	300	550	800	ns
$t_{D(on)IN}$	Other logic inputs to output turn ON delay time	I_{LOAD} =2.5 A, resistive load			2	ns
$t_{D(off)IN}$	Other logic inputs to out turn OFF delay time	I_{LOAD} =2.5 A, resistive load			2	ns

Table 4. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
t_{RISE}	Output rise time (2)	I_{LOAD} =2.5 A, resistive load	40		250	ns
t_{FALL}	Output fall time (2)	I_{LOAD} =2.5 A, resistive load	40		250	ns
t_{DT}	Dead time protection		0.5	1		µs
f_{CP}	Charge pump frequency	Tj = -25 °C to 125 °C (7)		0.6	1	MHz
PWM comparator and monostable						
I_{RCOFF}	Source current at pin RC_{OFF}	V_{RCOFF} = 2.5 V	3.5	5.5		mA
V_{offset}	Offset voltage on sense comparator	V_{REF} = 0.5 V		±5		mV
t_{PROP}	Turn OFF propagation delay (3)			500		ns
t_{BLANK}	Internal blanking time on SENSE comparator			1		µs
$t_{ON(MIN)}$	Minimum ON time			1.5	2	µs
t_{OFF}	PWM recirculation time	R_{OFF} = 20 kΩ; C_{OFF} = 1 nF		13		µs
		R_{OFF} = 100 kΩ; C_{OFF} = 1 nF		61		µs
I_{BIAS}	Input bias current at pins $VREF_A$ and $VREF_B$				10	µA
Tacho monostable						
$I_{RCPULSE}$	Source current at pin RCPULSE	$V_{RCPULSE}$ = 2.5 V	3.5	5.5		mA
t_{PULSE}	Monostable of time	R_{PUL} = 20 kΩ; C_{PUL} =1 nF		12		µs
		R_{PUL} = 100 kΩ; C_{PUL} =1 nF		60		µs
R_{TACHO}	Open drain ON resistance			40	60	Ω
Over current detection e protection						
I_{sover}	Supply overcurrent protection threshold	-25 °C<Tj <125 °C	4.0	5.6	7.1	A
R_{OPDR}	Open drain ON resistance	I = 4 mA		40	60	Ω
I_{OH}	OCD high level leakage current	V_{DIAG} = 5 V		1		µA
$t_{OCD(ON)}$	OCD turn-on delay time (4)	I = 4 mA; CEN < 100 pF		200		ns
$t_{OCD(OFF)}$	OCD turn-off delay time (4)	I = 4 mA; CEN < 100 pF		100		ns

1. Tested at 25 °C in a restricted range and guaranteed by characterization.
2. See *Figure 3*.
3. Measured applying a voltage of 1 V to pin SENSE and a voltage drop from 2 V to 0 V to pin V_{REF}.
4. See *Figure 4*.

Figure 3. Switching characteristic definition

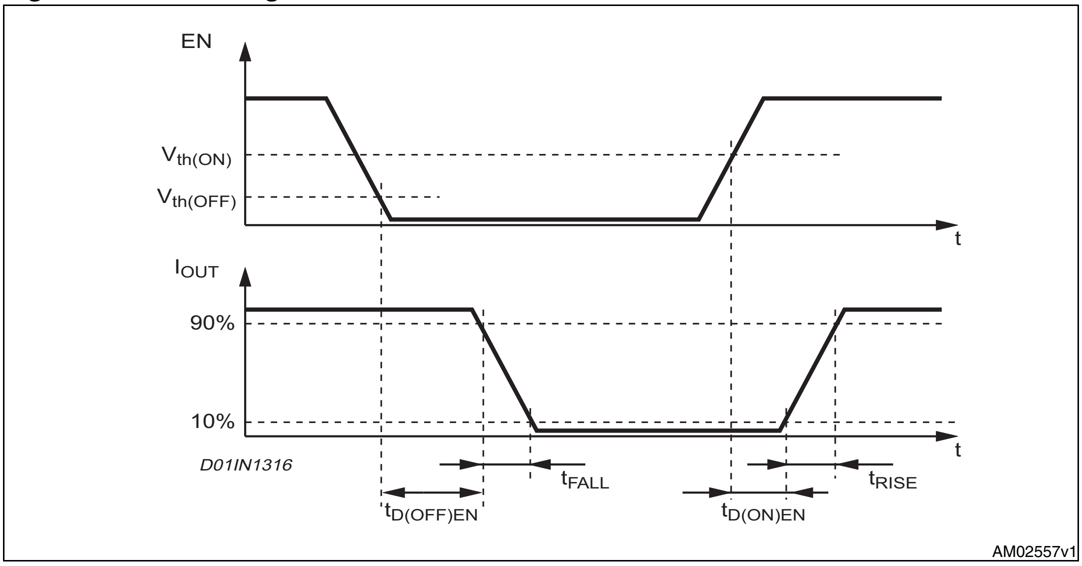
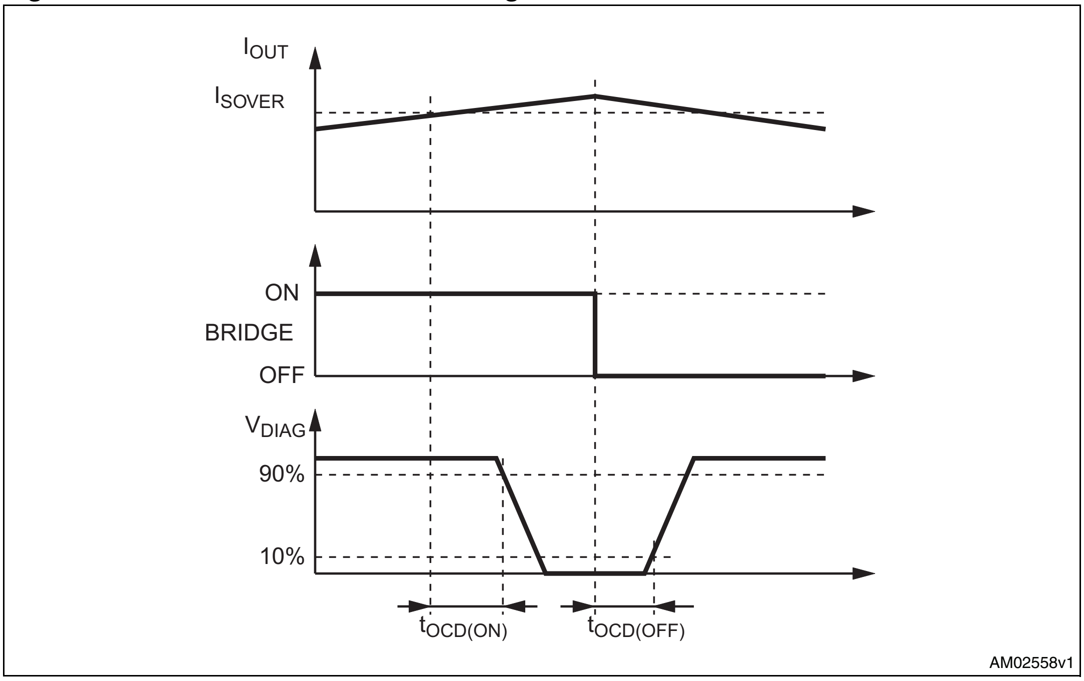


Figure 4. Overcurrent detection timing definition



4 Circuit description

4.1 Power stages and charge pump

The L6235Q integrates a 3-phase bridge, which consists of 6 power MOSFETs connected as shown in *Figure 1*, each power MOSFET has an $R_{DS(ON)}$ = 0.3 Ω (typical value @ 25 °C) with intrinsic fast freewheeling diode. Switching patterns are generated by the PWM current controller and the Hall effect sensor decoding logic (*Chapter 4.3 on page 11*). Cross conduction protection is implemented by using a dead time (t_{DT} = 1 µs typical value) set by internal timing circuit between the turn-off and turn-on of two power MOSFETs in one leg of a bridge.

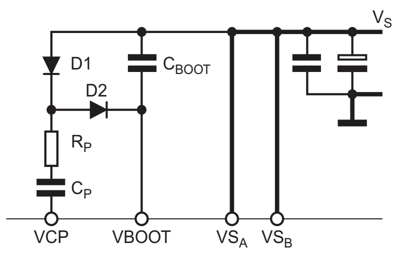
Pins VS_A and VS_B must be connected together to the supply voltage (V_S).

Using an N-channel power MOSFET for the upper transistors in the bridge requires a gate drive voltage above the power supply voltage. The bootstrapped supply (V_{BOOT}) is obtained through an internal oscillator and a few external components to realize a charge pump circuit, as shown in *Figure 5*. The oscillator output (pin VCP) is a square wave at 600 kHz (typically) with 10 V amplitude. Recommended values/part numbers for the charge pump circuit are shown in *Table 5*.

Table 5. Charge pump external component values

Component	Value
C_{BOOT}	220 nF
C_P	10 nF
R_P	100 Ω
D1	1N4148
D2	1N4148

Figure 5. Charge pump circuit



4.2 Logic inputs

Pins FWD/REV, BRAKE, EN, H1, H2 and H3 are TTL/CMOS and µC compatible logic inputs. The internal structure is shown in *Figure 6*. Typical value for turn-on and turn-off thresholds are respectively V_{thon}=1.8 V and V_{thoff} = 1.3 V.

Pin EN (enable) may be used to implement overcurrent and thermal protection by connecting it to the open collector DIAG output. If the protection and an external disable function are both desired, the appropriate connection must be implemented. When the external signal is from an open collector output, the circuit in *Figure 7* may be used. For external circuits that are push-pull outputs the circuit in *Figure 8* may be used. The resistor R_{EN} should be chosen in the range from 2.2 kΩ to 180 kΩ. Recommended values for R_{EN} and C_{EN} are respectively 100 kΩ and 5.6 nF. More information for selecting the values can be found in *Section 4.7*.

Figure 6. Logic inputs internal structure

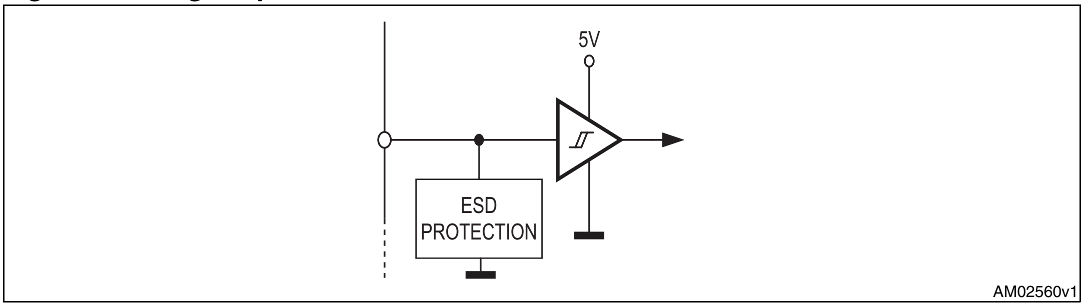


Figure 7. EN pins open collector driving

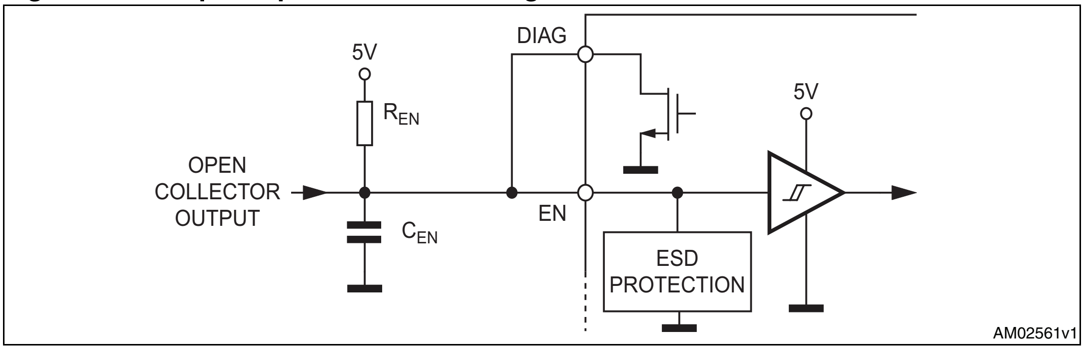
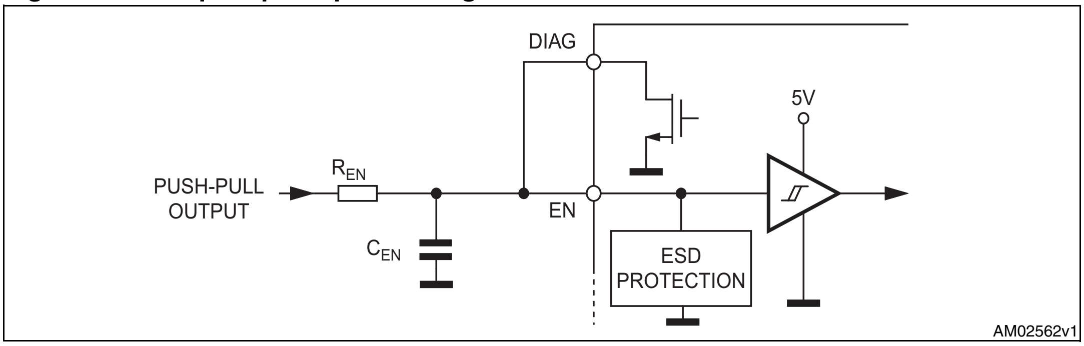


Figure 8. EN pins push-pull driving



4.3 PWM current control

The L6235Q includes a constant OFF time PWM current controller. The current control circuit senses the bridge current by sensing the voltage drop across an external sense resistor connected between the source of the three lower power MOSFET transistors and ground, as shown in *Figure 9*. As the current in the motor increases, the voltage across the sense resistor increases proportionally. When the voltage drop across the sense resistor becomes greater than the voltage at the reference input pin V_{REF}, the sense comparator triggers the monostable switching the bridge off. The power MOSFET remains off for the time set by the monostable and the motor current recirculates around the upper half of the bridge in slow decay mode, as described in *Section 4.4*. When the monostable times out, the bridge again turns on. Since the internal dead time, used to prevent cross conduction in the bridge, delays the turn-on of the power MOSFET, the effective OFF time t_{OFF} is the sum of the monostable time plus the dead time.

Figure 10 shows the typical operating waveforms of the output current, the voltage drop across the sensing resistor, the pin RC voltage and the status of the bridge. More details regarding the synchronous rectification and the output stage configuration are included in *Section 4.4*.

Immediately after the power MOSFET turns on, a high peak current flows through the sense resistor due to the reverse recovery of the freewheeling diodes. The L6235 provides a 1µs blanking time t_{BLANK} that inhibits the comparator output so that the current spike cannot prematurely re-trigger the monostable.

Figure 9. PWM current controller simplified schematic

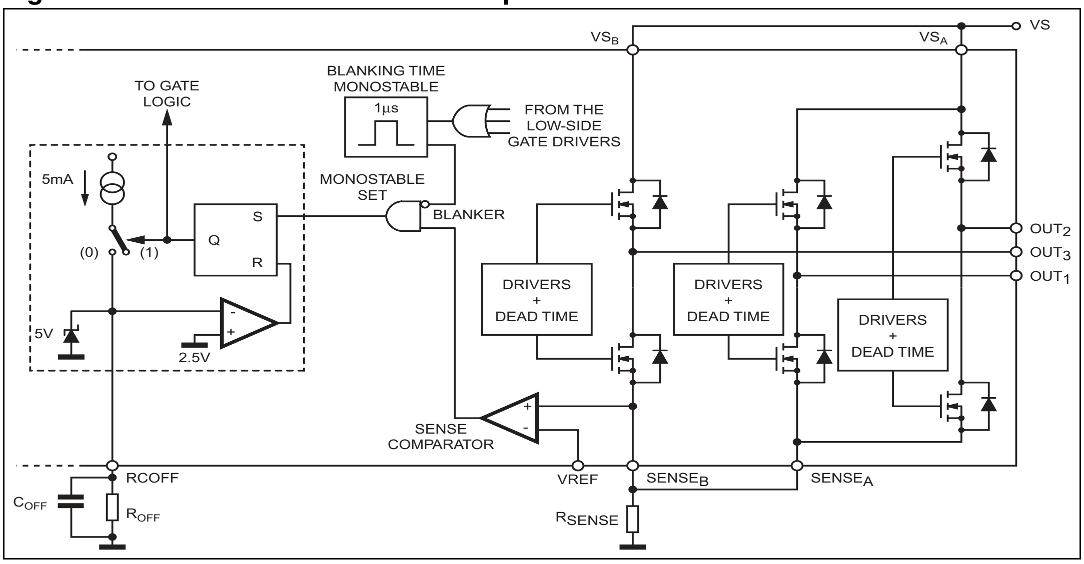


Figure 10. Output current regulation waveforms

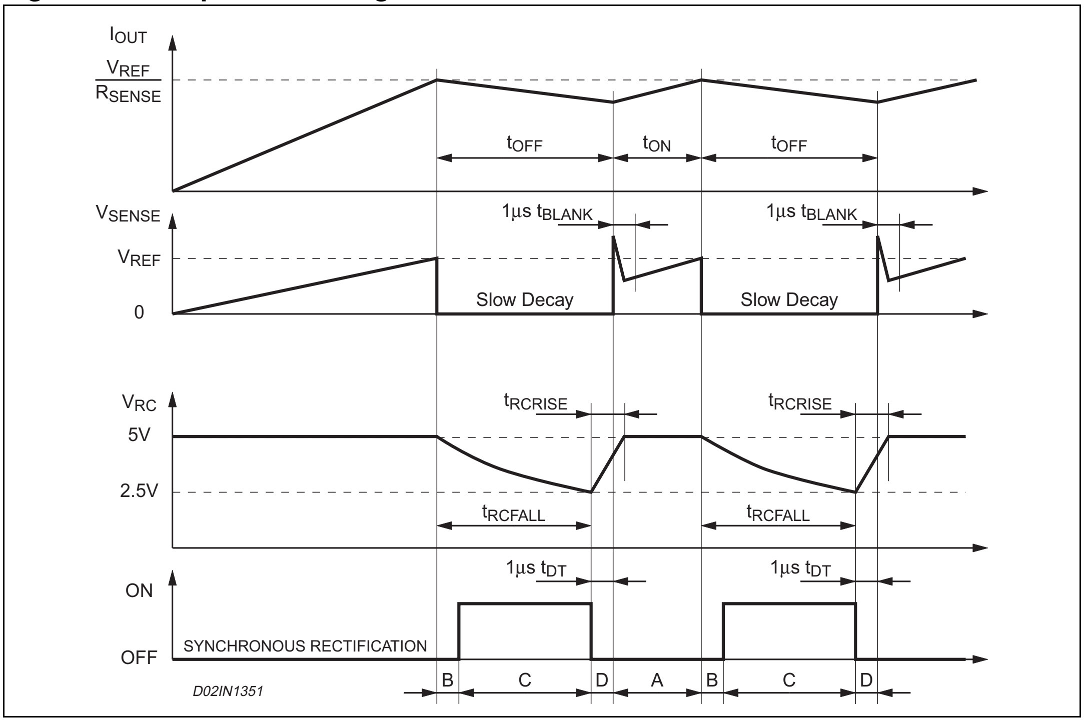


Figure 11 shows the magnitude of the OFF time t_{OFF} versus C_{OFF} and R_{OFF} values. It can be approximately calculated from the equations:

$$t_{RCFALL} = 0.6 \cdot R_{OFF} \cdot C_{OFF}$$

$$t_{OFF} = t_{RCFALL} + t_{DT} = 0.6 \cdot R_{OFF} \cdot C_{OFF} + t_{DT}$$

where R_{OFF} and C_{OFF} are the external component values and t_{DT} is the internally generated dead time with:

$$20\ k\Omega \leq R_{OFF} \leq 100\ k\Omega$$

$$0.47\ nF \leq C_{OFF} \leq 100\ nF$$

$$t_{DT} = 1\ \mu s \text{ (typical value)}$$

therefore:

$$t_{OFF(MIN)} = 6.6\ \mu s$$

$$t_{OFF(MAX)} = 6\ ms$$

These values allow a sufficient range of t_{OFF} to implement the drive circuit for most motors.

The capacitor value chosen for C_{OFF} also affects the rise time t_{RCRISE} of the voltage at the pin R_{COFF}. The rise time t_{RCRISE} is only an issue if the capacitor is not completely charged before the next time the monostable is triggered. Therefore, the ON time t_{ON}, which depends on motors and supply parameters, must be bigger than t_{RCRISE} to allow a good current regulation by the PWM stage. Furthermore, the ON time t_{ON} can not be smaller than the minimum ON time $t_{ON(MIN)}$.

$$\begin{cases} t_{ON} > t_{ON(MIN)} & = 1.5\mu s(typ) \\ t_{ON} > t_{RCRISE} - t_{DT} \end{cases}$$

$$t_{RCRISE} = 600 \cdot C_{OFF}$$

Figure 12 shows the lower limit for the ON time t_{ON} for having a good PWM current regulation capacity. It should be mentioned that t_{ON} is always bigger than $t_{ON(MIN)}$ because the device imposes this condition, but it can be smaller than t_{RCRISE} - t_{DT}. In this last case the device continues to work but the OFF time t_{OFF} is not more constant.

Therefore, a small C_{OFF} value gives more flexibility to the applications (allows smaller ON time and, therefore, higher switching frequency), but, the smaller the value for C_{OFF}, the more influential the noises on the circuit performance.

Figure 11. t_{OFF} vs. C_{OFF} and R_{OFF}

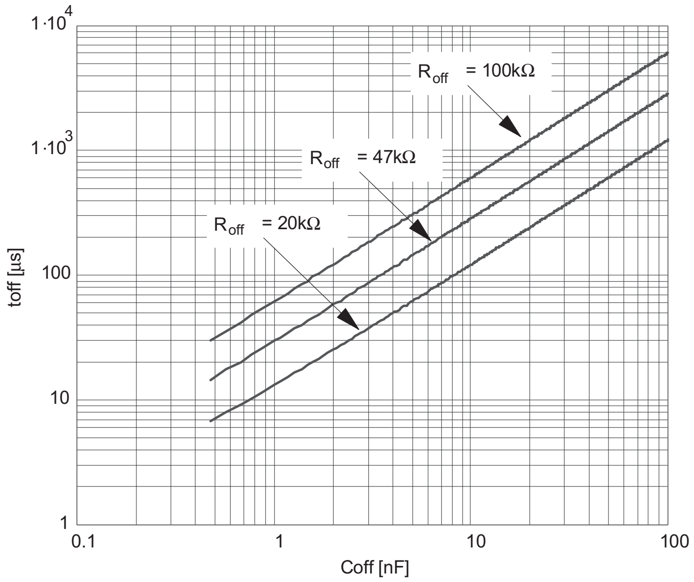
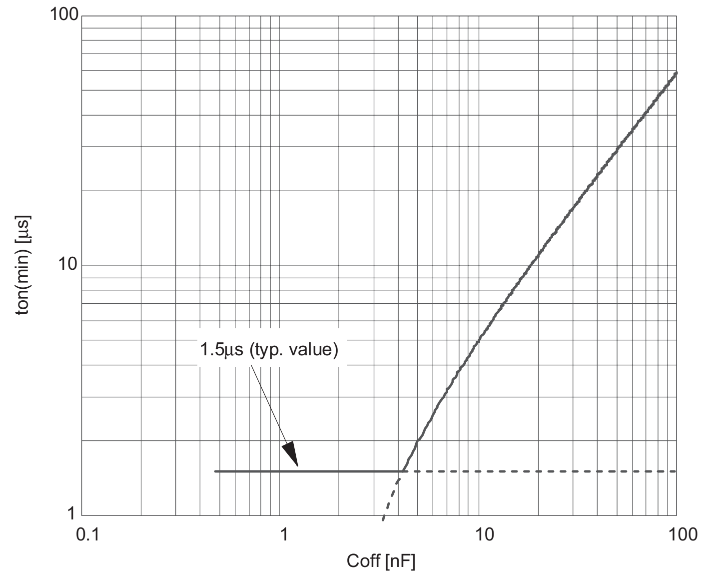


Figure 12. Area where t_{ON} can vary maintaining the PWM regulation

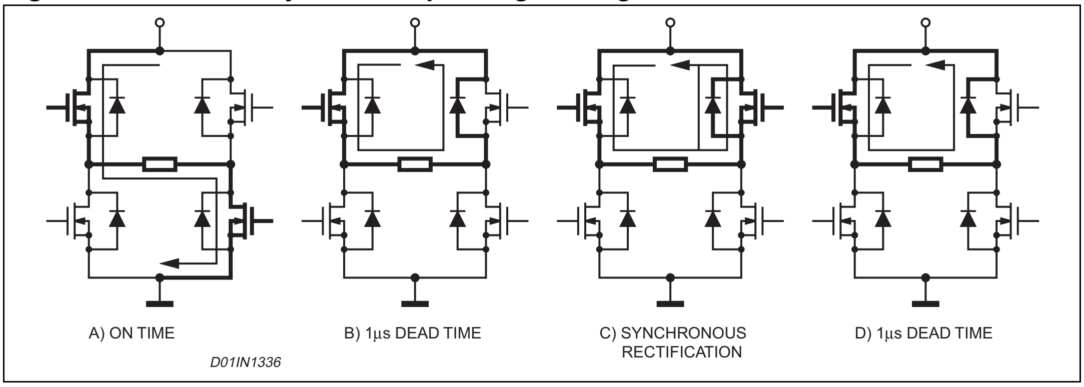


4.4 Slow decay mode

Figure 13 shows the operation of the bridge in slow decay mode during the OFF time. At any time only two legs of the 3-phase bridge are active, therefore, only the two active legs of the bridge are shown in the figure and the third leg is off. At the start of the OFF time, the lower power MOSFET is switched off and the current recirculates around the upper half of the bridge. Since the voltage across the coil is low, the current decays slowly.

After the dead time the upper power MOSFET is operated in the synchronous rectification mode reducing the impedance of the freewheeling diode and the related conducting losses. When the monostable times out, the upper power MOSFET that was operating the synchronous mode turns off and the lower power MOSFET is turned on again after some delay set by the dead time to prevent cross conduction.

Figure 13. Slow decay mode output stage configurations



4.5 Decoding logic

The decoding logic section is a combinatory logic that provides the appropriate driving of the 3-phase bridge outputs according to the signals coming from the three Hall sensors that detect rotor position in a 3-phase BLDC motor. This novel combinatory logic discriminates between the actual sensor positions for sensors spaced at 60, 120, 240 and 300 electrical degrees. This decoding method allows the implementation of a universal IC without dedicating pins to select the sensor configuration.

There are eight possible input combinations for three sensor inputs. Six combinations are valid for rotor positions with 120 electrical degrees sensor phasing (see *Figure 14*, positions 1, 2, 3a, 4, 5 and 6a) and six combinations are valid for rotor positions with 60 electrical degrees phasing (see *Figure 15*, positions 1, 2, 3b, 4, 5 and 6b). Four of them are used in common (1, 2, 4 and 5) whereas there are two combinations used only in 120 electrical degrees sensor phasing (3a and 6a) and two combinations used only in 60 electrical degrees sensor phasing (3b and 6b).

The decoder can drive motors with different sensor configurations simply by following *Table 2*. For any input configuration (H1, H2 and H3) there is one output configuration (OUT_1, OUT_2 and OUT_3). The output configuration 3a is the same as 3b and analogously output configuration 6a is the same as 6b.

The sequence of the Hall codes for 300 electrical degrees phasing is the reverse of 60 and the sequence of the Hall codes for 240 phasing is the reverse of 120. So, by decoding the 60 and the 120 codes it is possible to drive the motor with all four conventions by changing the direction set.

Table 6. 60 and 120 electrical degree decoding logic in forward direction

Hall 120°	1	2	3a	-	4	5	6a	-
Hall 60°	1	2	-	3b	4	5	-	6b
H1	H	H	L	H	L	L	H	L
H2	L	H	H	H	H	L	L	L
H3	L	L	L	H	H	H	H	L
OUT1	Vs	High Z	GND	GND	GND	High Z	Vs	Vs
OUT2	High Z	Vs	Vs	Vs	High Z	GND	GND	GND
OUT3	GND	GND	High Z	High Z	Vs	Vs	High Z	High Z
Phasing	1->3	2->3	2->1	2->1	3->1	3->2	1->2	1->2

Figure 14. 120° Hall sensor sequence

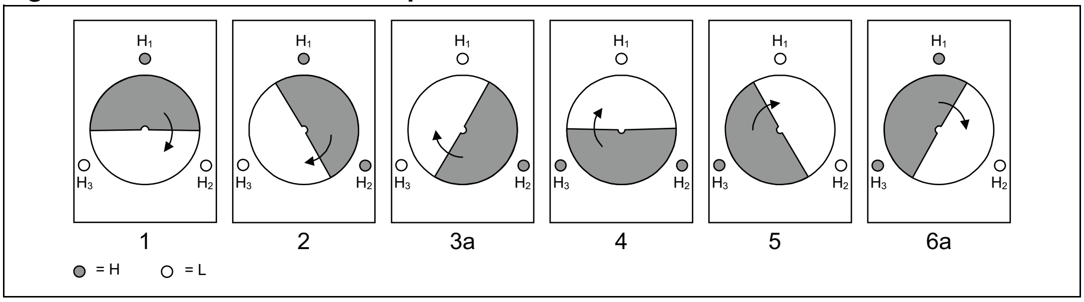
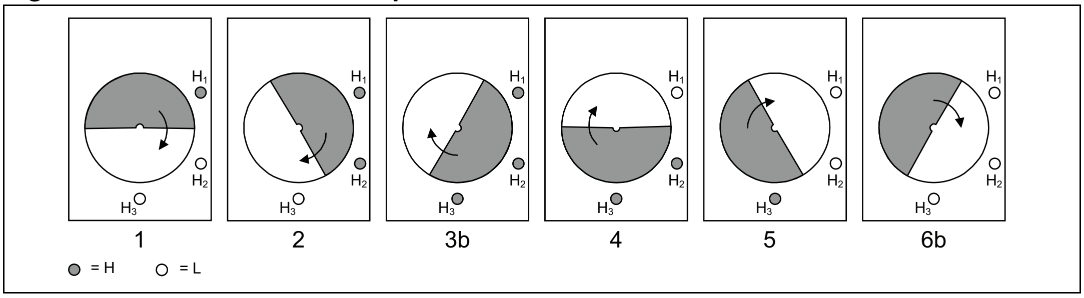


Figure 15. 60° Hall sensor sequence



4.6 Tacho

The tachometer function consists of a monostable, with constant OFF time (t_{PULSE}), whose input is one Hall effect signal (H_1). It allows to develop an easy speed control loop by using an external op amp, as shown in *Figure 17*. For component values refer to *Section 5*.

The monostable output drives an open drain output pin (TACHO). At each rising edge of the Hall effect sensors H1, the monostable is triggered and the MOSFET connected to pin TACHO is turned off for a constant time t_{PULSE} (see *Figure 16*). The OFF time t_{PULSE} can be set using the external RC network (R_{PUL}, C_{PUL}) connected to the pin RCPULSE. *Figure 18* gives the relation between t_{PULSE} and C_{PUL}, R_{PUL}. It is approximately:

$$t_{PULSE} = 0.6 \cdot R_{PUL} \cdot C_{PUL}$$

where C_{PUL} should be chosen in the range 1 nF … 100 nF and R_{PUL} in the range 20 kΩ … 100 kΩ.

By connecting the tachometer pin to an external pull-up resistor, the output signal average value VM is proportional to the frequency of the Hall effect signal and, therefore, to the motor speed. This realizes a simple frequency-to-voltage converter. An op amp, configured as an integrator, filters the signal and compares it with a reference voltage V_{REF}, which sets the speed of the motor.

$$V_M = \frac{t_{PULSE}}{T} \cdot V_{DD}$$

Figure 16. Tacho operation waveforms

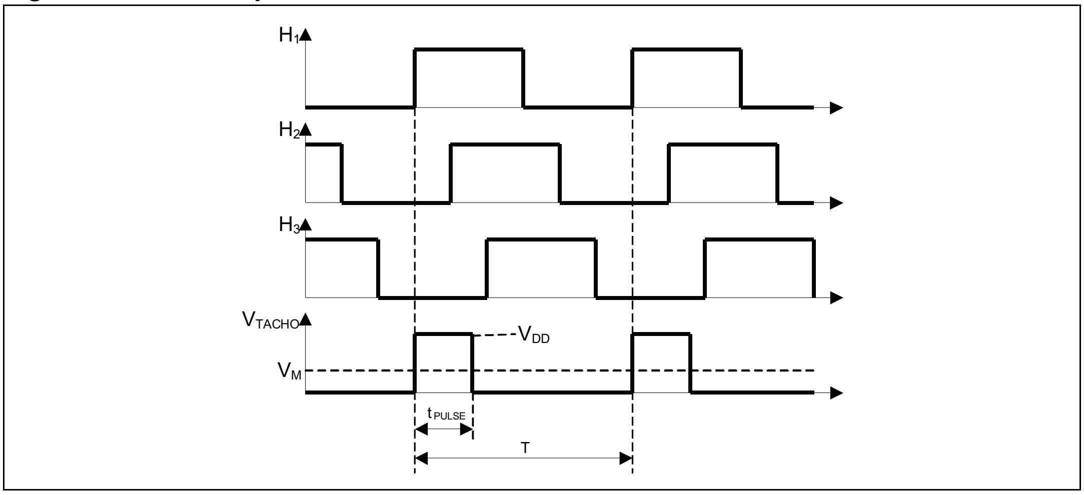


Figure 17. Tachometer speed control loop

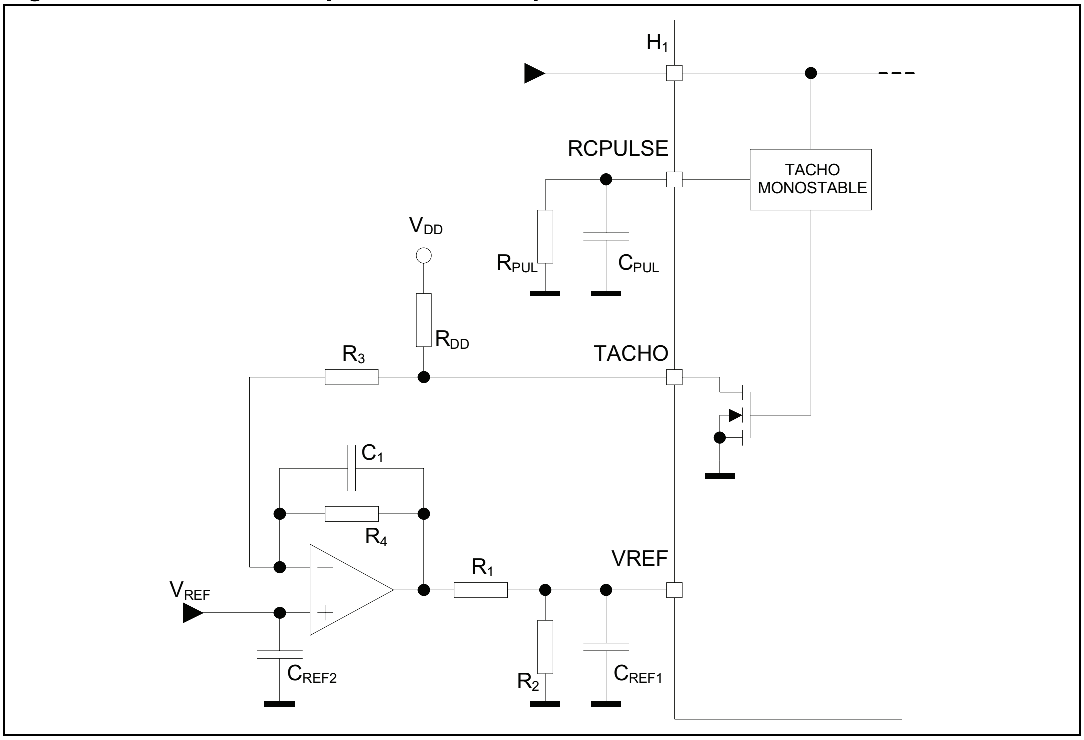
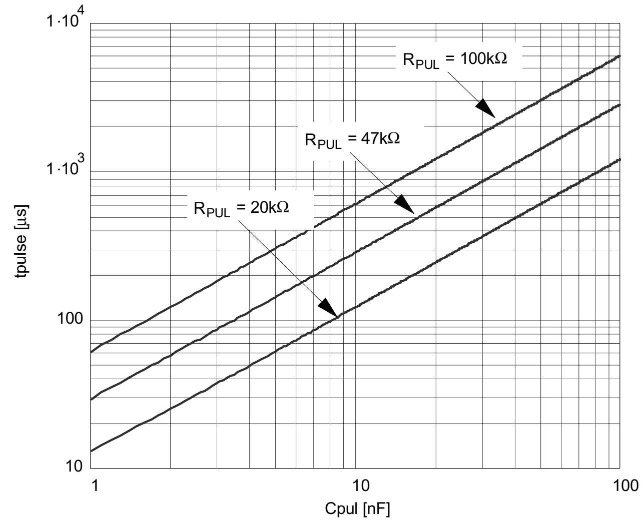


Figure 18. t_{PULSE} vs. C_{PUL} and R_{PUL}



4.7 Non-dissipative overcurrent detection and protection

The L6235Q integrates an overcurrent detection circuit (OCD) for full protection. With this internal overcurrent detection, the external current sense resistor normally used and its associated power dissipation are eliminated. *Figure 19* shows a simplified schematic of the overcurrent detection circuit.

To implement the overcurrent detection, a sensing element that delivers a small but precise fraction of the output current is implemented with each high-side power MOSFET. Since this current is a small fraction of the output current there is very little additional power dissipation. This current is compared with an internal reference current I_{REF}. When the output current reaches the detection threshold (typically I_{SOVER} = 5.6 A), the OCD comparator signals a fault condition. When a fault condition is detected, an internal open drain MOSFET with a pull-down capability of 4 mA connected to pin DIAG is turned on.

Pin DIAG can be used to signal the fault condition to a µC or to shut down the 3-phase bridge simply by connecting it to pin EN and adding an external R-C (see R_{EN}, C_{EN}).

Figure 19. Overcurrent protection simplified schematic

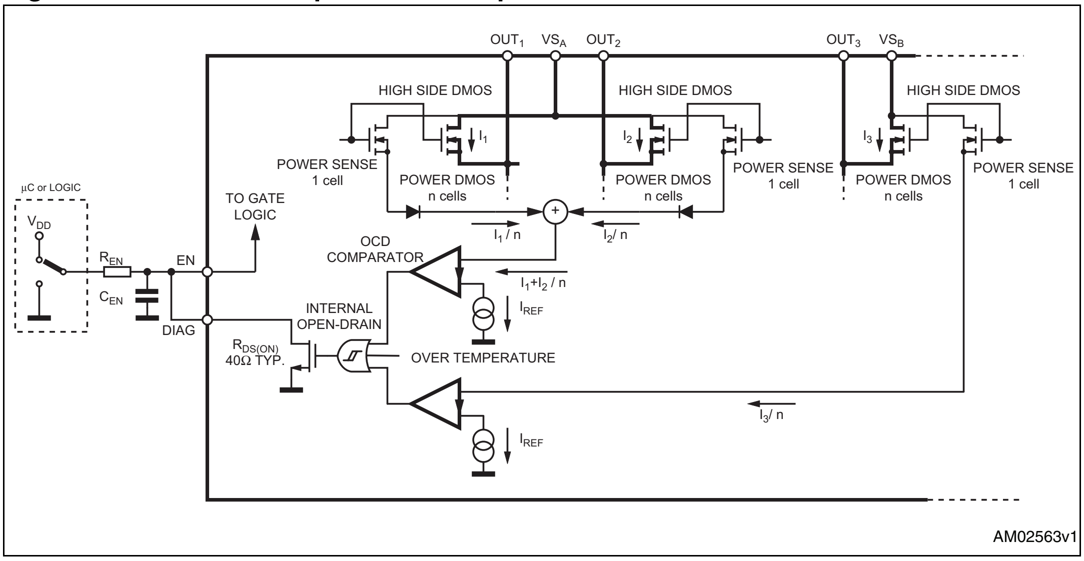


Figure 20 shows the overcurrent detection operation. The disable time $t_{DISABLE}$ before recovering normal operation can be easily programmed by means of the accurate thresholds of the logic inputs. It is affected by both C_{EN} and R_{EN} values and its magnitude is reported in *Figure 21*. The delay time t_{DELAY} before turning off the bridge, when an overcurrent has been detected, depends only on the C_{EN} value. Its magnitude is reported in *Figure 22*.

C_{EN} is also used for providing immunity to pin EN against fast transient noises. Therefore the value of C_{EN} should be chosen as big as possible according to the maximum tolerable delay time and the R_{EN} value should be chosen according to the desired disable time.

The resistor R_{EN} should be chosen in the range from 2.2 kΩ to 180 kΩ. Recommended values for R_{EN} and C_{EN} are respectively 100 kΩ and 5.6 nF which allow to obtain 200 µs disable time.

Figure 20. Overcurrent protection waveforms

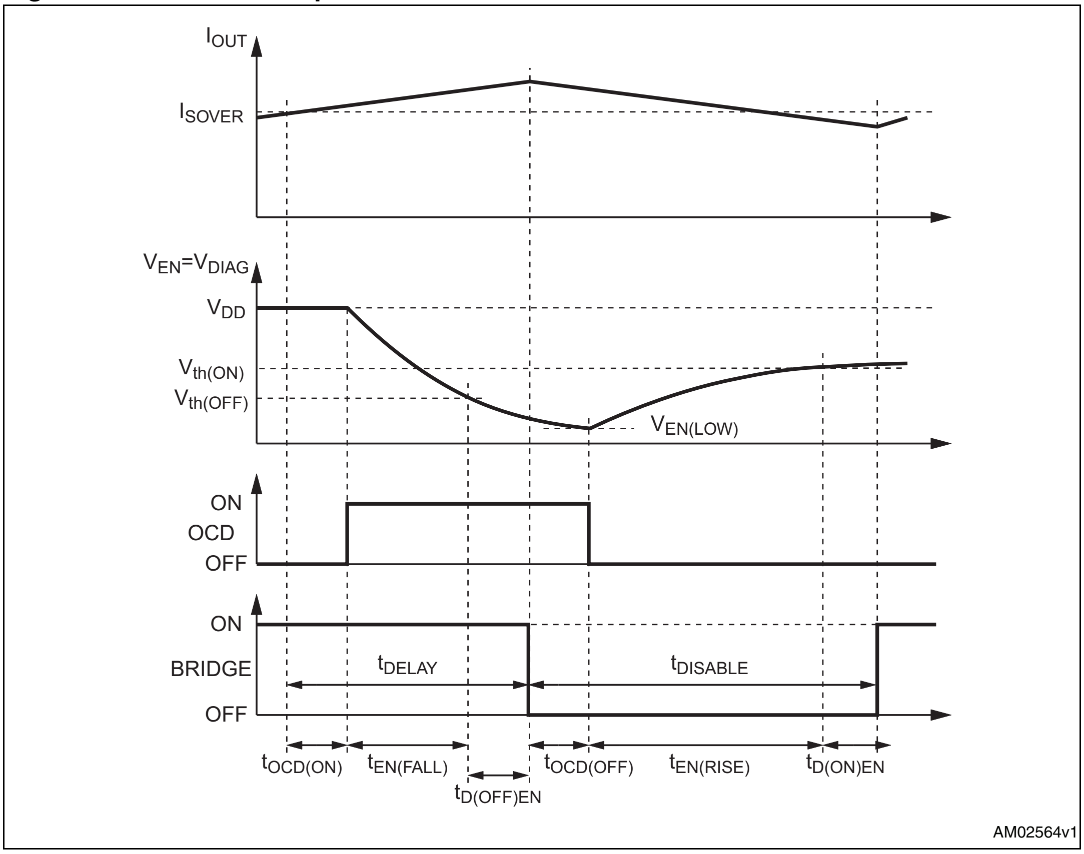


Figure 21. $t_{DISABLE}$ vs. C_{EN} and R_{EN} (V_{DD} = 5 V)

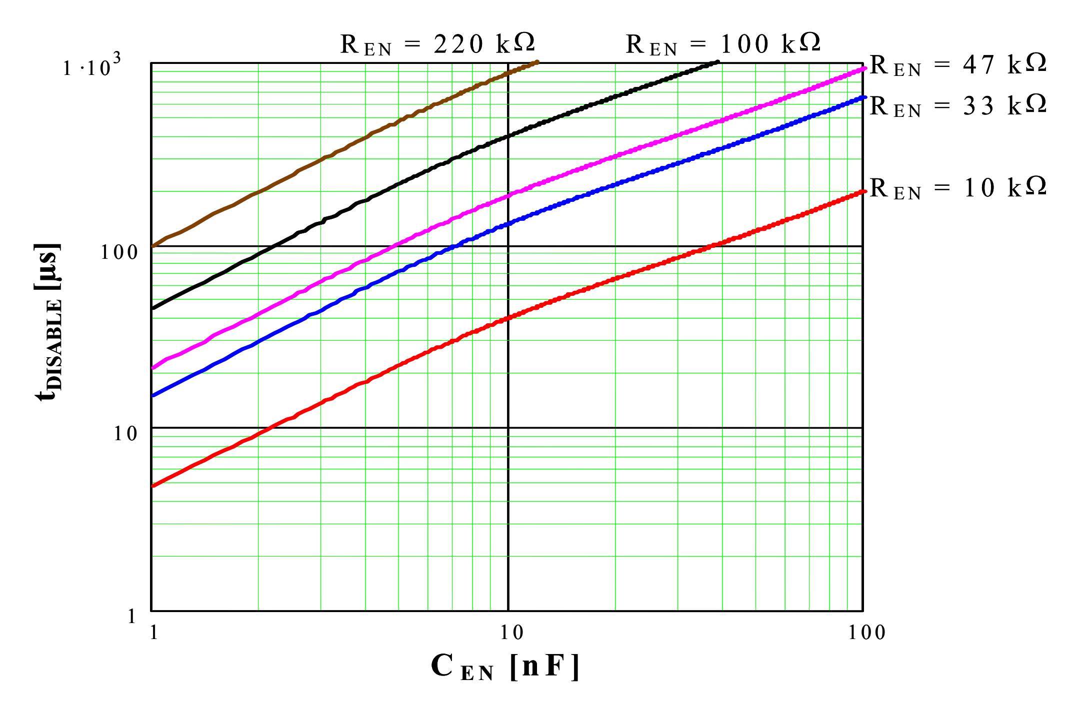
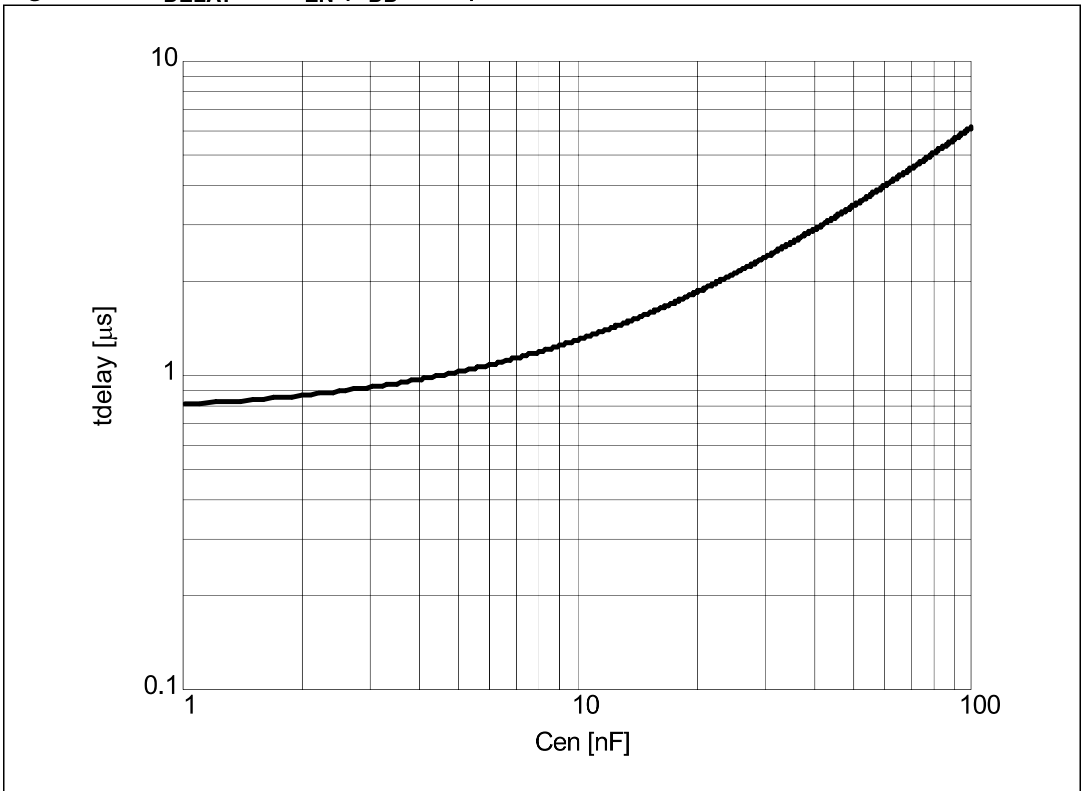


Figure 22. t_{DELAY} vs. C_{EN} (V_{DD} = 5 V)



4.8 Thermal protection

In addition to the overcurrent detection, the L6235Q integrates a thermal protection to prevent device destruction in case of junction overtemperature. It works sensing the die temperature by means of a sensitive element integrated in the die. The device switches off when the junction temperature reaches 165 °C (typ. value) with 15 °C hysteresis (typ. value).

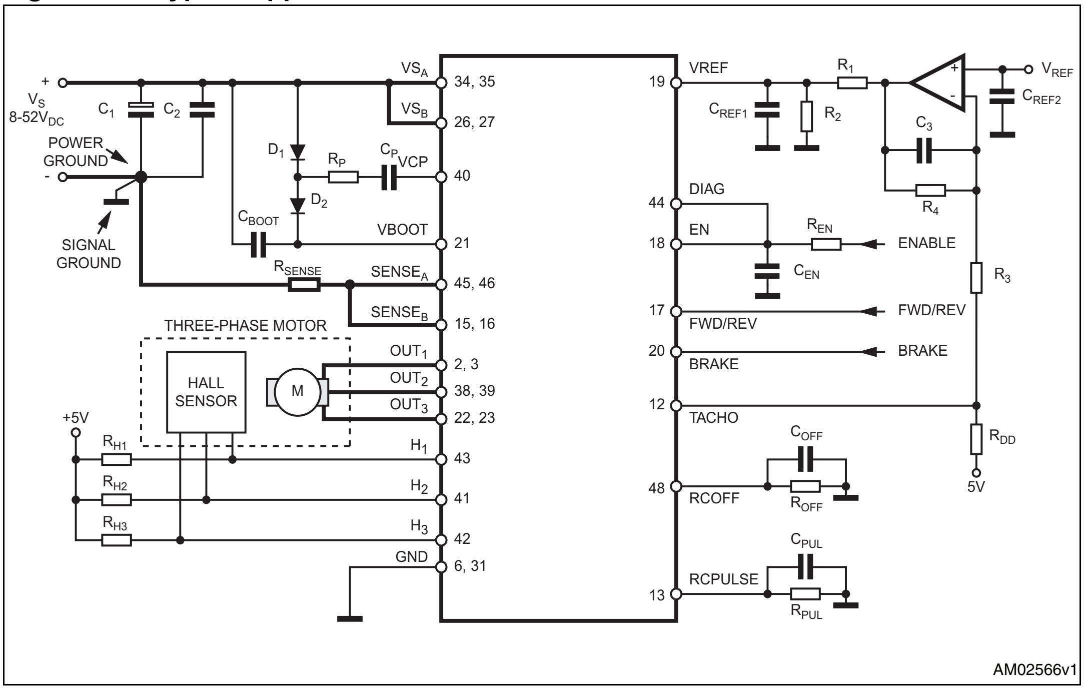
5 Application information

A typical application using L6235Q is shown in *Figure 23*. Typical component values for the application are shown in *Table 7*. A high quality ceramic capacitor (C_2) in the range of 100 to 200 nF should be placed between the power pins (VS_A and VS_B) and ground near the L6235Q to improve the high frequency filtering on the power supply and reduce high frequency transients generated by the switching. The capacitors (C_{EN}) connected from the EN input to ground sets the shutdown time when an overcurrent is detected (see *Section 4.7*). The two current sensing inputs ($SENSE_A$ and $SENSE_B$) should be connected to the sensing resistors R_{SENSE} with a trace length as short as possible in the layout. The sense resistors should be non-inductive resistors to minimize the di/dt transients across the resistor. To increase noise immunity, unused logic pins are best connected to 5 V (high logic level) or GND (low logic level) (see *Section 2*). It is recommended to keep power ground and signal ground separated on the PCB.

Table 7. Component values for typical application

Component	Value
C_1	100 uF
C_2	100 nF
C_3	220 nF
C_{BOOT}	220 nF
C_{OFF}	1 nF
C_{PUL}	10 nF
C_{REF1}	33 nF
C_{REF2}	100 nF
C_{EN}	5.6 nF
C_P	10 nF
D_1	1N4148
D_2	1N4148
R_1	5K6Ω
R_2	1K8Ω
R_3	4K7Ω
R_4	1 MΩ
R_{DD}	1 KΩ
R_{EN}	100 kΩ
R_P	100 Ω
R_{SENSE}	0.3 Ω
R_{OFF}	33 kΩ
R_{PUL}	47 kΩ
R_{H1}, R_{H2}, R_{H3}	10 kΩ

Figure 23. Typical application



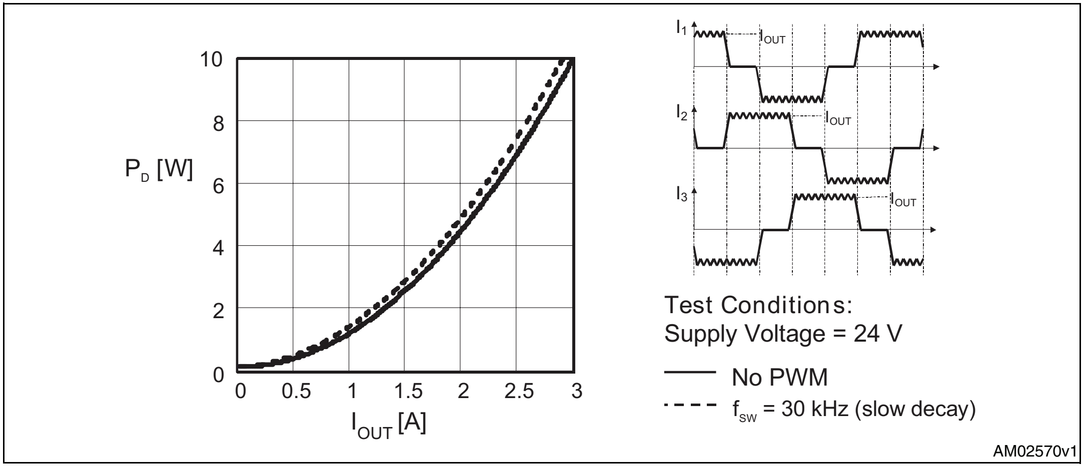
Note: *To reduce the IC thermal resistance, therefore improving the dissipation path, the NC pins can be connected to GND.*

6 Output current capability and IC power dissipation

Figure 24 shows the approximate relation between the output current and the IC power dissipation using PWM current control.

For a given output current the power dissipated by the IC can be easily evaluated, in order to establish which package should be used and how large the onboard copper dissipating area must be to guarantee a safe operating junction temperature (125 °C maximum).

Figure 24. IC power dissipation vs. output power



7 Thermal management

In most applications the power dissipation in the IC is the main factor that sets the maximum current that can be delivered by the device in a safe operating condition. Selecting the appropriate package and heatsinking configuration for the application is required to maintain the IC within the allowed operating temperature range for the application.

8 Electrical characteristics curves

Figure 25. Typical quiescent current vs. supply voltage

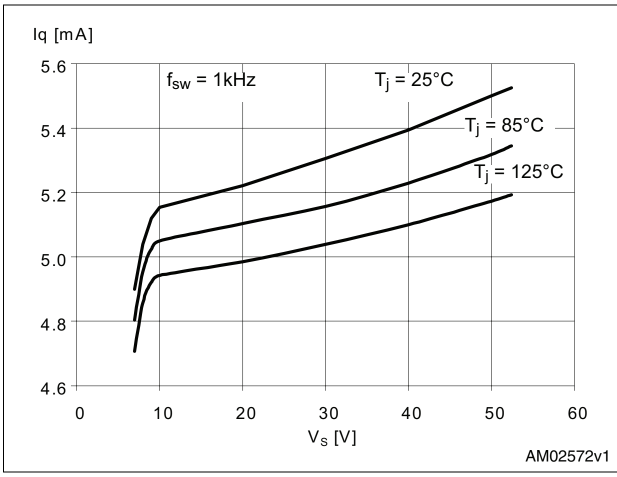


Figure 26. Typical high-side $R_{DS(on)}$ vs. supply voltage

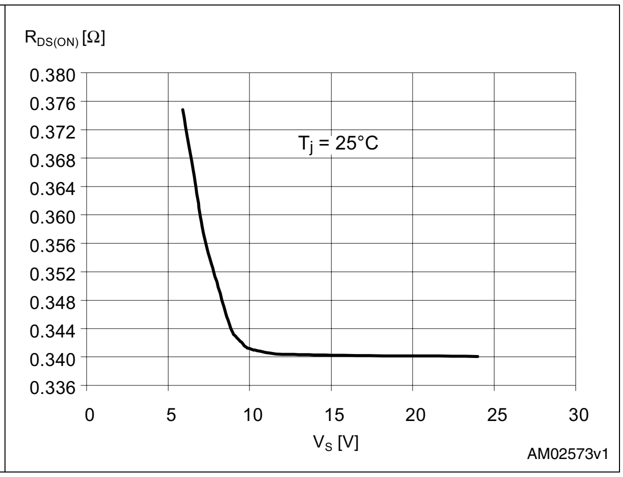


Figure 27. Normalized typical quiescent current vs. switching frequency

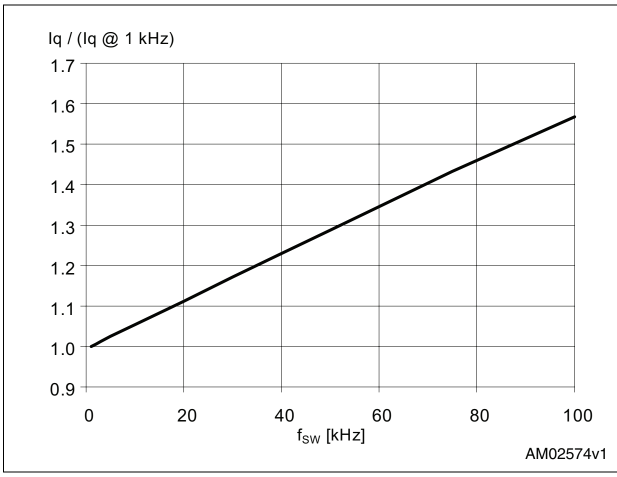


Figure 28. Normalized $R_{DS(on)}$ vs. junction temperature (typical value)

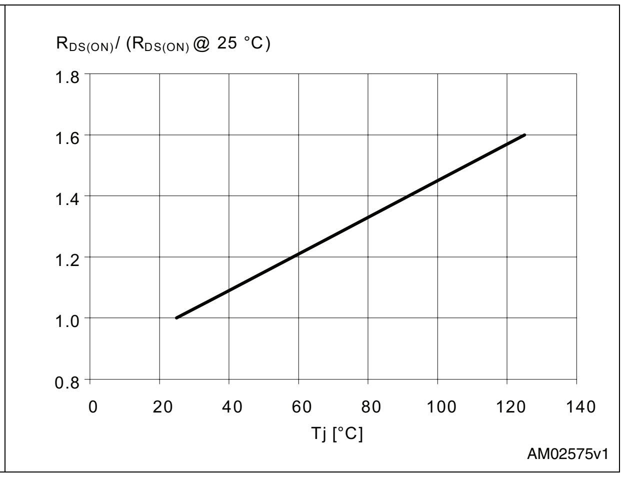


Figure 29. Typical low-side $R_{DS(on)}$ vs. supply voltage

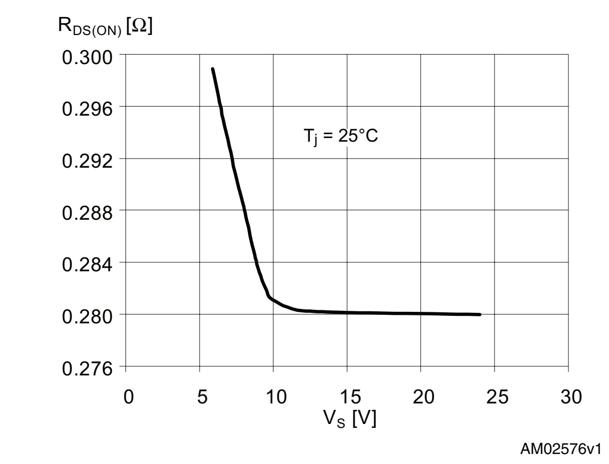
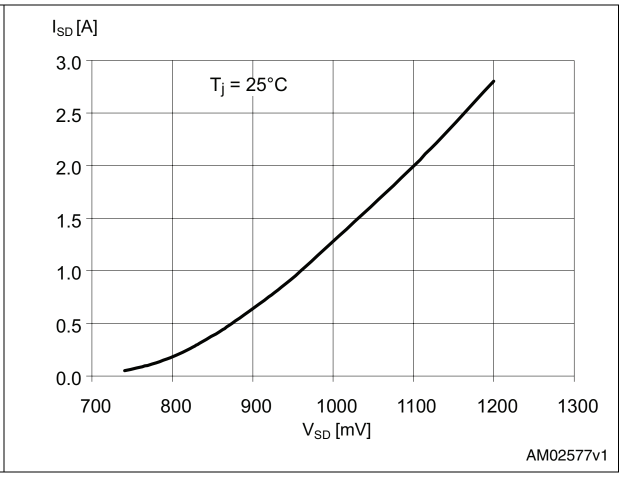


Figure 30. Typical drain-source diode forward ON characteristic



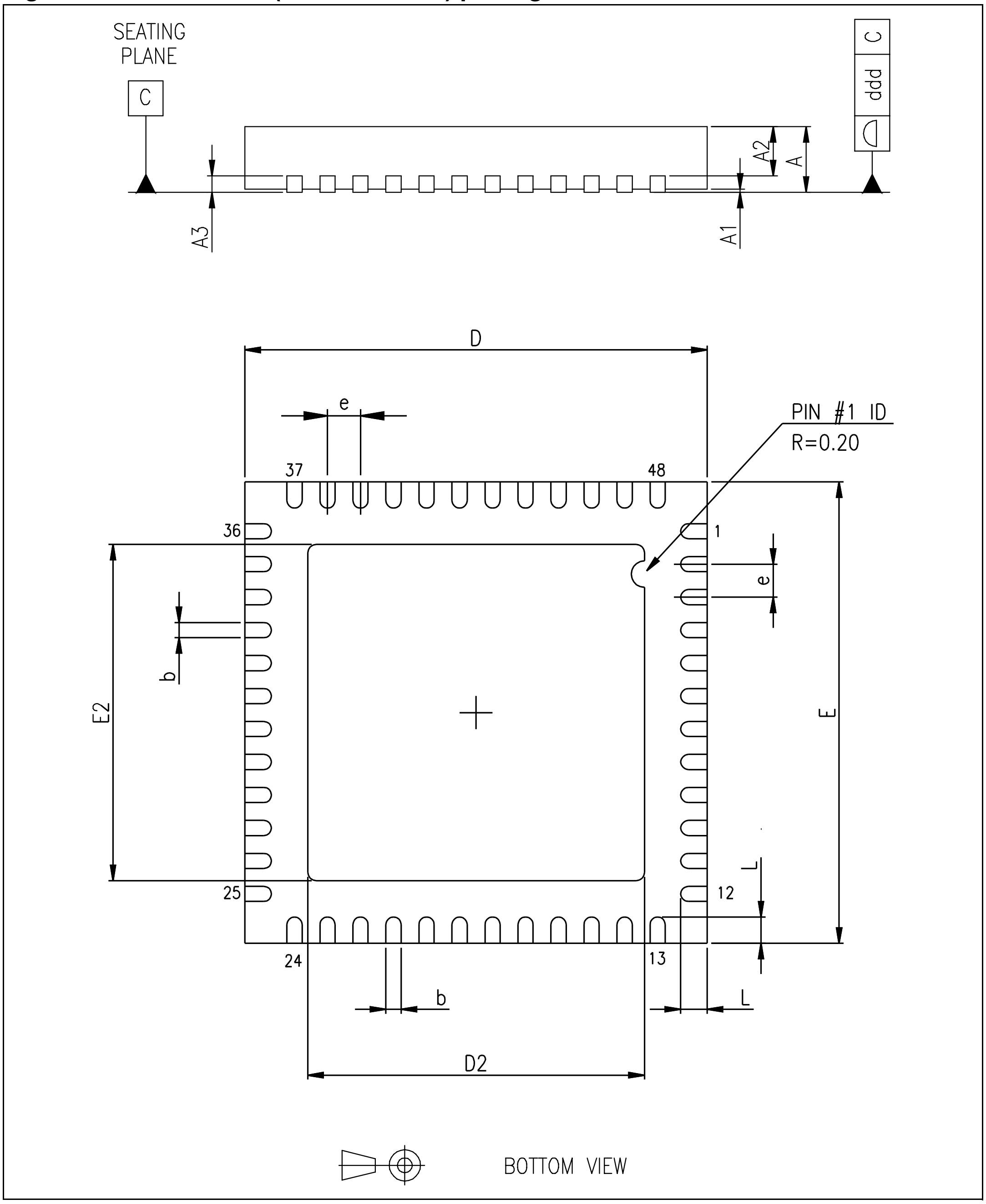
9 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 8. VFQFPN48 (7 x 7 x 1.0 mm) package mechanical data

Dim.	(mm)		
	Min.	Typ.	Max.
A	0.80	0.90	1.00
A1		0.02	0.05
A2		0.65	1.00
A3		0.25	
b	0.18	0.23	0.30
D	6.85	7.00	7.15
D2	4.95	5.10	5.25
E	6.85	7.00	7.15
E2	4.95	5.10	5.25
e	0.45	0.50	0.55
L	0.30	0.40	0.50
ddd		0.08	

Figure 31. VFQFPN48 (7 x 7 x 1.0 mm) package outline



10 Order codes

Table 9. Ordering information

Order codes	Package	Packaging
L6235Q	QFN48 7 x 7 x 1.0 mm	Tray
L6235QTR		Tape and reel

11 Revision history

Table 10. Document revision history

Date	Revision	Changes
30-Jul-2011	1	First release
28-Nov-2011	2	Document moved from preliminary to final datasheet