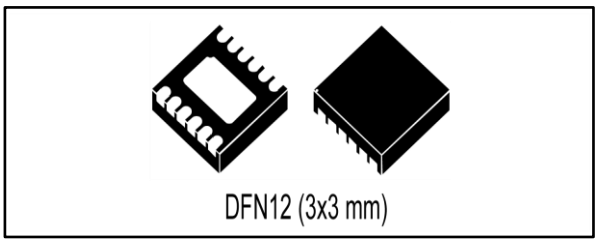
L6362A

IO-Link communication transceiver device IC

Datasheet - production data



Features

- Supply voltage from 7 V to 36 V
- 5 V and 3.3 V compatible I/Os
- 5 V or 3.3 V, 10 mA selectable linear regulator
- 0.3 A output current intervention threshold
- Fully protected
  - Reverse polarity
  - Overload with cut-off function
  - Overtemperature
  - Undervoltage and overvoltage
  - GND and V_{CC} open wire
- -40 to +125 °C operating ambient temperature
- Selectable output stages: high-side, low-side, push-pull
- Suitable to drive L, C and R loads
- 30 µF output load drive capability
- Switching capability of inductors up to 500 mJ
- Wake-up detection supported
- Fast demagnetization of inductive loads
- COM1, COM2 and COM3 mode supported
- Designed to meet:
  - Burst IEC 61000-4-4
  - ESD IEC 61000-4-2
  - Surge EN60947-5-2
- Miniaturized VFDFPN 12L (3x3x0.90 mm) package

Applications

- Industrial sensors
- Factory automation
- Process control

Description

The L6362A is an IO-Link and SIO mode transceiver device compliant to PHY2 (3-wire connection) supporting COM1 (4.8 kbaud), COM2 (38.4 kbaud) and COM3 (230.4 kbaud) modes. The output stage can be configured as high-side, low-side or push-pull and it can drive resistive, capacitive and inductive loads. It can be connected to a sensor chip with the industrial 24 V environment. The industrial environment could be a PLC, an IO-Link master, a relay or a valve. The L6362A is protected against reverse polarity, among VCC, GND, OUTH, OUTL and I/Q pins. Furthermore, the IC is protected against output short-circuit, overvoltage and impulse voltage withstand (±1 kV pulse amplitude,1.2/50 µs pulse duration, 500 Ω source impedance).

Table 1: Device summary

Order code	Package	Packing
L6362ATR	VFDFPN 12L (3x3x0.90 mm)	Tape and reel

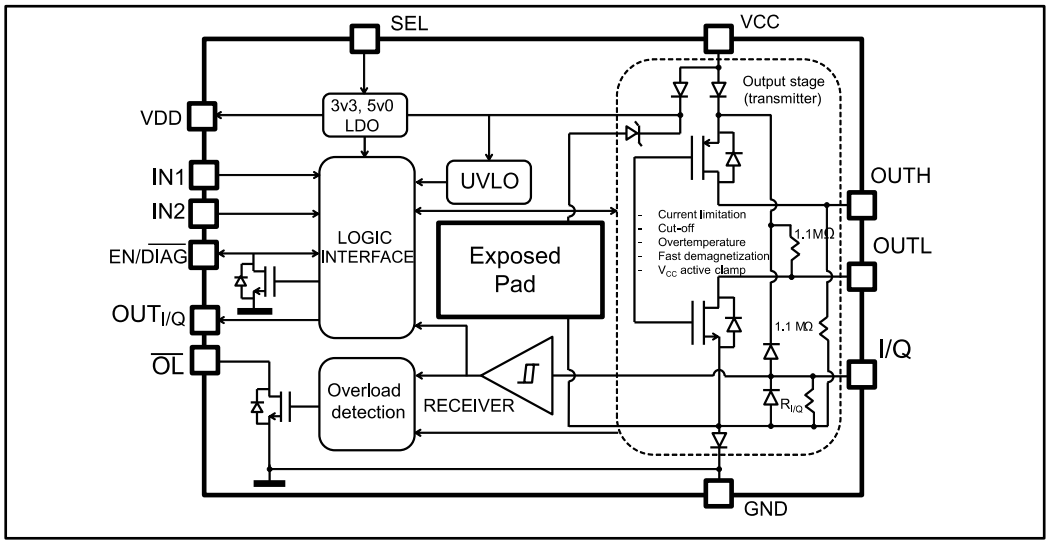
Contents

List of tables

List of figures

1 Block diagram

Figure 1: Block diagram



2 Pin description

Figure 2: Pin connection (top through view)

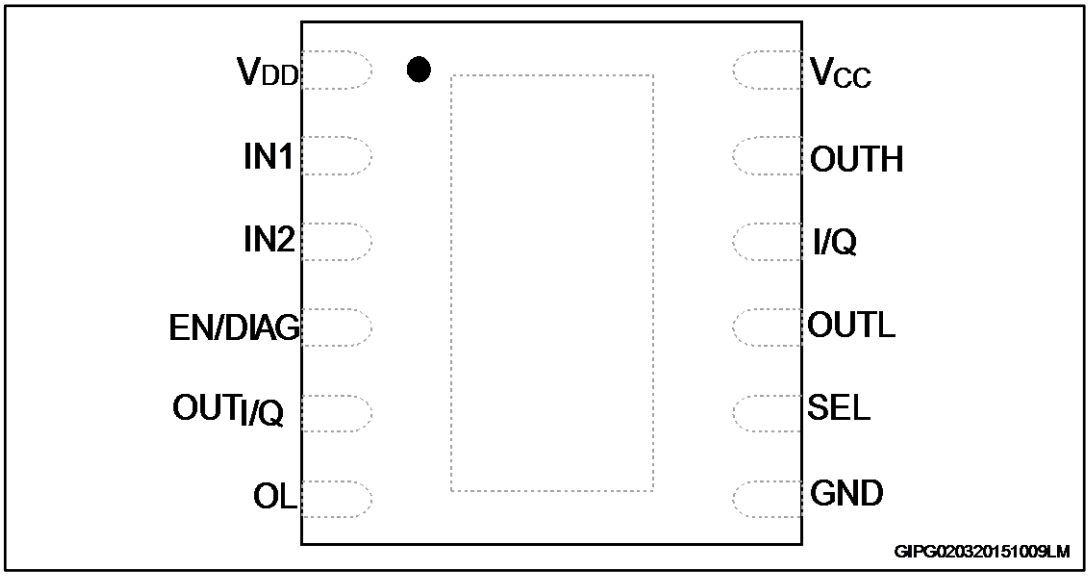


Table 2: Pin description

Number	Name	Function	Type
1	V_{DD}	Linear regulator output voltage	Output
2	IN1	Digital input	Input
3	IN2	Digital input	Input
4	EN/DIAG	Output enable/fault diagnostic	Input/output open drain
5	$OUT_{I/Q}$	I/Q channel logic output	Output
6	OL	Overload (diagnostic)	Output (open drain)
7	GND	IC ground	Supply
8	SEL	Linear regulator output voltage selection	Input
9	OUTL	LS channel output	Output
10	I/Q	I/Q receiver line	Input
11	OUTH	HS channel output	Output
12	V_{CC}	IC supply voltage	Supply
13	Exposed pad	Not connected	

In order to guarantee all features and protections, the exposed pad cannot be electrically connected to any other net. To improve the thermal performance, it can be connected to a floating copper area.

2.1 IN1, IN2

These pins control the output stage on OUTH and OUTL pins, see *Table 14: "Output stage truth table"*. When used in push-pull configuration (OUTH and OUTL wired together), the IC must be driven by the IN2 pin, to allow the dead time function to protect the output stage. The IN1 pin can be wired to GND or V_{DD} depending on the desired polarity. In order to avoid IC overstress, in push-pull configuration, IN1 pin has to be hardwired to V_{DD} or GND. IN1 could be also actively controlled, but must be switched only while EN/DIAG pin is at a low logic level. When used in high-side (OUTL left unconnected) or low-side (OUTH left unconnected) configurations, the IC should be driven by the IN1 pin, in order to avoid the unnecessary delay, which is introduced by the dead time function. The pin IN2 can be wired to GND or V_{DD} depending on the desired polarity, or can be actively controlled (for example by a microcontroller).

2.2 EN/DIAG

This pin controls the output stage on pins OUTH and OUTL. When EN/DIAG is at a low logic level (GND), the output stage is disabled. The EN/DIAG pin is also internally wired to an open drain transistor, used for diagnostic purposes and must be driven through a series resistor. The open drain transistor turns on in case of faults. EN/DIAG pin has an internal weak pull-down resistor. If the OUTH and OUTL pins are wired together the IC can be still used in HS or LS mode (with slow demagnetization) by applying a fixed high or low level voltage to IN1 pin, using the IN2 pin to set the polarity and the EN/DIAG pin to control the power stage.

2.3 OUT I/Q

This pin reports the status of the receiver line (I/Q). It swings from GND to V_{DD} and should generally be connected to a microcontroller input. $OUT_{I/Q}$ relation to I/Q is shown in *Table 14: "Output stage truth table"* .

2.4 SEL

This pin cannot be left floating and it allows the linear regulator output voltage to be configured at 3.3 V or 5 V.

Table 3: Linear regulator voltage configuration

SEL	V_{DD} supplied voltage
GND	3.3 V
V_{DD}	5 V

2.5 VDD

This is the output of the integrated linear voltage regulator and the supply voltage of the I/O interface. It can supply a small current (I_{scr}) to a microcontroller or external circuitry. The integrated liner regulator could supply the whole system, provided that the amount of required current is within IC limits, or the system can be supplied by an external regulator and the regulator integrated in the IC supplies the integrated logic only.

2.6 GND

IC ground.

2.7 OL

This pin has an open drain structure and is active low. The open drain is active in case of overload (current limitation). It can be used by the host microcontroller to detect an IO-Link wake-up request event.

2.8 VCC

IC supply voltage.

2.9 OUTH

This pin is the output of the high-side power transistor.

2.10 OUTL

This pin is the output of the low-side power transistor.

2.11 I/Q

Input pin of the integrated receiver. The level of the signal on I/Q pin is transferred to the OUTI/Q pin, according to the receiver thresholds defined in *Table 8: "Output stage"*, and truth table see *Table 14: "Output stage truth table"*. In IO-Link mode, OUTH and OUTL outputs have to be connected to the load. I/Q pin has to be connected to the load as well, through a 22 kΩ resistor. If it is not used, this pin can remain floating; it has to be connected to GND to improve EMC robustness.

3 Absolute maximum ratings

Table 4: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage (steady-state)	-36 to +36	V
	Supply voltage transient(1)	Internally limited	
V_{OUTH} V_{OUTL}	HS or LS output channel voltage (steady-state)	-36 to +36	V
	HS or LS output channel voltage (transient) (1)	Internally limited	
$V_{I/Q}$	I/Q channel voltage (steady-state)	-36 to +36	
	I/Q channel voltage (transient) (1)	Internally limited	
$V_{IN1, IN2}$	IN voltage	-0.3 to V_{DD}+0.3	V
V_{EN}	EN/DIAG voltage	-0.3 to V_{DD}+0.3	V
V_{SEL}	SEL voltage	-0.3 to V_{DD}+0.3	V
V_{OL}	OL voltage	-0.3 to V_{DD}+0.3	V
$I_{OUTH,OUTL}$	Output stage current (continuous) (1)	Internally limited	A
I_{CC}	Supply current	2(2)	A
$I_{OUT\_I/Q}$	$OUT_{I/Q}$ current	-10/+10	mA
I_{OL}	OL	-10/+10	mA
I_{EN}	EN/DIAG current	-10/+10	
P_D	Power dissipation	Internally limited	W
T_J	Junction temperature	-40 to 150	°C
T_{Stor}	Storage temperature range	-55 to 150	

Notes:

(1)During fast transients according to IEC61000-4-5 (±1 kV, RC coupling R=500 Ω, C=18 µF).

(2)Peak value during fast transient test only.

Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. All voltages are referred to GND.

Table 5: Thermal data

Symbol	Parameter	Value	Unit
$R_{th(JC)}$	Thermal resistance junction-case	2.5	°C/W
$R_{th(JA)}$	Thermal resistance junction-ambient. (FR4, Cu thick. 35 µm, 2 layers, the exposed pad is not soldered to total exposed area = 5 mm^2)	200	
	Thermal resistance junction-ambient. (FR4, Cu thick. 35 µm, 2 layers, the exposed pad is soldered to total exposed area = 5 mm^2)	100	

Symbol	Parameter	Value	Unit
	Thermal resistance junction-ambient. (FR4, Cu thick. 35 µm, 2 layers, the exposed pad has to be soldered to total exposed area = 100 mm^2 with vias)	50	

4 Recommended operating conditions

Table 6: Recommended operating conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply voltage	7		36	V
C_{VCC}	Capacity on V_{CC} pin	1			µF
C_{VDD}	Capacity on V_{DD} pin	47		68	nF

C_{VDD} higher than recommend values is allowed but external protection nets on V_{DD} could be necessary for high V_{CC} slew rate (>15 V/µs).

5 Electrical characteristics

(7 V < V_{CC} < 36 V; -40 °C < T_J < 125 °C, unless otherwise specified)

Table 7: Supply

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{UVON}	Undervoltage on threshold		5.5		6.5	V
V_{UVOFF}	Undervoltage off threshold		5.1		5.9	V
V_{UVH}	Undervoltage hysteresis		300			mV
I_{CC}	Supply current	V_{CC} = 24 V, no-load on output stage and V_{DD}, EN/DIAG=1	1.2		2.3	mA
		V_{CC} = 36 V, no-load on output stage and V_{DD}, EN/DIAG=1	1.4		2.5	
		V_{CC} = 5 V, no-load on output stage and V_{DD}, EN/DIAG=1			0.8	
		V_{CC} = 24 V, no-load on output stage and V_{DD}, EN/DIAG=0			2	
SR	Maximum slew rate of V_{CC} increase from off condition to avoid current pulse on output stage (I_{OUT} < 10 mA)	OUTH = GND or OUTL = V_{CC}, EN=GND V_{CC} = 36 V		1.5		V/µs

Table 8: Output stage

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$R_{DS(on)}$	High-side on-state resistance	I_{OUT} = 0.1 A @ T_J = 25 °C		1		Ω
		I_{OUT} = 0.1 A @ T_J = 125 °C			1.6	
	Low-side on-resistance	I_{OUT} = 0.1 A @ T_J = 25 °C		0.8		
		I_{OUT} = 0.1 A @ T_J = 125 °C			1.4	
V_{OLHS}	OUTH output voltage	V_{CC} = 24 V; open load; EN/DIAG=0			3	V
V_{OLLS}	OUTL output voltage	V_{CC} = 24 V; open load; EN/DIAG = 0	V_{CC}-3			V
I_{Olk}	Output leakage current HS	Output leakage current (HS) IN1 = GND, IN2 = GND, EN = V_{DD} and OUTH = GND		1	10	µA
	Output leakage current LS	Output leakage current (LS) IN1 = V_{DD}, IN2 = GND, EN = V_{DD} and OUTL = V_{CC}		0.7	10	µA
I_{OPP}	Current from OUT pin in PP	Output current (PP) EN = GND and OUT = V_{CC} or OUT = GND			70	µA

Table 9: I/Q receiver

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{I/QTHLH}$	I/Q upper voltage threshold	8 V < V_{CC} < 18 V	61.1		69.4	%V_{CC}
		V_{CC} ≥ 18 V	11	11.75	12.5	V
$V_{I/QTHHL}$	I/Q lower voltage threshold	8 V < V_{CC} < 18 V	47.2		61.1	%V_{CC}
		V_{CC} ≥ 18 V	8.5	9.75	11	V
V_{QHY}	I/Q hysteresis voltage	V_{CC} ≥ 18 V	0.8	2		V
$R_{I/Q}$	Weak pull-down on I/Q pin		250		550	kΩ
t_{dbq}	I/Q debounce time		30	50	110	ns

Table 10: Timing VCC = 24 V

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
DT_{HS-LS}	Dead time between HS switch-off and LS switch-on (push-pull configuration)	IN2 commutations only $LOAD_H$ = 120 Ω between OUT and GND; $LOAD_L$ = 120 Ω between OUT and V_{CC}		110		ns
DT_{LS-HS}	Dead time between LS switch-off and HS switch-on (push-pull configuration)			140		
$t_{pI/Q}$	I/Q to $OUT_{I/Q}$ propagation delay time				200	
t_{pOUT}	INx (or EN/DIAG) to OUTH or OUTL propagation delay time	EN/DIAG = V_{DD}, IN1 commutations in HS or LS configurations only. R-L load (120 Ω, 10 µH) to GND in HS; to V_{CC} in LS			370	ns
		EN/DIAG=V_{DD}, IN2 commutations in PP configuration only. R-L load (120 Ω, 10 µH) to GND for high, low transitions of the output; to V_{CC} for low, high transitions			270	ns
		EN/DIAG commutations in HS or LS configurations only. R-L load (120 Ω, 10 µH) to GND in HS; to V_{CC} in LS			400	ns
$t_{r(ON)}$	OUT_X and I/Q rise time (from V_{CC} 10% to V_{CC} 80%) in push-pull and HS configuration (high-side switch turn-on)	I_{OUT} = 0.2 A, R-L load (L = 10 µH) to GND. I = 0.2 A flowing from the IC to the load. EN/DIAG, IN1 or IN2 commutations	380		860	ns
$t_{f(ON)}$	OUT_X and I/Q fall time (from V_{CC} 90% to V_{CC} 10%) in push-pull and LS configuration (low-side switch turn-on)	I_{OUT} = 0.2 A, R-L load (L = 10 µH) to V_{CC}. I = 0.2 A flowing from the load to the IC. EN/DIAG, IN1 or IN2 commutations	380		860	ns

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{r(OFF)}$	OUT_X and I/Q rise time (from V_{CC} 10% to V_{CC} 80%) in push-pull and LS configuration (low-side switch turn-off)	I_{OUT} = 0.2 A, R-L load (L = 10 µH) to V_{CC}. I = 0.2 A flowing from the load to the OUTL (OUTH floating). EN/DIAG or IN1 commutations	380		860	ns
		I_{OUT} = 0.2 A, R-L load (L = 10 µH) to V_{CC}. I = 0.2 A flowing from the load to the OUT (OUTL=OUTH). IN2 commutations			180	ns
$t_{f(OFF)}$	OUT_X and I/Q fall time (from V_{CC} 90% to V_{CC} 10%) in push-pull and HS configuration (high-side switch turn-off)	I_{OUT} = 0.2 A, R-L load (L = 10 µH) to GND. I = 0.2 A flowing from OUTH to the load (OUTL floating). EN/DIAG, or IN1 commutations	380		860	ns
		I_{OUT} = 0.2 A, R-L load (L = 10 µH) to GND. I = 0.2 A flowing from OUT to the load (OUTH =OUTL). IN2 commutations			180	ns

Table 11: Electrical characteristics, logic inputs (IN1, IN2, EN/DIAG and SEL)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input low level voltage (INx, EN/DIAG)				0.3xV_{DD}	V
V_{IH}	Input high level voltage (INx, EN/DIAG)		0.7xV_{DD}			V
V_{IHY}	Input level voltage hysteresis (INx, EN/DIAG)		0.08xV_{DD}			V
I_{IN}	Input current at IN1, IN2, SEL pins	V_{IN} = 5 V			2	µA
I_{EN}	Input current on EN/DIAG pin	V_{EN} = 5 V, internal open drain not active			15	µA
V_{EN}	Voltage drop on EN/DIAG pin	I_{EN} = 5 mA			0.15	V

Table 12: Protection and diagnostic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{clamp}	V_{CC} active clamp	I_{clamp} = 10 mA	38	39	40	V
		I_{clamp} = 2 A (peak value during fast transient only)	40	41	42	
V_{demag}	Demagnetization voltage		38	39	40	
I_{OLS}	Low-side switch load current limitation level in overload and cut-off		-220		-310	mA

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{OLS-PEAK}$	Low-side switch intervention threshold for current limitation and cut-off		-300		-450	mA
I_{OHS}	High-side switch load current limitation level in overload and cut-off		220		310	mA
$I_{OHS-PEAK}$	High-side switch intervention threshold for current limitation and cut-off		300		450	mA
t_{dOUT}	Low and high-side cut-off current delay time		3.6		6.4	ms
t_{rOUT}	Output stage restart delay time after cut-off or thermal protection intervention		55		105	ms
t_{OL}	Overload delay time	OUTH = GND or OUTL = V_{CC}. Turn on the outputs and measure the delay between limitation event and signalization on OL pin. OL pulled to V_{DD} with R = 3.3 kΩ, without any capacitor connected versus GND		2.5		µs
V_{OL}	Voltage drop on OL pin	I_{OL} = 1 mA OUTL short to V_{CC} or OUTH short to GND			0.1	V
I_{OL}	OL pin leakage current	V_{OL} = 5 V internal open drain not active			1	µA
I_{GD}	Ground rail disconnection output current (HS mode)	OUTH short-circuit to ground rail			500	µA
I_{VD}	V_{CC} rail disconnection output current (LS mode)	OUTL short-circuit to V_{CC} rail			500	µA
T_{JSD}	Junction temperature shutdown		150		170	°C
T_{JR}	Junction temperature restart		125		145	
T_{JHYST}	Junction temperature thermal hysteresis			25		

Table 13: Linear voltage regulator

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{DD5}	Regulated output voltage	V_{CC} from 7 V to 36 V, no-load on V_{DD}	4.5	5	5.5	V
$V_{DD3.3}$			3.0	3.3	3.6	
I_{scr}	Short-circuit current limitation	SEL = GND	12		20	mA
		SEL = VDD	10		20	

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
ΔV_{LR}	Line regulation	V_{CC} = 8 to 36 V, T_J = 25 °C, Io = 2 mA			8	mV
ΔV_{LDR}	Load regulation	Io = 2 to 7 mA, T_J = 25 °C			20	mV

6 Output logic

Table 14: Output stage truth table

Operation	EN/DIAG	IN1	IN2	HS configuration (OUTL not connected)	LS configuration (OUTH not connected)	PP (OUTH wired with OUTL)
Normal	1	0	0	Off (active clamp)(1)	On (GND)	GND
Normal	1	0	1	On (V_{CC})	Off	V_{CC}
Normal	1	1	0	On (V_{CC})	Off	V_{CC}
Normal	1	1	1	Off (active clamp)	On (GND)	GND
Normal	0	X	X	Off	Off	High Z (slow demagnetization)(2)
During DT(3)	1	X	X			High Z
Cut-off	(4)	X	X	Off (active clamp)	Off (active clamp)	High Z
UVLO(5)	0	X	X	Off (active clamp)	Off (active clamp)	High Z
Overtemperature	0	X	X	Off (active clamp)	Off (active clamp)	High Z

Notes:

(1)Active clamp (fast demagnetization) is active in case of residual currents on OUTH or OUTL.

(2)See slow demagnetization section.

(3)Dead time is inserted between each HS switch-off and LS switch-on, and vice versa, only if the IC is driven by the IN2 pin. No dead time is inserted when the IN1 pin is commutated.

(4)EN/DIAG pin is driven “high” through a resistor, but the internal open drain is active and the pin is pulled to GND.

(5)When VCC < 2.5 V (typ.), the device is completely turned off.

7 Receiver logic

The level of the signal on I/Q pin is transferred to the $OUT_{I/Q}$ pin, according to the receiver thresholds defined in and truth table below. The receiver is always active independently on the EN/DIAG pin status. The IN1 pin sets the phase relation between I/Q and $OUT_{I/Q}$.

Table 15: I/Q truth table

EN/DIAG	IN2	IN1	I/Q	$OUT_{I/Q}$
X	X	0	0	0
X	X	0	1	1
X	X	1	0	1
X	X	1	1	0
UVLO	X	X	X	0
Overtemperature	X	X	X	IN1 XOR I/Q(1)

Notes:

(1)The receiver keeps working in overtemperature conditions.

Thanks to the internal pull-up and pull-down resistors on OUTH, OUTL and I/Q pins, the receiver logic can be used for the automatic identification of the load connection (high-side or low-side) even in the 3-wire configurations. Referring to the table above, the microcontroller (µC) can force the EN/DIAG = GND and read the information from OUT I/Q: considering the voltage thresholds VI/QTHLH and VI/QTHHL, µC can know whether the load is connected in high-side or low-side. The table below summarize the OUT I/Q logic level according to the load connection and IN1 set-up.

Table 16: Load connection identification by OUTI/Q

EN/DIAG	IN2	IN1	$OUT_{I/Q}$	
			PP-HS	PP-LS
GND	X	0	0	1
	X	1	1	0

8 Output stage operation

8.1 Set output stage

The IC can be operated in high-side, low-side and push-pull mode, according to the electrical connections on OUTH and OUTL pins. Depending on the chosen operation mode, the IC must be driven by the IN1, IN2 or EN/DIAG pins. Table below refers to normal operation mode. For example, in push-pull mode the driving signal (high = VDD, low = GND) could be applied to IN2 or EN/DIAG only, while IN1 is connected to VDD or GND. In high-side and low-side modes only, the driving signal can be applied to IN1.

Table 17: Configuration summary

Configuration	IN1	IN2		EN/DIAG		OUT
Push-pull	GND	Drive signal	High	V_{DD}		H
	V_{DD}		Low			L
			High			L
			Low			H
	X		X	GND		High impedance
	GND	GND		Drive signal	High	L
	GND	V_{DD}				H
	V_{DD}	GND				H
	V_{DD}	V_{DD}				L
	X	X			Low	High impedance

Table 18: Configuration summary 2

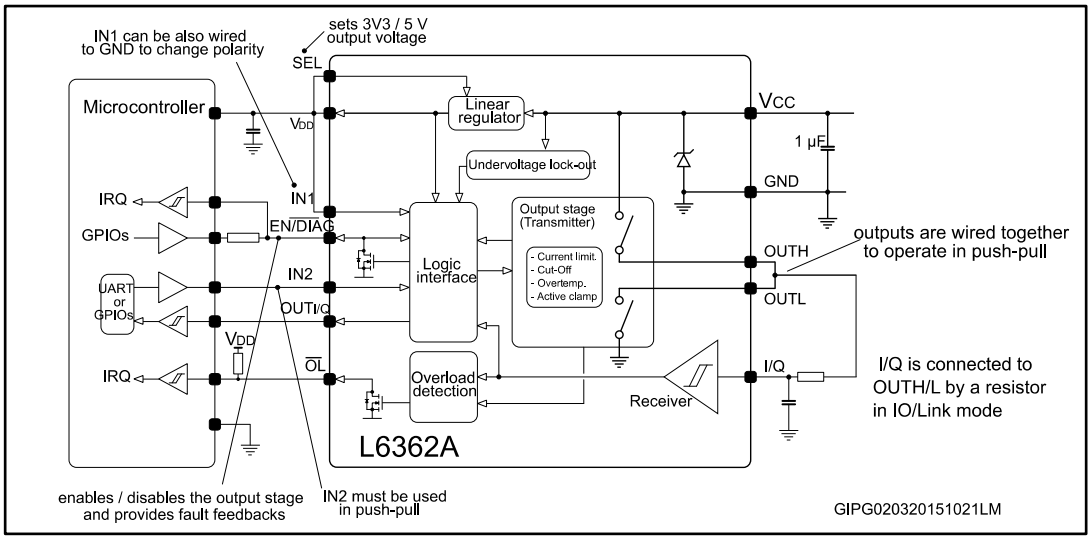
Configuration	IN1		IN2		EN/DIAG	OUTL	OUTH
High-side	Drive signal	High	Drive signal or wire to GND or V_{DD}	GND	V_{DD}	NC	H
		Low					L
		High		V_{DD}			L
		Low					H
		X		X	GND		L
Low-side	Drive signal	High	Drive signal or wire to GND or V_{DD}	GND	V_{DD}	H	NC
		Low				L	
		High		V_{DD}		L	
		Low				H	
		X		X	GND	H	

8.2 Push-pull (PP) and IO-link operation

The IC can be operated in push-pull mode, with slow demagnetization, by wiring OUTH and OUTL together. When OUTH and OUTL are wired together, IC must be driven by the IN2 pin, to allow the dead time function to properly protect the output stage. IN1 pin sets

the phase relation between IN2 and the output stage (OUTH, OUTL). The IO-Link operation is active when I/Q pin is connected to OUTH and OUTL by a resistor. According to the required protections and EMC levels, it could be necessary to protect the I/Q pin by an RC net, see the figure below, *Section 11.3: "Current limitation and cut-off"* and *Table 14: "Output stage truth table"*.

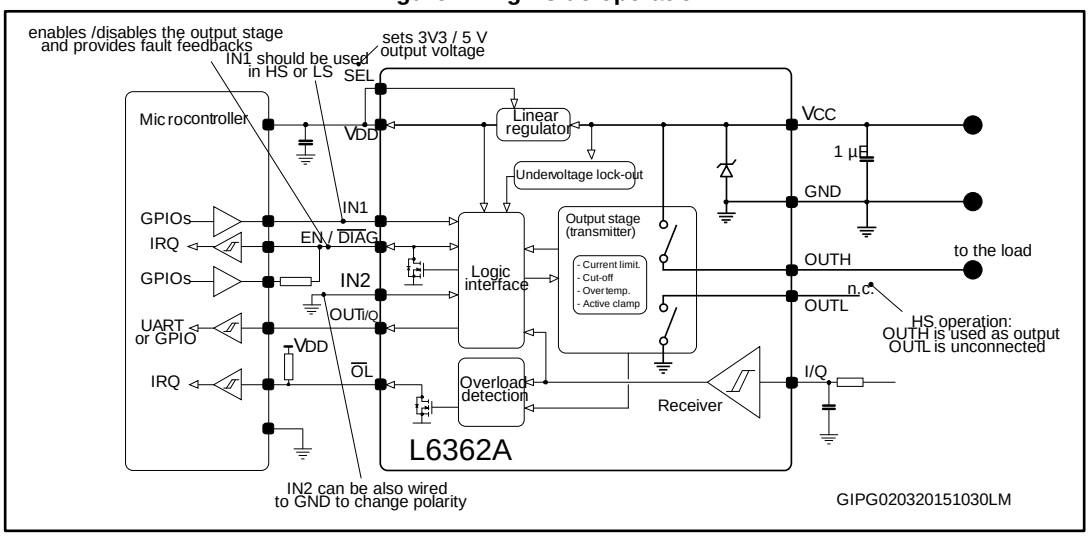
Figure 3: IO-Link operation



8.3 High-side operation

The IC can be operated in high-side mode, with active clamping, by leaving the OUTL pin unconnected. IC should be driven by the IN1 pin and IN2 pin sets the phase relation between IN1 and OUTH. See *Table 14: "Output stage truth table"*.

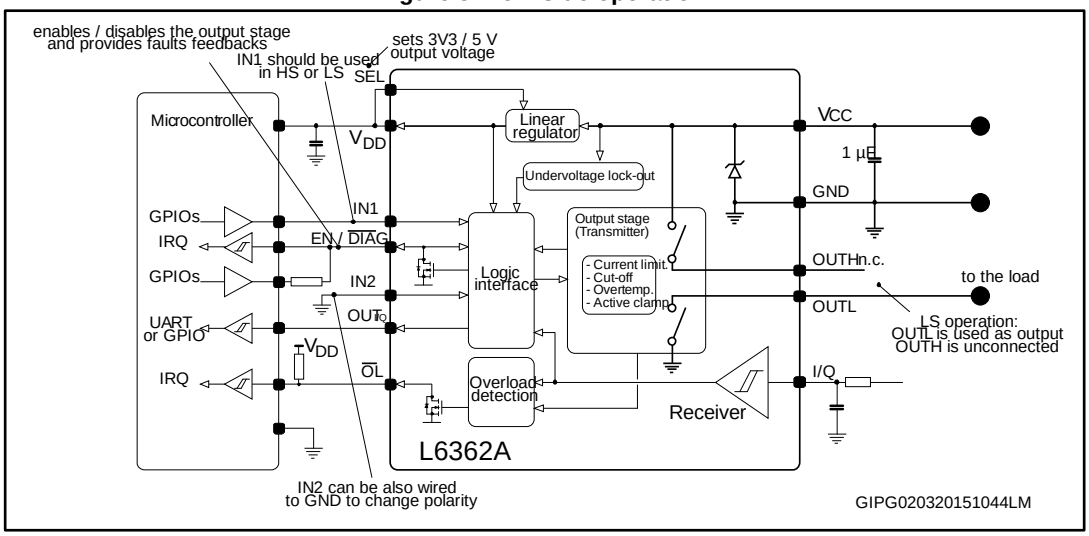
Figure 4: High-side operation



8.4 Low-side operation

The IC can be operated in low-side mode, with active clamping, by leaving the OUTH pin unconnected. IC should be driven by the IN1 pin and IN2 pin sets the phase relation between IN1 and OUTL. See *Table 14: "Output stage truth table"*.

Figure 5: Low-side operation



9 Active clamp

Active clamping is always used in HS and LS configurations. In PP configuration slow demagnetization is used. Active clamp is also known as fast demagnetization of inductive loads or fast current decay. When a high-side driver turns off an inductance, a reversed polarity voltage appears across the load. The OUTH pin is pulled to a voltage below the ground until it reaches the demagnetization voltage, V_{CC}-V_{demag}. The conduction state is linearly modulated by an internal circuitry in order to keep the OUTH pin voltage at about V_{CC} -V_{demag} until the energy in the load has been dissipated. The energy is dissipated both in IC internal switch and load resistance. Similarly, in case of load connected between the LS pin and V_{CC}, at the switch-off (of the low-side switch) the output is pushed to +V_{demag}. See *Table 14: "Output stage truth table"* for the detailed behavior of the power stage in different configurations and conditions.

Figure 6: Active clamp equivalent principle schematic. HS configuration (load to GND)

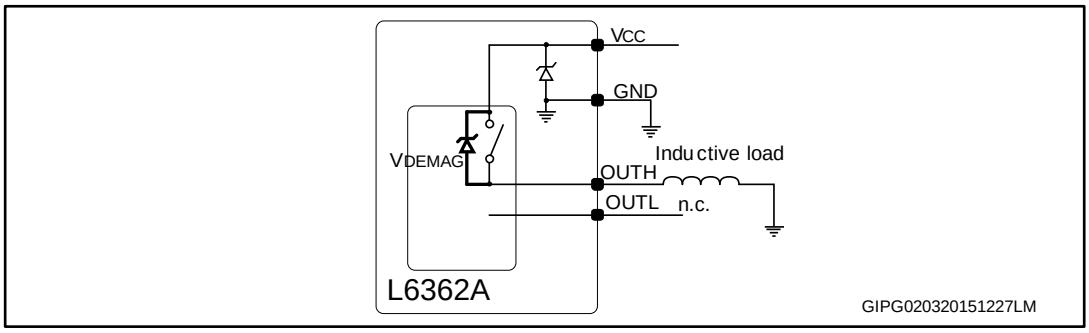


Figure 7: Active clamp equivalent principle schematic. LS configuration (load to VCC)

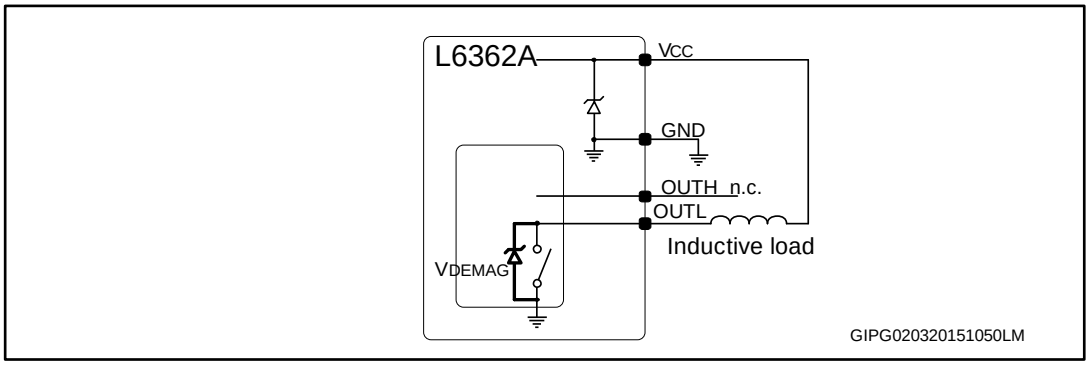


Figure 8: Fast demagnetization operation example. HS configuration (load to GND)

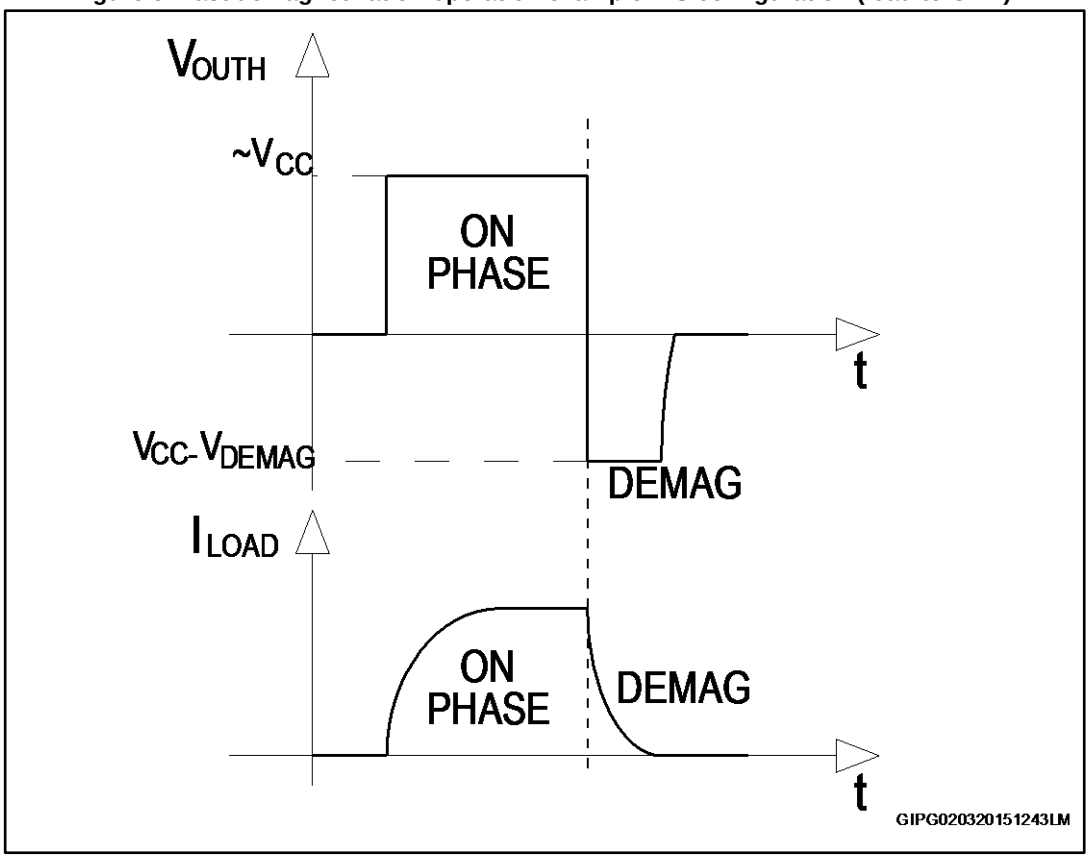
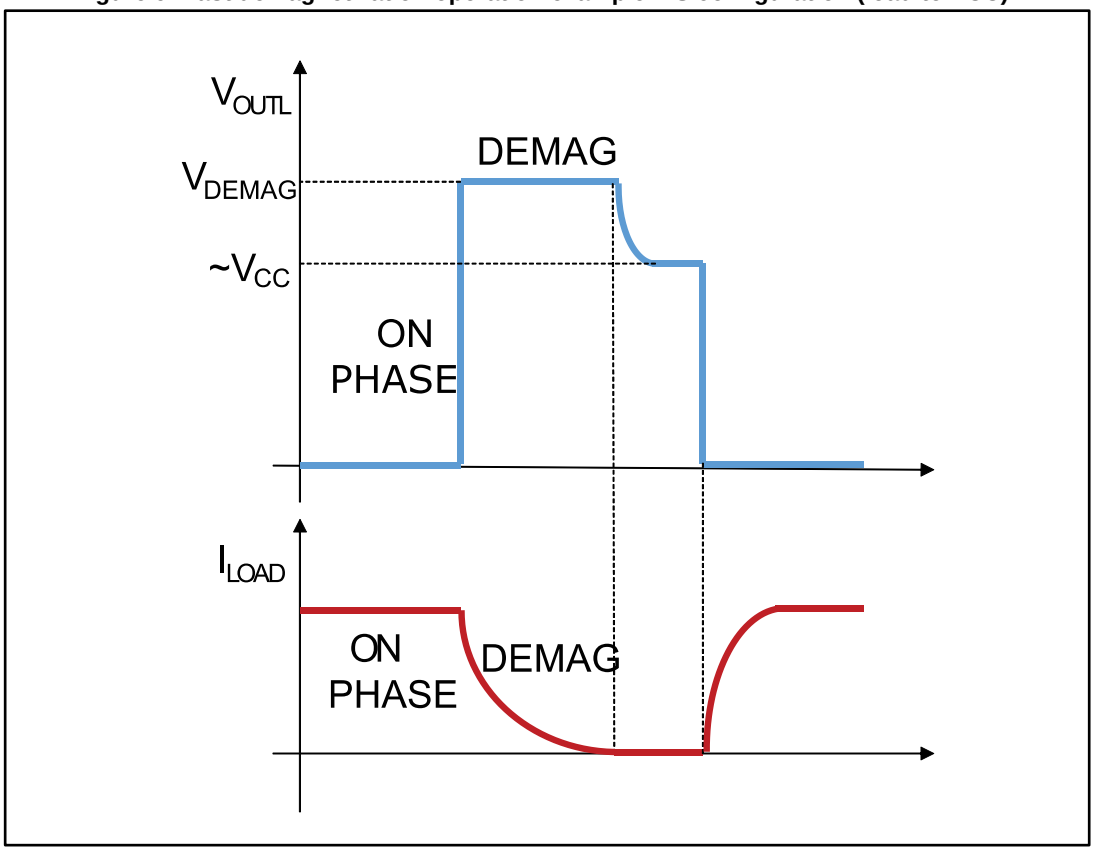


Figure 9: Fast demagnetization operation example. LS configuration (load to VCC)



10 Slow demagnetization

Slow demagnetization is also known as synchronous rectification or slow current decay and it is active in push pull mode. When a high-side driver turns off an inductance, a reversed polarity voltage appears across the load. In push-pull configuration the low-side switch is ON and the OUTH pin is pulled at a voltage slightly (depending on the low-side switch drop) below the ground. The energy is dissipated in both IC internal switch and load resistance. Similarly, in case of load connected between the OUTL pin and V_{CC}, at the switch-off of the low-side switch, the HS switch is ON and the output is pushed to a voltage slightly higher than V_{CC}. Slow demagnetization is always active in PP configurations: the diodes of the integrated switches activate the slow demagnetization even when the IC is driven by EN/DIAG instead of IN2. See *Table 14: "Output stage truth table"* for the detailed behavior of the power stage in different configurations and conditions.

Figure 10: Slow demagnetization principle operation. (PP, load to GND)

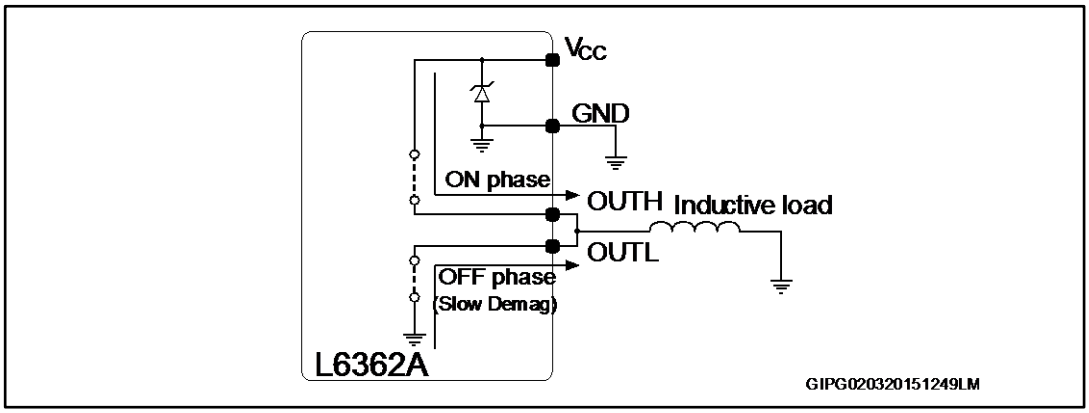


Figure 11: Slow demagnetization operation example. HS configuration (load to GND)

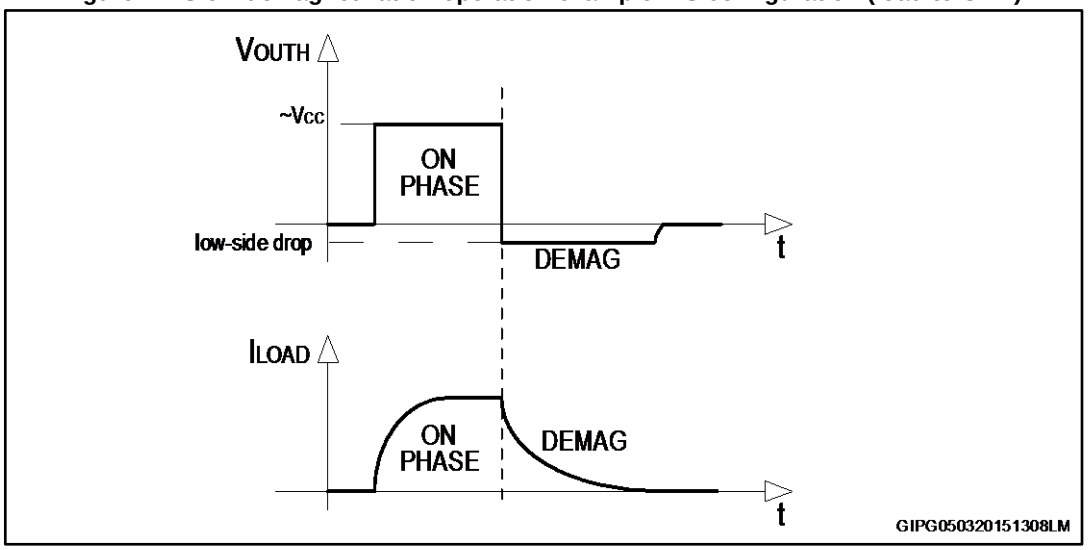
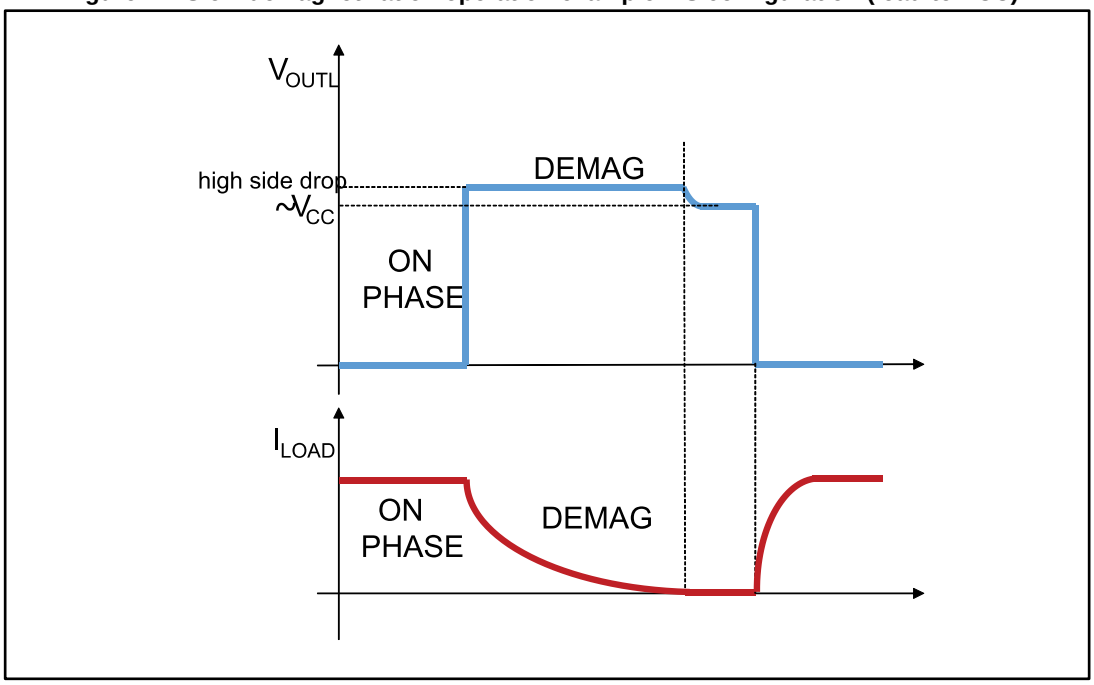


Figure 12: Slow demagnetization operation example. LS configuration (load to VCC)



11 Protection and diagnostic

The IC integrates several protections to ease the design of a robust application. Protection functions are intended to avoid IC damage in fault conditions and are not intended for continuous operation. Continuous and repetitive operations of protection functions may reduce the IC lifetime.

Table 19: Diagnostic truth table

Operation	DIAG	OL	HS configuration (OUTL not connected)	LS configuration (OUTH not connected)	PP (OUTH wired to OUTL)
During DT	1	1			High Z slow demagnetization
Cut-off	0	1	Off (active clamp)(1)	Off (active clamp)	High Z slow demagnetization
Current limitation	1	0	Linearly controlled	Linearly controlled	Linearly controlled
UVLO(2)	0	Not controlled	Off (active clamp)	Off (active clamp)	High Z active clamp
Overtemperature	0	1	Off (active clamp)	Off (active clamp)	High Z slow demagnetization

Notes:

(1)Active clamp (fast demagnetization) is active in case of residual currents on OUTH or OUTL. If OUTH and OUTL are wired together, slow demagnetization is used only in case of overtemperature protection intervention.

(2)When V_{CC} < 2.5 V (typ.), the device is completely turned off.

11.1 Undervoltage lock-out

The output stage, the receiver and several internal circuitries turn off as the supply voltage falls below the turn-off threshold (V_{UVOFF}). Normal operation restarts, after V_{CC} exceeds the turn-on threshold (V_{UVON}). Turn-on and turn-off thresholds are defined in table *Table 7: "Supply"*.

11.2 Overtemperature

The output stage turns off as the internal IC temperature (T_J) exceeds the shutdown temperature see *Table 11: "Electrical characteristics, logic inputs (IN1, IN2, EN/DIAG and SEL) "*. Normal operation restarts when the T_J goes back below the restart temperature (T_{jr}) and, in case the cut-off protection is triggered too, after the t_{rout} delay time expires.

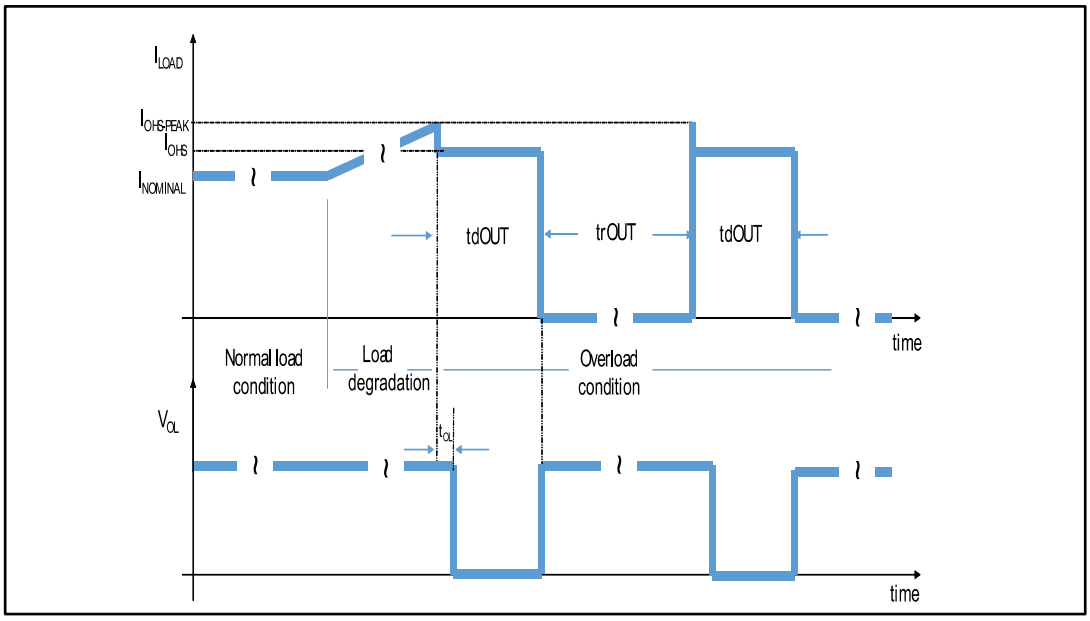
11.3 Current limitation and cut-off

The output current of the power stage is internally limited, see *Table 12: "Protection and diagnostic"*.

The current limitation circuit is active when the output current triggers peak threshold ($I_{OHS-PEAK}$ for high-side, $I_{OLS-PEAK}$ for low-side) by limiting the output current to I_{OHS} (or I_{OLS} for low-side). The current limitation persists until the current required by the load becomes lower than the limitation level (I_{OHS} or I_{OLS}).

If the output stage remains in a current limitation condition for a time longer than the t_{dOUT} delay, the cut-off occurs, therefore the output stage turns off and restarts after the t_{rOUT} restart time. Please notice that the power dissipated by the IC can be significantly high in current limitation condition.

Figure 13: Output current in overload condition



11.4 Dead time

Dead time protection is also known as cross-conduction or shoot-through protection. When used in push-pull configuration, OUTH and OUTL pins are wired together. A dead time is necessary between each high-side switch (HS) turn-off and low-side switch (LS) turn-on, and vice versa, in order to avoid cross-conduction of the two switches. The IC integrates a dead time generator to properly drive the output stage avoiding cross-conduction. The dead time is inserted only when the IN2 pin changes its state. The dead time is not inserted when IN1 or EN/DIAG pin changes its state. The IC must be driven by the IN2 pin in case of push-pull configuration (OUTH and OUTL wired together). The IC should be driven by IN1 in case of HS (OUTL left unconnected) or LS (OUTH left unconnected) configurations, in order to avoid unnecessary delays when the output switch turns on. In any case, the EN/DIAG pin can be also driven by an external source (for example a microcontroller).

11.5 EN/DIAG pin

The EN/DIAG pin is internally wired to a diagnostic open drain transistor, so it must be driven by a series resistor only. The open drain transistor is active (turn-on) while any of the following fault conditions is present, independently on the INx pin state:

- Undervoltage lock-out (2.5 V < V_{CC} < V_{UVOFF})
- Overtemperature detected (T_J is above the threshold specified in *Table 12: "Protection and diagnostic"*
- The output turns off due to the cut-off protection

Please note that in case of faults, the output stage (OUTH and OUTL) is disabled by an internal path, independently on the status of the EN/DIAG pin. Besides, note that the diagnostic signal is not visible if the EN/DIAG pin is pulled low from the microcontroller.

11.6 OL (overload) pin

The integrated open drain transistor is active (turn-on) in case of overload conditions.

Overload is detected when the output current exceeds the $I_{OLS-PEAK}$ or $I_{OHS-PEAK}$ threshold. The open drain transistor is active with a small delay (t_{OL}), after the overload condition is detected. Overload is not detected when EN/DIAG pin is at a low logic level. Overload is not detected in cut-off conditions: if the output stage remains in a current limitation (OL) condition for a time longer than the t_{dOUT} delay, the output stage is turned off (cut-off condition) and the OL pin is released. The output stage is restarted after the t_{rOUT} restart time.

11.7 Reverse polarity protection

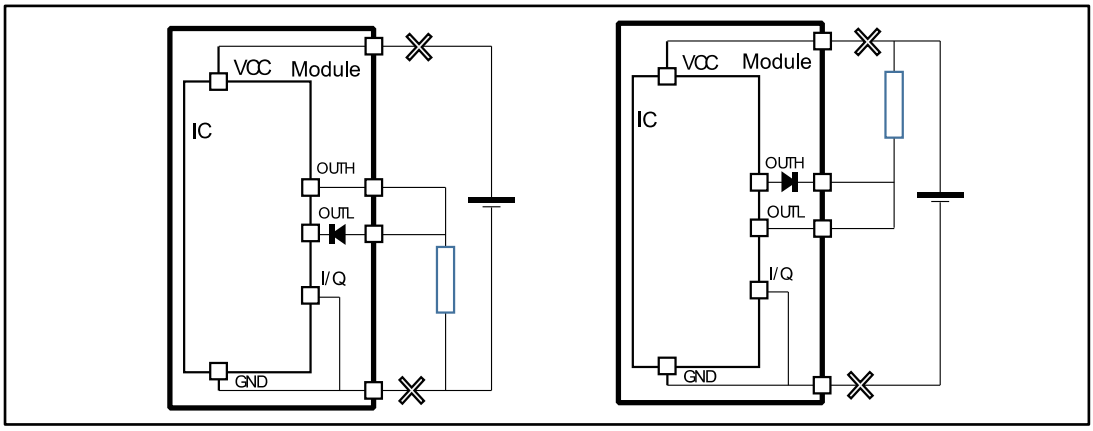
The integrated reverse polarity protection (RPP) avoids any damage to the IC in case of erroneous swapped connection of the high voltage pins to the supply and reference rails. These protected pins, despite reverse polarity, are: VCC, GND, OUTH, OUTL and I/Q. In order to protect the IC against any reverse current from load (e.g due to different and unbalanced supply load voltage rails), please refer to section below.

11.8 GND/VCC open wire protection

The GND and V_{CC} open wire protections are intended as protections against the disconnection of the application module from ground and/or supply rails. The IC is self-protected against these events both for high-side and low-side configurations.

For Push-Pull configuration an external blocking diode in series to OUTH is necessary if load is connected to V_{CC} supply rail. An external diode in series to OUTL is necessary if the load is connected to GND reference rail.

Figure 14: PP configuration, open wire external protections



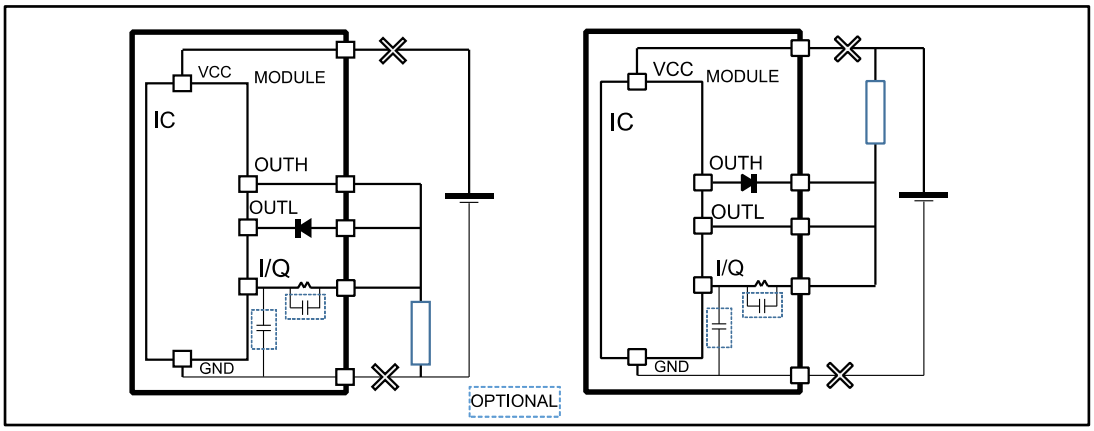
The same considerations for PP configuration are valid for IO-Link configuration. Furthermore, the external resistor between I/Q and load has to be selected to force the IC in UVLO off. A 22 kOhm resistor protects the IC up to V_{CC} = 36 V, even though a lower value resistance can be used according to the following design rule:

$R_{ext} = [V_{CC(max.)} - V_{uvoff(min.)}]/I_{CC}(min.)$

Despite the presence of the external components listed above, the IC is able to meet the standard EMC requirements according to IEC 60947-5-2. Only if higher voltage levels are necessary, then a small $C_{I/Q}$ capacitance between I/Q and GND could be necessary: the

effects at high switching frequency of R_{ext} and $C_{I/Q}$ can be limited by a further small capacitance in parallel to R_{ext}.

Figure 15: IO-Link configuration, open wire external protections



12 Typical application

Figure 16: Typical IO-Link sensor application 2

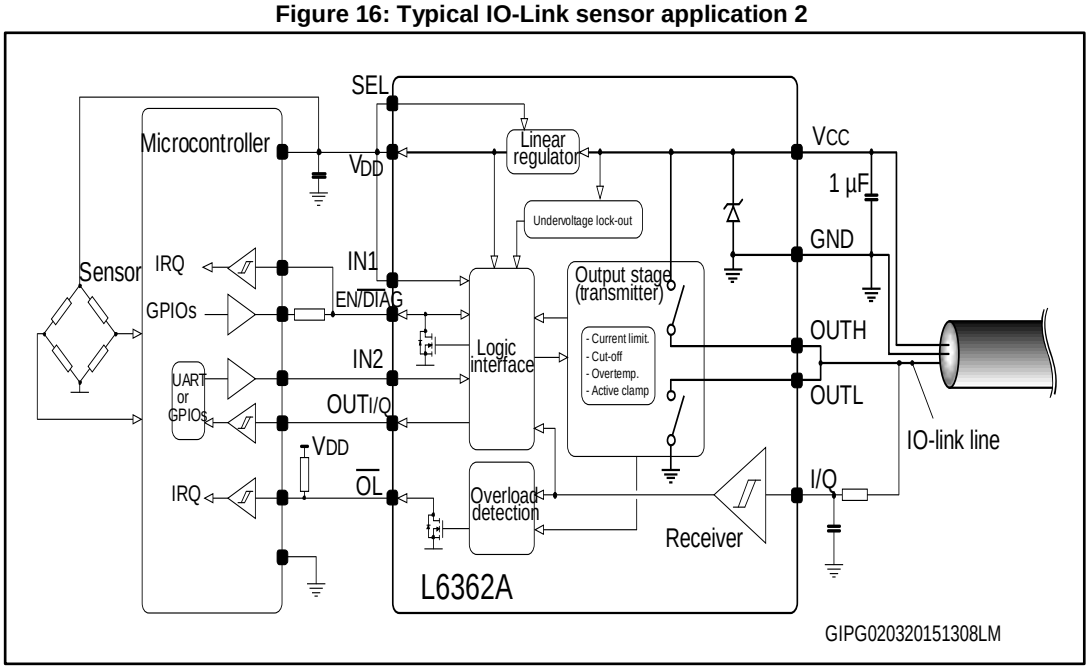


Figure 17: Sensor application without microcontroller

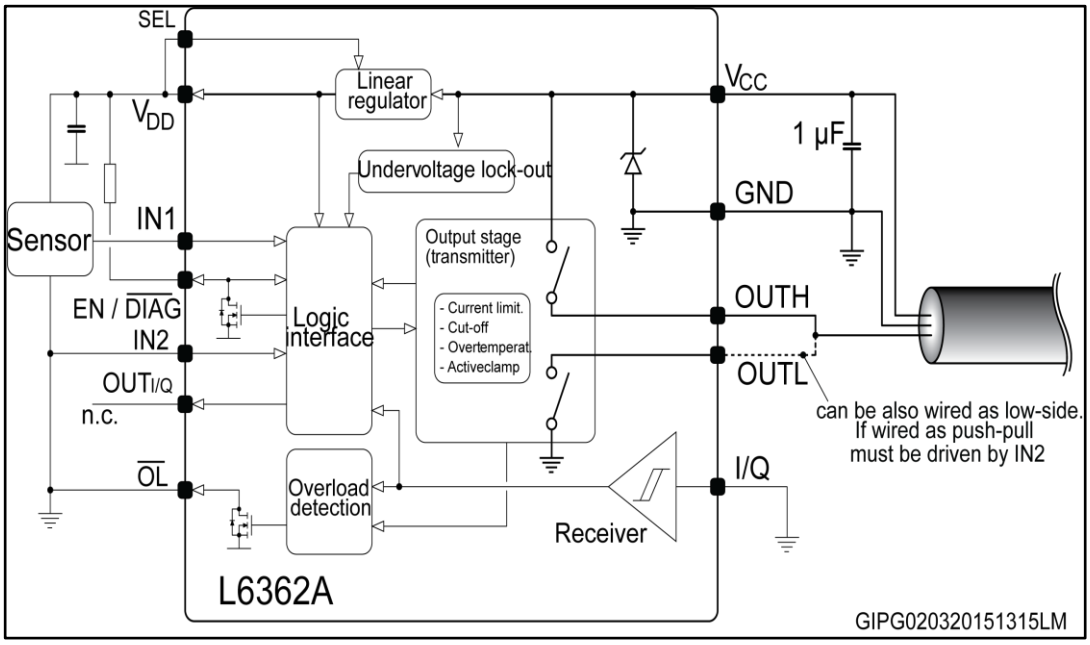
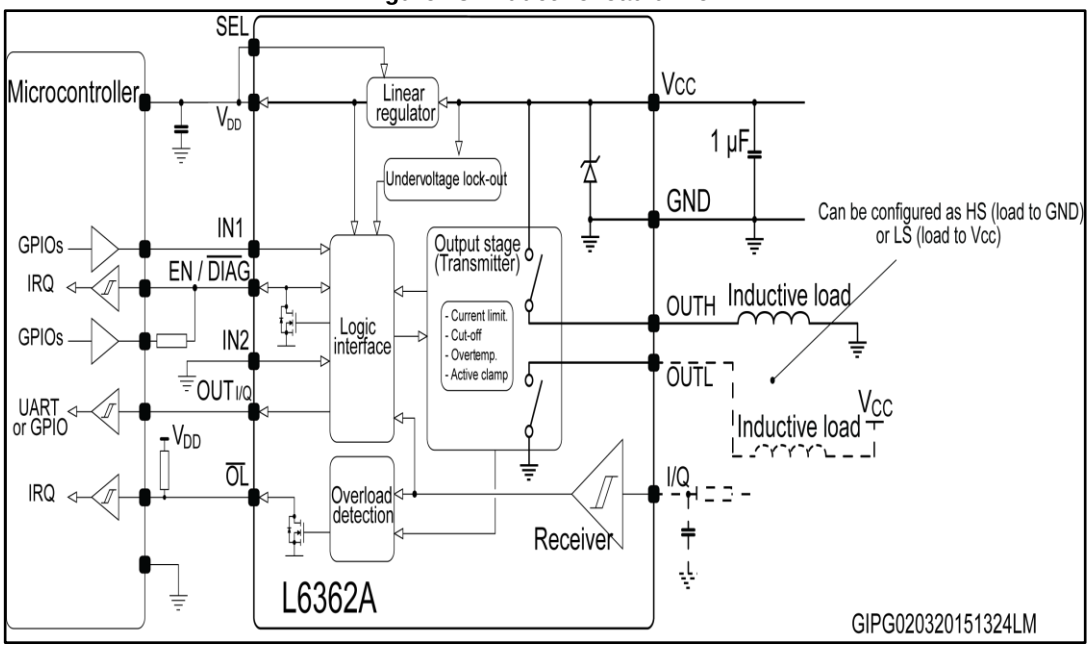


Figure 18: Inductive load driver



13 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

13.1 VFDFPN 12L (3x3x0.90 mm) package information

Figure 19: VFDFPN 12L (3x3x0.90 mm) package outline

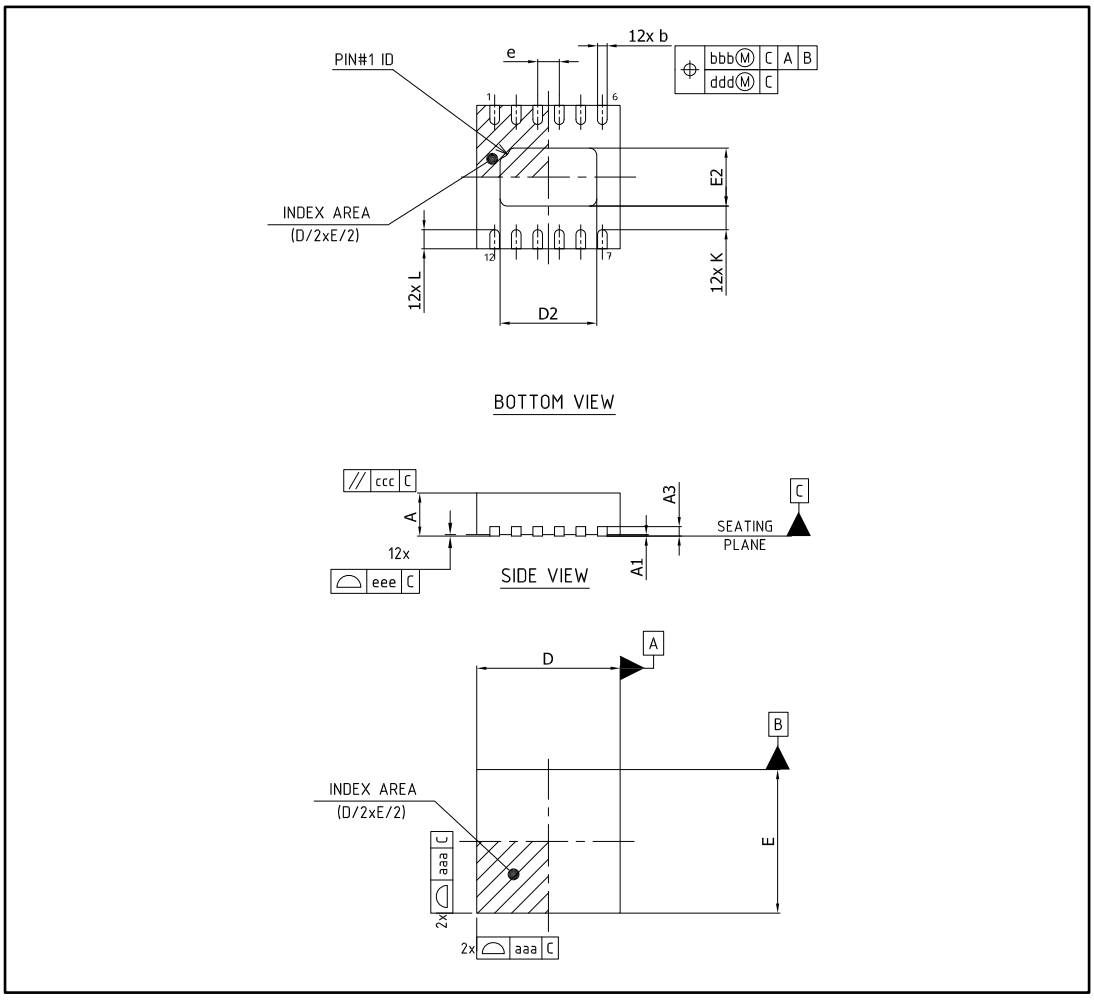
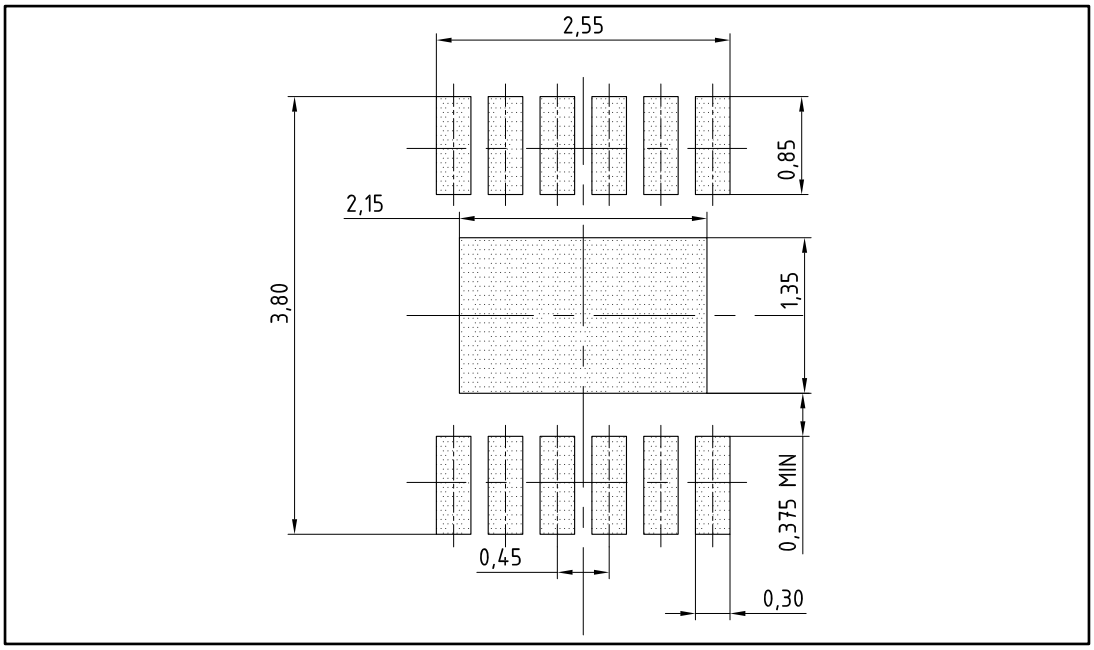


Table 20: VFDFPN 12L (3x3x0.90 mm) package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A3		0.20 BSC	
b	0.15		0.30
D		3.00 BSC	
E		3.00 BSC	
D2	1.87	2.02	2.12
E2	1.06	1.21	1.31
e		0.45 BSC	
L	0.30	0.40	0.50
k	0.20		
aaa		0.05	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	

VFDFPN stands for thermally enhanced plastic: very thin, fine pitch, dual flat package and no lead. The lead size is comprehensive of the thickness of the lead finishing material. Dimensions do not include mold protrusion, not to exceed 0.15 mm. Package outline exclusive of metal burr dimensions. Pits, visible to the naked eye, are not allowed on the marking area.

Figure 20: VFDFPN 12L (3x3x0.90 mm) recommended footprint



13.2 VFDFPN 12L (3x3x0.90 mm) packing information

Figure 21: VFDFPN 12L (3x3x0.90 mm) carrier tape outline

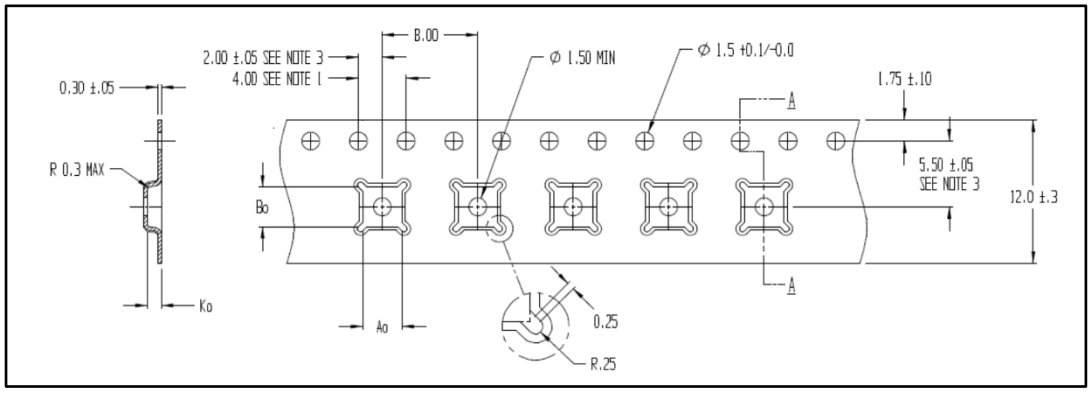
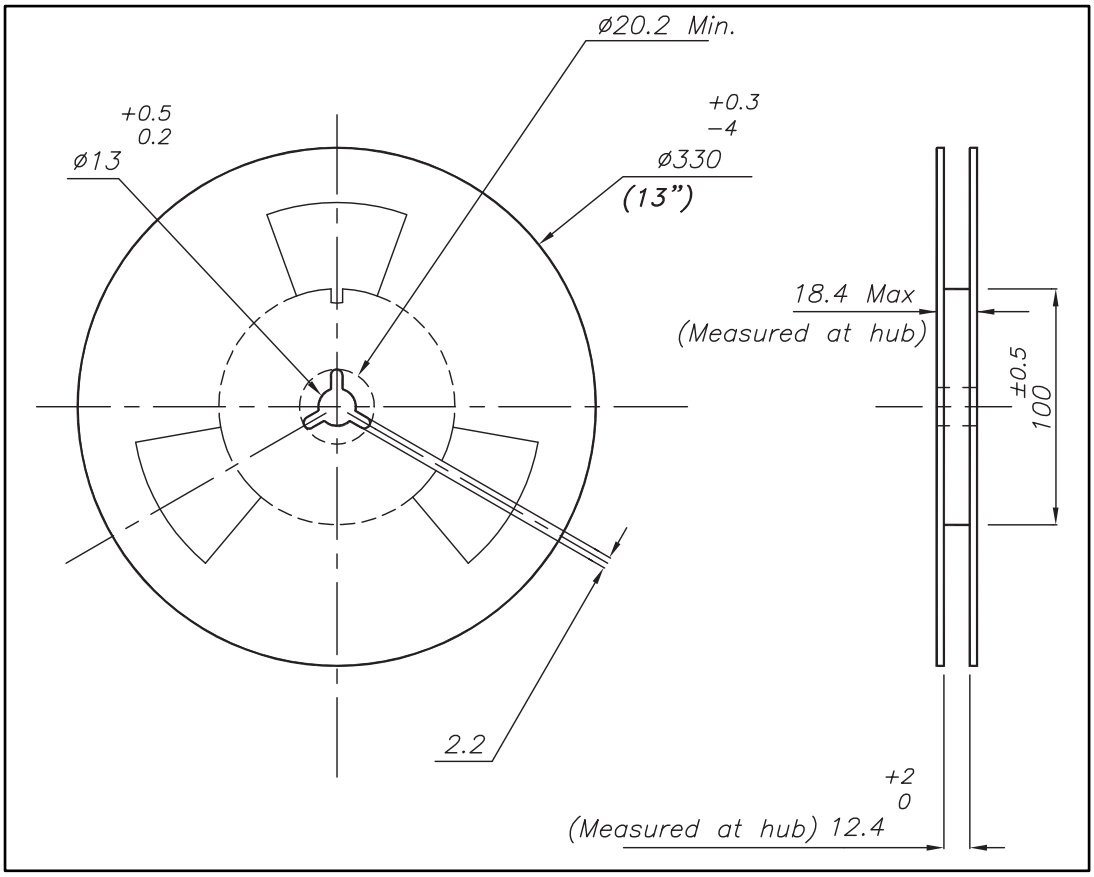


Figure 22: VFDFPN 12L (3x3x0.90 mm) reel outline



14 Revision history

Table 21: Document revision history

Date	Revision	Changes
20-Mar-2015	1	Initial release.
04-May-2015	2	Updated *features*. Updated *section 2.3*. Updated min. and max. value of $I_{OLS-PEAK}$ parameter in *table 3*. Added V_{EN} parameter to *table 11*. Added V_{OL} and I_{OL} parameter to *table 12*. Updated EN/DIAG value in *table 14* and DIAG value in *table 17*.
29-Jan-2016	3	Updated *section"Features"*, *section "Description"*, *table 2: "Pin description"*, all tables related to *section 5: "Electrical characteristics", section 6: "Output logic", section 9: "Active clamp", section 10: "Slow demagnetization", section 11: "Protection and diagnostic"*.
03-Feb-2016	4	Document status promoted from preliminary to production data.
16-Mar-2016	5	Updated the *device summary table*.
01-Apr-2016	6	Updated *VFDFPN 12L (3x3x0.90 mm) package information*.
28-Apr-2016	7	Updated table titled "*Output stage*". Updated *"Current limitation and cut-off" section*. Changed figure titled *"Output current in overload condition"*.
13-Jun-2016	8	Added *VFDFPN 12L (3x3x0.90 mm) packing information*.
20-Jul-2016	9	Updated *OUTI/Q*
22-Nov-2017	10	Updated the description and the device summary table. Updated *Figure 1: "Block diagram"*. Updated *Section 2.7: "OL"*. Updated *Section 3: "Absolute maximum ratings"*. Updated *Table 7: "Supply"*, *Table 9: "I/Q receiver"* and *Table 18: "Configuration summary 2"*. Updated *Section 8.1: "Set output stage"*. Updated *Figure 3: "IO-Link operation"*, *Figure 9: "Fast demagnetization operation example. LS configuration (load to VCC)"*, *Figure 14: "PP configuration, open wire external protections"* and *Figure 15: "IO-Link configuration, open wire external protections"*. Added *Section 11.8: "GND/VCC open wire protection"*.

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